

# Low Operating Voltage and Immediate Read-After-Write of HZO-Based Si Ferroelectric Field-Effect Transistors with High Endurance and Retention Characteristics

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The study demonstrates HfZrO<sub>x</sub> (HZO)-based Si ferroelectric field-effect transistors (FeFETs) with a low operating voltage (1.5 V) and immediate read-after-write operation (100 ns) via HZO thickness scaling, electron-beam-irradiation (EBI) treatment, and interfacial layer (IL) scavenging. With these three strategies, reduced operating voltage, immediate read-after-write capability, and improved endurance (>10<sup>8</sup> cycles) and retention (extrapolated 10-year) characteristics are achieved in FeFETs. The improved characteristics of FeFETs are attributed to the reduced operating voltage by HZO thickness scaling, the ferroelectric orthorhombic phase-oriented crystallization by EBI treatment, and the reduced gate voltage drop across the IL and reduced depolarization field by the IL scavenging. It is believed that this work contributes to the development of low-power and fast-read FeFETs.

devices are becoming essential to overcome the limitations of conventional computing architecture because not only data traffic has become extremely heavier, but it also requires access to a tremendous amount of data. For next-generation computing, ferroelectric materials are promising due to their non-volatility of polarization, high speed, low power consumption, and multifunctionality, enabling their use as both logic and memory devices within a single device.<sup>[1,2]</sup> However, as devices are scaled down to the nanoscale dimension, retaining the ferroelectricity of conventional perovskite-structure materials is challenging, which hinders research on the ferroelectric device.

## 1. Introduction

Recently, with the innovation of data-intensive applications such as big data, artificial intelligence, and machine learning and battery-powered devices such as smartphones, wearables, portables, Internet-of-Things, low-power, and high-speed memory

Since the first discovery of ferroelectricity in 10 nm thick Si-doped HfO<sub>2</sub>,<sup>[3]</sup> HfO<sub>2</sub>-based ferroelectric materials are gaining interest again, thanks to their scalability and compatibility with complementary metal-oxide-semiconductor technology. Various dopants that exhibit ferroelectricity in HfO<sub>2</sub> thin films such as Al,<sup>[4]</sup> Gd,<sup>[5]</sup> La,<sup>[6]</sup> Sc,<sup>[7]</sup> Y,<sup>[8]</sup> and Zr<sup>[9]</sup> have been studied, and among the proposed dopants, Zr has the higher feasibility because Zr has almost identical physical properties as Hf, including atomic radius, crystal phase, and lattice parameter, thus, it is easy to integrate into HfO<sub>2</sub>. In addition, unlike other dopants that require precise control of doping concentration within a 5 at% range, Zr exhibits a wide process window.<sup>[10]</sup> Despite the several advantages of HfZrO<sub>2-x</sub> (HZO), the high operating voltage,<sup>[11]</sup> poor endurance,<sup>[12]</sup> and read latency<sup>[13]</sup> of HZO-based ferroelectric field-effect-transistor (FeFET) are critical obstacles.

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Most of the characteristics requiring improvement are caused by the interfacial layer (IL) that is unavoidably formed between the ferroelectric layer and the semiconductor substrate. This phenomenon changes the gate stack structure of FeFET to the metal-ferroelectric-insulator-semiconductor (MFIS) structure even if IL is not intentionally inserted.<sup>[14]</sup> In general, SiO<sub>x</sub> with a thickness of 1 nm is formed as IL on a Si substrate. Since the dielectric constants of SiO<sub>2</sub> and HZO are typically 3.9 and 30,<sup>[15]</sup> respectively, in the MFIS structure of 10 nm thick HZO, the voltage drop distribution across the gate oxide is 43.5% and 56.6% for the IL and HZO, respectively, according to capacitive division. Additionally, considering the voltage drop in the Si substrate and flat band potential, and including polarization

## Three Strategies to Improve MFIS Structure

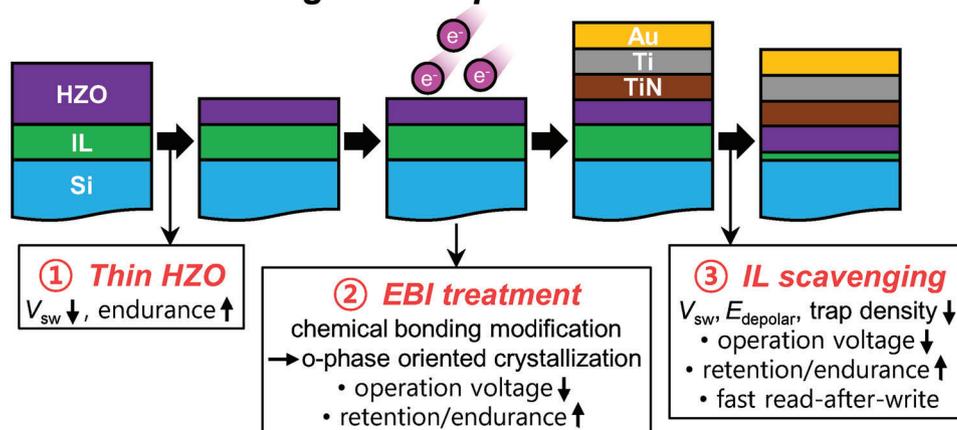


Figure 1. Schematic illustrations of three strategies to improve MFIS structure.

( $20 \mu\text{C cm}^{-2}$ ), charge trapping ( $10^{14} \text{ cm}^{-2}$ ),<sup>[16]</sup> and depolarization field, the electric field across the IL at the gate voltage ( $V_g$ ) of 4 V is  $>20 \text{ MV cm}^{-1}$ , which is very severe stress. The additional voltage drop and severe electrical stress across the IL cause an increase in the switching voltage and the degradation of endurance characteristics in the MFIS structure. In order to alleviate the electrical stress applied across the IL, methods of inserting a high- $k$  material<sup>[17–20]</sup> and reducing the thickness of the IL<sup>[21,22]</sup> have been reported.

In addition to the voltage drop across the IL, the charge trapping caused by the IL also impairs the endurance characteristics of the MFIS structure.<sup>[23]</sup> Moreover, oxygen vacancy, a defect mainly formed at the interface between HZO and IL, creates defect levels near the conduction band,<sup>[24]</sup> which causes electron trapping. As a result, when a positive pulse is applied as a write operation, not only polarization switching but also electron trapping is induced, and read latency occurs as the trapped electrons are gradually de-trapped over time.<sup>[13]</sup> The depolarization field generated by the IL also deteriorates the retention characteris-

tics of the MFIS structure.<sup>[25]</sup> The decrease in IL thickness and increase in the dielectric constant of IL, which alleviated voltage drop and electrical stress, can also mitigate charge trapping and depolarization field.<sup>[22,26]</sup> Methods of forming a high-quality interface using direct<sup>[12]</sup> and remote<sup>[21,27]</sup> scavenging that can reduce charge trapping are also proposed.

In order to improve the performance of FeFET, IL engineering is important in the MFIS structure, but the engineering of the ferroelectric layer is also indispensable. First of all, reducing the thickness of HZO film can achieve a reduction in switching voltage ( $V_{sw}$ ) and an improvement in endurance.<sup>[28]</sup> However, there is a trade-off in that the temperature of the post-metallization annealing for inducing the ferroelectric orthorhombic phase is increased. Other approaches have been reported to improve device performance by surface treatment such as microwave annealing<sup>[29,30]</sup> and plasma treatment,<sup>[31,32]</sup> and to improve ferroelectricity by generating defects,<sup>[33,34]</sup> i.e., oxygen vacancy, using sputtering and ion bombardment. In particular, oxygen vacancy in HZO film plays an important role in favoring the formation of a ferroelectric orthorhombic phase during the annealing process.<sup>[35,36]</sup>

In this work, we utilized HZO thickness scaling, electron-beam-irradiation (EBI) treatment, and IL scavenging as three strategies to reduce the operating voltage, promote the ferroelectric orthorhombic phase-oriented crystallization, and reduce IL thickness, respectively. EBI treatment can induce sub-oxides in HZO films, which not only formed more orthorhombic phase in the subsequent PMA but also reduced the bulk trap density. Reducing the IL thickness minimizes the  $V_g$  drop across the IL, allowing sufficient electric field to be applied to the HZO, which realizes a low-voltage operation. In addition, IL scavenging induced during post-metallization annealing (PMA) improves endurance and retention characteristics by reducing interfacial trap density.<sup>[22,27]</sup> Finally, we achieved FeFETs capable of low operating voltage (1.5 V) and immediate read-after-write operation (100 ns) with high endurance ( $>10^8$  cycles) and retention (extrapolated 10 years) characteristics. We believe that our strategies of HZO thickness scaling, EBI treatment, and IL scavenging are promising for improving the performance of FeFETs.

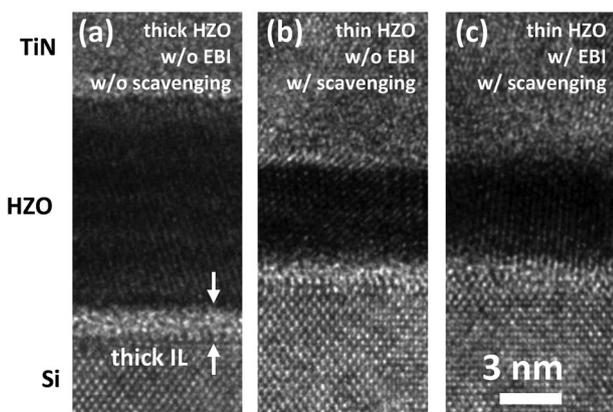
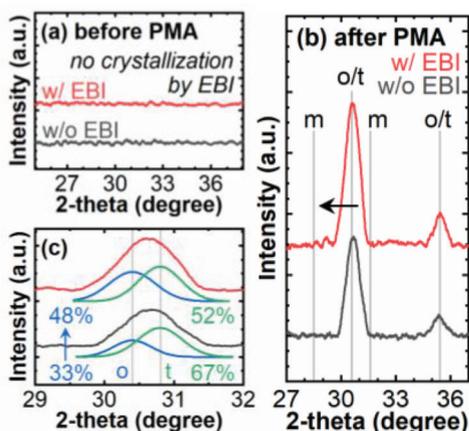


Figure 2. Cross-sectional TEM images of a) thick HZO without EBI treatment and without scavenging (10 nm, no EBI, Au/TiN gate metal stack), b) thin HZO without EBI treatment with scavenging (5 nm, no EBI, Au/Ti/TiN gate metal stack), and c) thin HZO with EBI and with scavenging (5 nm, EBI of 100 V, Au/Ti/TiN gate metal stack). All stacks are after PMA.



**Figure 3.** GIXRD spectra of HZO films without EBI and with EBI treatment a) before PMA and b) after PMA. c) The deconvolution of peaks appeared at  $30.6^\circ$ .

## 2. Results and Discussion

### 2.1. Strategies for Improving Device Performance in MFIS Structures

Figure 1 shows three strategies for improving the MFIS structure using HZO thickness scaling, EBI treatment, and IL scavenging. As a method of scaling the HZO thickness, it is expected to reduce the operating voltage and improve endurance characteristics. EBI treatment modifies the chemical bonding state of HZO film to promote ferroelectric orthorhombic phase-oriented crystallization in the subsequent PMA process, resulting in a decrease in operating voltage and improvement in retention and endurance characteristics. Lastly, IL scavenging can reduce the operating voltage, improve retention and characteristics, and reduce read latency by scaling IL thickness. It is expected that the performance of HZO-based FeFETs can be comprehensively improved by combining the three strategies. The device fabrication flow and structural schematic are depicted in the Experimental Section and Figure S1 (Supporting Information).

### 2.2. Effects of Three Strategies on HZO Films

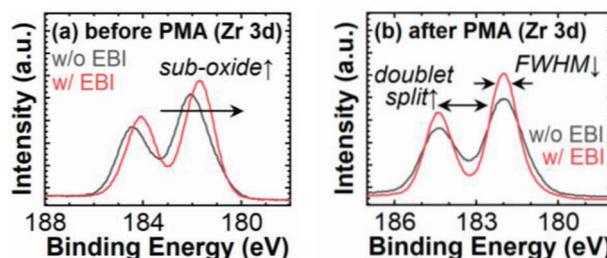
Figure 2a–c shows the cross-sectional TEM images of the fabricated gate stacks of 10 nm HZO without EBI treatment and without scavenging, 5 nm HZO without EBI treatment and with scavenging, and 5 nm HZO with EBI treatment and with scavenging. The thickness of the HZO film was reduced from 10 to 5 nm, and IL was successfully removed by IL scavenging induced by Ti inserted into the gate metal stack. It is quite difficult to find a clear  $\text{SiO}_x$  IL between HZO and Si (Figure 2b,c). However, ferroelectric orthorhombic phase-oriented crystallization by EBI treatment, which was conducted before gate metal stack deposition was not noticeable in microscopic cross-sectional TEM images. For a further macroscopic and comprehensive structural analysis, grazing incidence X-ray diffraction (GIXRD) and X-ray photoelectron spectroscopy (XPS) analysis were performed.

Figure 3 shows the results of GIXRD analysis of HZO films without EBI and with EBI treatment before PMA and after PMA.

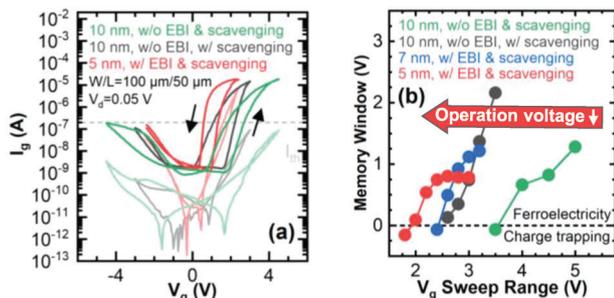
As shown in Figure 3a, before PMA, both HZO films without EBI and with EBI treatment were amorphous and no peaks appeared, which indicates EBI treatment did not affect the physical structure of HZO before PMA. However, after PMA, it was confirmed that the ferroelectric orthorhombic phase and tetragonal phase were formed for both HZO films without EBI and with EBI treatment (Figure 3b). According to several studies, the peak at  $30.6^\circ$  can be deconvoluted into the orthorhombic phase at  $30.4^\circ$  and the tetragonal phase at  $30.8^\circ$ .<sup>[37]</sup> Although GIXRD analysis is difficult due to the nearly identical XRD patterns of the orthorhombic phase and tetragonal phase of HZO, the peaks at  $30.6^\circ$  were precisely deconvoluted using a Gaussian function and shown in Figure 3c. The peak at  $30.6^\circ$  of HZO without EBI was deconvoluted into the orthorhombic phase of 33% and tetragonal phase of 67%, while that of HZO with EBI was deconvoluted into 48% and 52%, respectively. The deconvolution of peaks at  $30.6^\circ$  suggests that more ferroelectric orthorhombic phase was induced in HZO with EBI than in HZO without EBI after PMA. The result that more orthorhombic phase was induced in HZO with EBI after PMA was due to the generation of sub-oxide in HZO by EBI, as shown in the XPS spectra in Zr 3d (Figure 4a). EBI treatment did not affect the physical structure of HZO but modified the chemical bonding state before PMA. Furthermore, after PMA, the doublet in Zr 3d of HZO with EBI was more clearly separated than that of HZO without EBI and the full-width at half-maximums of the peaks decreased in HZO with EBI (Figure 4b), indicating more homogeneous chemical bonding states. Here, sub-oxide in HZO before crystallization by PMA was found to be effective to promote orthorhombic phase-oriented crystallization as previously reported.<sup>[35,36]</sup> The effect of increasing the orthorhombic phase by EBI, reducing the bulk trap density, is discussed in detail in the next section.

### 2.3. Effects of Three Strategies on HZO-Based FeFETs

Then, we systematically investigated the electrical characteristics of ferroelectric field-effect transistors (FeFETs) with our strategies. Figure 5 shows the DC transfer curves and memory window (MW) of fabricated FeFETs. The  $V_{th}$  values of FeFETs were derived according to the constant current method ( $I_{th} = W/L \times 10^{-7}$ ). As shown in Figure 5a, ferroelectric counterclockwise hysteresis was exhibited in all FeFETs. The MW values were 1.28, 2.30, and 0.74 V at  $V_g$  sweep of 5, 4, and 2.4 V for HZO of 10 nm without EBI and without scavenging, HZO of 10 nm without EBI and with scavenging, and HZO of 5 nm with EBI and with scavenging, respectively. Figure 5b shows the MW value according



**Figure 4.** XPS spectra in Zr 3d of HZO films without EBI and with EBI treatment a) before PMA and b) after PMA.



**Figure 5.** a) Transfer curves and b) MW of FeFETs according to the  $V_g$  sweep in the transfer curve. With the strategy, the gate current and operation voltage increased and decreased, respectively.

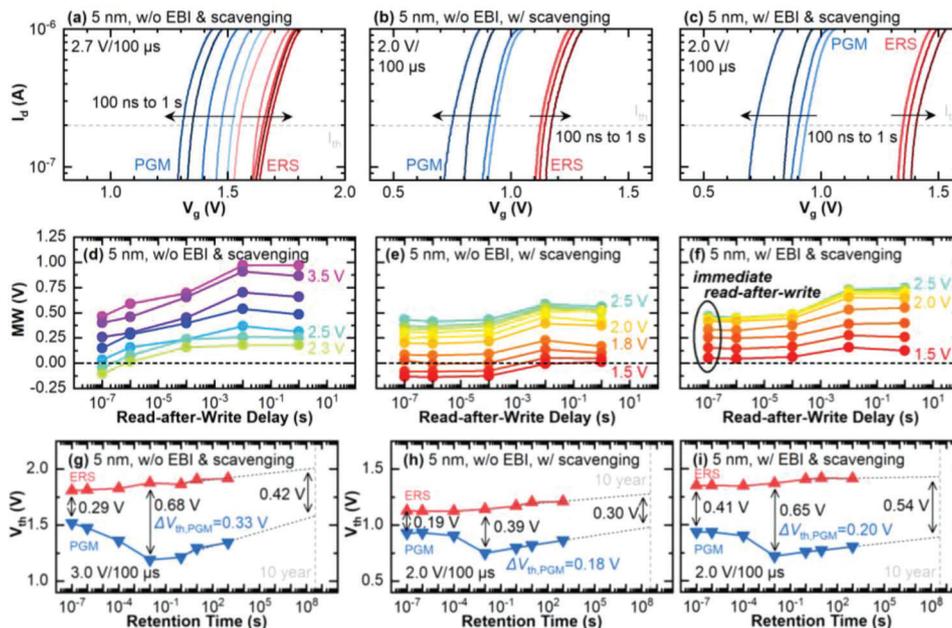
to the  $V_g$  sweep, which confirms that the operating voltage significantly decreases with HZO thickness scaling and IL scavenging. For example, HZO of 10 nm without EBI and without scavenging exhibited clockwise hysteresis at  $V_g$  sweep of 3.5 V, indicating charge trapping was dominant over ferroelectricity, but HZO of 10 nm without EBI and with scavenging and HZO of 5 nm with EBI and with scavenging exhibited ferroelectric counterclockwise hysteresis even at  $V_g$  sweep of 2.6 and 2.0 V, respectively. The reduction of operating voltage was confirmed according to our strategies in the DC transfer curve, but it was also highlighted by the pulse measurement of the positive-up-negative-down (PUND) method in the MFIS structures (Figure S3, Supporting Information). The  $V_{sw}$  decreased from 3.87 V for HZO of 10 nm without EBI and without scavenging to 2.37 V for HZO of 5 nm with EBI and with scavenging. According to the strategies,  $V_{sw}$  was finally reduced by 39%. IL scavenging greatly reduced  $V_{sw}$ , and HZO scaling and EBI treatment further reduced  $V_{sw}$ . Additionally, since  $V_{sw}$  decreased as the HZO thickness decreased from 10 to 5 nm, the maximum MW proportional to  $V_{sw}$  also decreased, but the  $V_g$  to achieve the same MW decreased and the minimum operating voltage also decreased. In addition, in Figure 5a, the minimum value of subthreshold swing (SS) for HZO of 10 nm without EBI and without scavenging, HZO of 10 nm without EBI and with scavenging, and HZO of 5 nm with EBI and with scavenging were 350, 250, and 123 mV  $\text{dec}^{-1}$ , respectively, indicating the improvement in interface quality due to our three strategies. IL scavenging, which decomposes IL, also decreased SS by reducing oxygen vacancy at the bottom interface<sup>[21]</sup> and interface trap density<sup>[26]</sup> as previously reported. Meanwhile, the high gate current in the off-state is considered to be caused by the gate-induced drain leakage from the gate-drain overlap structure.

In order to investigate the ferroelectricity of the FeFETs according to our strategies in more detail, it was analyzed based on the pulse scheme in Figure S2 (Supporting Information). Figure 6 shows the pulsed  $I_d$ - $V_g$  curves and MW obtained by performing the write (program and erase) operation and reading after the retention time as shown in Figure S2a (Supporting Information). The read-after-write delay was also examined by measuring the pulsed  $I_d$ - $V_g$  curves while waiting for the retention time of at least 100 ns. Figure 6a-c shows pulsed  $I_d$ - $V_g$  curves of FeFETs with HZO of 5 nm without EBI and without scavenging, with HZO of 5 nm without EBI and with scavenging, and with HZO of 5 nm with EBI and with scavenging. For FeFETs with HZO

without scavenging and with HZO with scavenging, write pulses of  $\pm 2.7$  V/100  $\mu\text{s}$  and  $\pm 2.0$  V/100  $\mu\text{s}$  were applied, respectively. As shown in Figure 6a, MW after 100 ns of write operation was very small,  $\approx 0.03$  V, for FeFETs with HZO of 5 nm without EBI and without scavenging. The MW gradually increased according to the retention time and became 0.31 V at 1 s after the write operation, which means that the trapped charges are de-trapped over time. In Figure 6b,c, the MW of FeFETs with scavenging also gradually increased with time, however, the change was smaller compared to FeFETs without scavenging. Above all, FeFETs with scavenging exhibited higher MW than FeFETs without scavenging even at lower write pulse amplitude.

The tendency of scavenging to lower the write pulse amplitude is clearly shown by the MW according to the write pulse amplitude in Figure 6d-f. Write pulses of  $\pm 2.3$  to  $\pm 3.5$  V were applied to FeFETs without scavenging, while write pulses of  $\pm 1.5$  to  $\pm 2.5$  V were applied to FeFETs with scavenging. Figure 6d shows that FeFETs with HZO without EBI and without scavenging can perform a read operation with a read-after-write delay of 100 ns at a write pulse amplitude of  $\pm 2.9$  V or higher. On the other hand, FeFETs with HZO without EBI and with scavenging and with HZO with EBI and with scavenging were capable of read operation with a read-after-write delay of 100 ns at  $\pm 1.8$  and  $\pm 1.5$  V, respectively (Figure 6e,f). All FeFETs exhibited the maximum MW at the retention time of 10 ms to 1 s in common. The maximum MW of FeFETs with HZO without EBI and without scavenging was 0.54 V at the write pulse of  $\pm 2.9$  V/100  $\mu\text{s}$ . However, with scavenging, the maximum MW was 0.55 V at the write pulse of  $\pm 2.3$  V/100  $\mu\text{s}$ . Finally, with EBI and with scavenging, the write pulse to obtain the maximum MW of 0.53 V was reduced to  $\pm 1.8$  V/100  $\mu\text{s}$ . In other words, FeFETs with EBI and with scavenging enabled read-after-write operation with only a delay of 100 ns even with write pulses of  $\pm 1.5$  V, and required lower write pulses to achieve the same MW as other devices.

Figure 6g-i shows long-term retention characteristics with 10-year extrapolation. For FeFETs without scavenging, write pulses of  $\pm 3.0$  V/100  $\mu\text{s}$  were applied while write pulses of  $\pm 2.0$  V/100  $\mu\text{s}$  were applied for FeFETs with scavenging. From the retention time of 100 ns to 10 ms, retention instability was evaluated while comparing the  $V_{th}$  change after program operation ( $\Delta V_{th, PGM}$ ) since charge trapping usually occurs by positive program pulses due to the defect level originating from oxygen vacancy as in the case with our devices and typical HZO-based FeFETs.<sup>[13,24]</sup> Evaluating the  $\Delta V_{th, PGM}$  accordingly, the  $\Delta V_{th, PGM}$  values of FeFETs with HZO without EBI and without scavenging, with HZO without EBI and with scavenging, with HZO with EBI and with scavenging were 0.33, 0.18, and 0.20 V, respectively. In addition, retention loss was assessed by comparing the MW at the retention time of 10-year extrapolation to the maximum MW. For FeFETs with HZO without EBI and without scavenging, maximum MW and MW at the retention time of 10-year extrapolation were 0.68 and 0.42 V, respectively, which is a retention loss of 38%. On the other hand, the retention loss of FeFETs with HZO without EBI and with scavenging and with HZO with EBI and with scavenging were 23% and 17%, respectively, lower than that of FeFETs with HZO without EBI and without scavenging. These results suggest that scavenging and EBI are very effective in alleviating retention instability and retention loss.

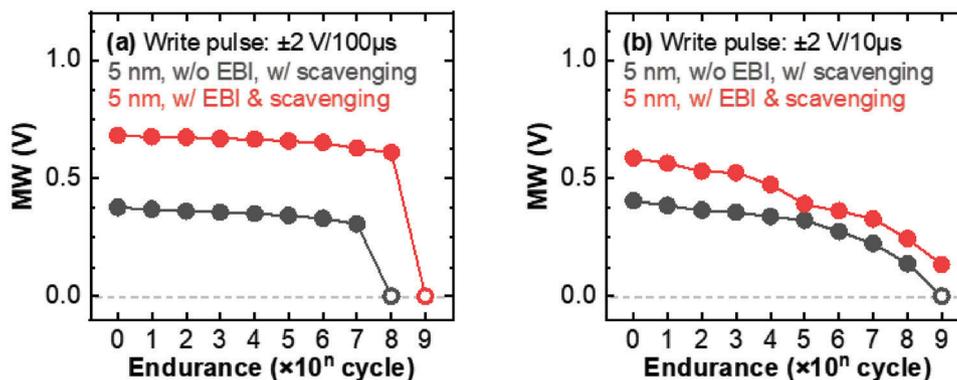


**Figure 6.** Time evolution of a–c) pulsed  $I$ - $V$  curves, d–f) MW (pulse width = 100  $\mu$ s), and g–i)  $V_{th}$  after write operations ( $V_d = 0.1$  V). FeFETs of 5-nm HZO with EBI and scavenging were capable of immediate read-after-write (100 ns) even with a 1.5 V write pulse.

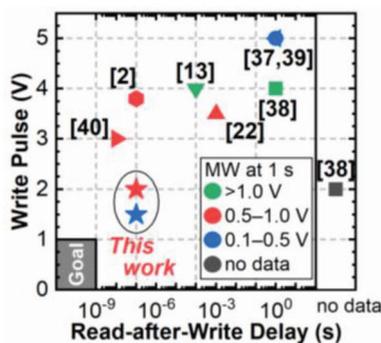
The excellent retention characteristics of the FeFETs with scavenging are attributed to the reduced charge trapping and depolarization field due to the reduced IL thickness. With EBI, retention loss was further reduced. Interfacial trap density estimated from  $\Delta V_{th, PGM}$  according to the retention time was similarly lower in FeFETs with HZO without EBI and with scavenging and with HZO with EBI and with scavenging than in FeFETs with HZO without EBI and without scavenging, but bulk trap density derived from slow double-pulsed  $I$ - $V$  (DPiV) measurement (Figure S2b, Supporting Information) was lower in FeFETs with HZO with EBI and with scavenging than in FeFETs with HZO without EBI and with scavenging. The  $V_{th}$  hysteresis measured by DPiV decreased by 43% from 0.28 V for FeFETs with HZO without EBI and with scavenging to 0.16 V for FeFETs with HZO with EBI and with scavenging (Figure S4, Supporting Information), implying that the sub-oxide generated by EBI penetrating

from the top surface reduced the bulk trap density in the subsequent PMA process. Due to trap reduction by EBI, the FeFETs with EBI and scavenging showed superior endurance characteristics compared to the FeFETs without EBI and with scavenging (Figure 7). At the write pulse of  $\pm 2$  V/100  $\mu$ s, the FeFETs with EBI and scavenging showed breakdown at  $10^9$  cycles, which was improved than the FeFETs without EBI and with scavenging in which breakdown occurs at  $10^8$  cycles (Figure 7a). Moreover, at the write pulse of  $\pm 2$  V/10  $\mu$ s, no breakdown occurred until  $10^9$  cycles in the FeFETs with EBI and scavenging, while the breakdown occurred at  $10^9$  cycles in the FeFETs without EBI and with scavenging (Figure 7b).

Finally, the benchmark<sup>[2,13,23,38–41]</sup> in Figure 8 highlights the low-voltage and fast read-after-write operation of our FeFETs with HZO thickness scaling, EBI treatment, and IL scavenging. The FeFETs with HZO with EBI and with scavenging showed the MW



**Figure 7.** Endurance characteristics of fabricated FeFETs. FeFET with HZO (5 nm) with EBI and scavenging exhibited endurance of  $10^8$  cycles and  $>10^9$  cycles at the write pulse of a)  $\pm 2$  V/100  $\mu$ s and b)  $\pm 2$  V/10  $\mu$ s, respectively.



**Figure 8.** Benchmark according to write pulse, read-after-write delay, and MW in Si n-FeFETs. It demonstrates the superiority of the device fabricated in this work and the potential of the strategies used.

of 0.65 V at a read-after-write delay of 100 ns when a write voltage of 2 V was applied. Even at a write voltage of 1.5 V, it showed a MW of 0.12 V. This result shows that these engineering strategies are very effective and have great potential for improving the performance of FeFETs, evident by the record-performance matrix in Figure 8. More detailed benchmarks related to write and read operations are shown in Table S1 (Supporting Information).

### 3. Conclusion

We have systematically investigated the strategies of HZO thickness scaling, EBI treatment, and IL scavenging to improve the performance of FeFETs. The thickness reduction of HZO and IL was manifested by TEM cross-section analysis. The generation of oxygen vacancy and ferroelectric orthorhombic phase-oriented crystallization by EBI treatment was confirmed by XRD and XPS analysis. As a result, the reduction of ferroelectric switching voltage and operating voltage of FeFET with the three strategies was demonstrated by PUND measurement and transfer curves. Finally, our FeFET with the strategies was capable of immediate read-after-write operation (100 ns) at the low operating voltage (1.5 V) with the endurance characteristic exceeding  $10^8$  cycles and 10-year retention characteristics with extrapolation. The excellent performance of our FeFET shows that the strategies of HZO thickness scaling, EBI treatment, and IL scavenging have great potential for low-power and fast-read FeFET.

### 4. Experimental Section

**Fabrication:** A fabrication flow and structure of FeFETs to investigate the improvement of device performance by EBI treatment and oxygen scavenging are illustrated in Figure S1 (Supporting Information). The FeFETs were fabricated by the gate last process, and the S/D regions were formed first by implantation and activation annealing. Then, native oxide ( $\text{SiO}_x$ ) on Si substrates was removed by buffered oxide etchant prior to HZO thin film deposition. The HZO films with a thickness of 5, 7, and 10 nm were deposited using an ozone oxidant at 270 °C by ALD. Tetrakis (ethylmethylamino) hafnium and tetrakis (ethylmethylamino) zirconium were used as precursors. Next, EBI treatment was carried out for 1 min on the as-deposited HZO films. An electron beam source with a diameter of 60 mm discharged the mixed  $\text{Ar}/\text{O}_2$  plasma and accelerated the electrons to the HZO films. The accelerating voltage was 100 V. On the pristine HZO film (without EBI) and the EBI-treated HZO film (with EBI), gate metal stacks

of Au (80 nm)/TiN (20 nm) and Au (80 nm)/Ti (20 nm)/TiN (20 nm) were formed for gate stacks without scavenging and with scavenging. Crystallization of HZO film and oxygen scavenging by Ti was induced by PMA at 500 °C for 1 min. Finally, Si-doped Al was deposited as the S/D electrodes followed by PMA at 300 °C for 5 min.

**Material Characterization:** TEM (JEOL, JEM-2100F) was used to obtain cross-sectional images of gate stacks. The phase and chemical bonding state of the HZO films were analyzed by GIXRD (Rigaku, SmartLab) and XPS (ThermoFisher Scientific, K-Alpha+). In the XPS analysis, the charge-up effect was compensated by calibrating the whole spectra based on the peak of C 1s at 284.5 eV.

**Electrical Characterization:** The electrical characteristics of the fabricated FeFETs were investigated by a parameter analyzer (Keithley, 4200A-SCS) with a pulse measurement unit (Keithley, 4225-PMU) and remote preamplifier/switch modules (Keithley, 42250RPM). The pulse scheme used for device characterization is shown in Figure S2 (Supporting Information). In order to evaluate the read-after-write delay, the retention time from the write operation (program and erase) to the read operation was given. The interfacial trap density could also be evaluated from the  $V_{th}$  shift according to the retention time. DPIV measurement was conducted to evaluate the bulk trap density of the fabricated HZO films.

### Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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### Conflict of Interest

The authors declare no conflict of interest.

### Data Availability Statement

Research data are not shared.

### Keywords

electron-beam-irradiation, fast read, ferroelectric field-effect transistor,  $\text{HfZrO}_x$ , interfacial layer scavenging, low operating voltage, thickness scaling

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