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Enhancing Electrical and Interfacial Properties of BeO/4H-SiC Structures with SiO_2 Interlayer

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Beryllium oxide (BeO) has exceptionally high thermal conductivity (330 W m^{-1}·K^{-1}), a large bandgap energy, and a high dielectric constant, making it an optimal dielectric for high-power devices. However, its direct application on 4H-SiC is hindered by interfacial carbon-cluster formation during high-temperature annealing, primarily due to the decomposition of 4H-SiC. In this study, a SiO_2 interlayer is introduced between BeO and 4H-SiC using plasma-enhanced chemical-vapor deposition to address these challenges. Electrical measurements reveal that the BeO/SiO_2/4H-SiC stack exhibits a reduced leakage-current density, an enhanced breakdown field (>7.5 MV cm^{-1}), and a smaller capacitance–voltage hysteresis compared with direct BeO deposition owing to reduced interface defects. Band-alignment analysis shows an increased conduction-band offset between BeO/4H-SiC, potentially contributing to improved carrier confinement. The interface trap density (Dit) is reduced by two orders of magnitude, indicating an improved interface quality owing to the presence of the SiO_2 interlayer. The SiO_2 interlayer significantly improves interface quality, reduces leakage current, and enhances the breakdown field of the BeO/4H-SiC system. These results suggest that interfacial engineering using a SiO_2 interlayer can be an effective approach for improving the electrical reliability of high-temperature dielectric stacks on 4H-SiC.

1. Introduction

The pursuit of high-performance power electronics has driven significant interest in wide-bandgap semiconductors, with 4H-SiC receiving considerable attention because of its exceptional material properties. 4H-SiC offers exceptional thermal conductivity (370 W m^{-1}·K^{-1}),[1] high breakdown-field strength (3 MV cm^{-1}),[2] high electron mobility (2×10^7 cm s^{-1}), and low intrinsic carrier concentration (8×10^{-9} cm^{-3}),[3] making it an ideal candidate for power-device applications. Thermally oxidized SiO_2 has been widely adopted as a gate dielectric for 4H-SiC MOSFETs due to its excellent thermodynamic stability, wide bandgap (≈9 eV), mature fabrication process compatibility, and chemical inertness at high temperatures.[4] Furthermore, it offers superior interface passivation and a high conduction band offset (≈3.2 eV), which are critical for device reliability. Nevertheless, when directly grown on 4H-SiC by thermal oxidation, SiO_2 suffers from a high interface trap density (Dit ≈10^{13} $cm^{-2}eV^{-1}$), primarily due to residual carbon atoms generated during the incomplete oxidation of SiC.[5] This interface degradation significantly limits channel mobility and device performance.

Furthermore, the smaller permittivity of SiO_2 (3.9) compared with 4H-SiC (9.6) results in the SiO_2 electric field being 2.5 times higher than that in 4H-SiC.[6] This forces 4H-SiC MOSFETs to operate at electric fields far below the breakdown capability of 4H-SiC to prevent the breakdown of SiO_2. In addition, its limitations in thermal conductivity and dielectric constant hinder device performance in high-power applications. To address these limitations and fully exploit the potential of 4H-SiC in power applications, the development of high-k materials has emerged as a promising approach for enhancing 4H-SiC power-device performance and reliability (**Figure 1**).[7]

Compared with conventional high-k materials such as Al_2O_3 and HfO_2, Beryllium oxide (BeO) exhibits outstanding properties that make it a promising high-k dielectric material for 4H-SiC-based power devices. BeO has superior electrical insulating properties, a large band gap of 10.6 eV,[8] crystalline growth,[9] and a high dielectric constant of 6.9.[10] Additionally, BeO stands out among high-k oxides due to its exceptionally high thermal

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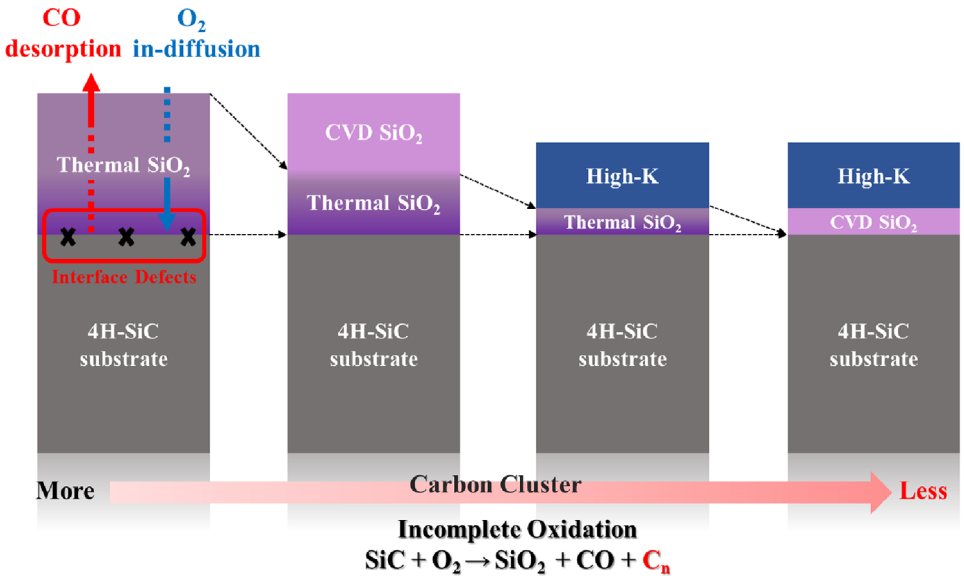

Figure 1. Schematic of interface-defect formation during the incomplete thermal oxidation of 4H-SiC. High-k dielectrics can reduce carbon generation by reducing the reliance on thermally oxidized SiO_2.

conductivity of 330 W m^{-1}·K^{-1}[11] at 300 K. This thermal advantage, attributed to its strong Be–O bonding and limited soft phonon modes,[12] is critical for power devices operating under elevated temperatures, where effective heat dissipation is essential. Furthermore, the strong covalent bonding between Be and O atoms contributes to enhanced thermal stability during high-temperature processing. Another critical advantage is the high conduction band offset (CBO) of 2.28 eV[12] between BeO and 4H-SiC, which is substantially larger than those of Al_2O_3[13] or HfO_2[14] (typically ≈1.5 eV or less). A higher CBO ensures better carrier confinement and leakage suppression under high electric fields, a key requirement for reliable power device operation.

Table 1 presents a comparison of key physical properties among representative high-k dielectrics. BeO offers a large bandgap, high thermal conductivity, and wide conduction band offset(CBO) with SiC, making it particularly promising for wide-bandgap semiconductors, which are designed for high-voltage and high-temperature environments.

However, the integration of BeO with 4H-SiC presents interfacial challenges, particularly under high-temperature processing conditions required for device fabrication and reliable ohmic contact formation. Previous studies, have shown that direct deposition of BeO on 4H-SiC can lead to increased C—C bonding and carbon-cluster formation at the interface after annealing, resulting in degraded electrical properties.[15] To mitigate interfacial defects such as poor chemical bonding and carbon-related residues arising during high-temperature annealing, a thermally stable PECVD SiO_2 interlayer was introduced between BeO and 4H-SiC. Rather than serving as a conventional gate dielectric, this interlayer acts as a chemical buffer, transforming the BeO/SiC interface into a passivated SiO_2/SiC interface that is known to suppress interface trap densities of High-K/4H-SiC interfaces and enhance thermal and chemical stability during annealing.[12,15] While thermally grown SiO_2 is typically preferred for its superior electrical properties,[16–18] PECVD-deposited SiO_2 has also been employed effectively as an interfacial layer in various high-κ/4H-SiC MOS structures, with demonstrated performance in terms of leakage current and interface trap density.[19–21]

Table 1. Comparison of representative high-k dielectric materials for 4H-SiC power devices.

Property	BeO[12]	Al_2O_3[13]	HfO_2[14]
Thermal Conductivity (W/m·K)	330	30	1.5
Bandgap (eV)	10.6	8.8	5.7
Dielectric Constant (k)	6.9	9	25
Conduction Band Offset with 4H-SiC (eV)	2.28	1.9	0.7
Crystallinity	Crystalline	Amorphous	Amorphous

Building upon this prior work, we investigated the effect of introducing a thin SiO_2 interlayer between BeO and 4H-SiC. Previous research has demonstrated that thermally oxidized or PECVD SiO_2 interlayers can effectively suppress carbon-related defect formation and improve interface quality in SiC-based devices.[22–26] The SiO_2 interlayer in this study is expected to serve as a buffer layer, mitigating carbon-related defects during high-temperature annealing while providing a higher conduction-band offset (CBO). This improvement can potentially reduce the interface trap density and improve the overall dielectric reliability.

In this study, we employed atomic-layer deposition (ALD) techniques to fabricate high-quality BeO films on 4H-SiC substrates with a 10-nm SiO_2 interlayer deposited via plasma-enhanced chemical-vapor deposition (PECVD). The structural and electrical properties of the BeO/SiO_2/4H-SiC stack were systematically investigated and compared with those of the BeO/4H-SiC to evaluate its effectiveness in suppressing interfacial defects. To address high-temperature stability, we also explored the electrical and chemical behavior of BeO/SiO_2/4H-SiC and BeO/SiO_2 stacks before and after post-deposition annealing.

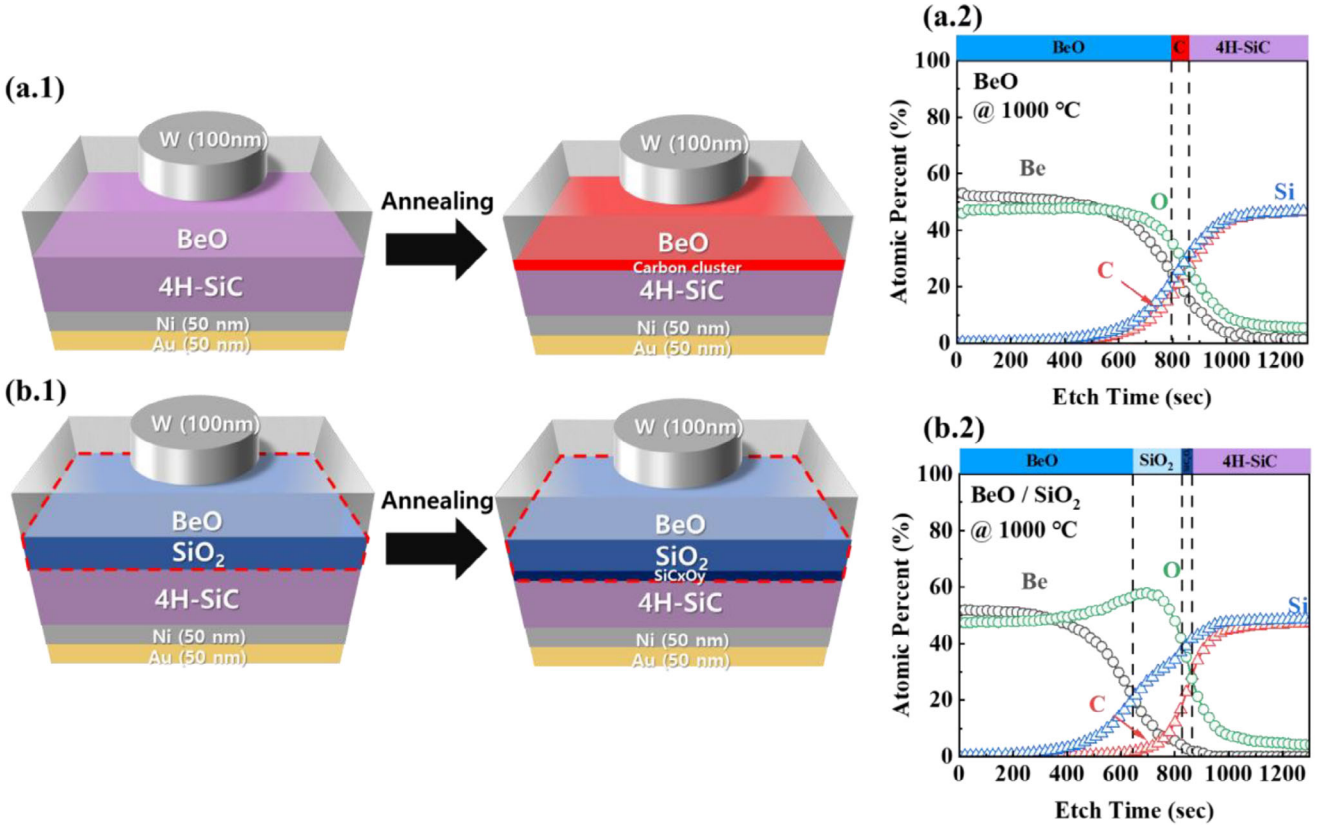

Figure 2. Schematic comparing carbon formation during annealing for two different substrates: a.1) BeO/4H-SiC and b.1) BeO/SiO_2/4H-SiC. XPS-depth profile of atomic concentration of carbon with a.2) BeO/4H-SiC and b.2) BeO/SiO_2/4H-SiC.

Comprehensive material-characterization techniques, including X-ray diffraction (XRD), X-ray reflectometry (XRR), X-ray photoelectron spectroscopy (XPS), and electrical measurements, were utilized to analyze the quality of the deposited films and evaluate the effectiveness of the SiO_2 interlayer. Our findings demonstrate that the SiO_2 interlayer significantly improves the dielectric performance of BeO by reducing the interface trap density, decreasing the leakage current, and enhancing the breakdown voltage. This study contributes to the advancement of high-performance power devices by optimizing the dielectric interface in 4H-SiC based structures, thereby extending the application range of BeO in high-temperature and high-voltage power-device technologies.

2. Results and Discussion

Figure 2 presents a schematic of the structural difference and interfacial changes of the BeO/4H-SiC and BeO/SiO_2/4H-SiC stacks after annealing, along with the corresponding XPS-depth profiles. The schematic in Figure 2(a.1) represents the BeO/4H-SiC structure, where annealing leads to significant carbon segregation at the interface. Owing to the limited oxygen supply from BeO, 4H-SiC is not completely oxidized, causing the carbon atoms to separate from the Si atoms. While Si may form Si-rich compounds, carbon atoms cluster near the interface, resulting in electrically active defects that degrade the dielectric properties of the stack. The absence of an intermediate layer allows these carbon atoms to accumulate without suppression or further reactions, as evidenced by the XPS profile in Figure 2(a.2). The profile shows that the carbon concentration remains high near the interface, with ≈8 atomic percent (at.%) detected at a depth corresponding to 5 nm from the interface. The carbon concentration gradually decreases, which further indicates diffusion into adjacent layers.

In contrast, Figure 2(b.1) depicts the BeO/SiO_2/4H-SiC structure, where a SiO_2 interlayer is introduced between BeO and 4H-SiC. The SiO_2 interlayer provides an additional oxygen source that actively participates in interfacial reactions during annealing. Oxygen released from the SiO_2 interlayer reacts with carbon byproducts from the decomposition of 4H-SiC, leading to the formation of a thin, passivated SiO_2/SiC_xO_y layer.[24] This suppresses carbon segregation and prevents excessive carbon cluster formation, as shown in Figure 2(a.2). The effectiveness of the SiO_2 interlayer is confirmed by the XPS depth profile shown in Figure 2(b.2), where carbon concentration decreases sharply near the interface, with values below 2 at.% at a depth of 5 nm from the interface. The steeper gradient demonstrates that SiO_2 effectively mitigates carbon accumulation and limits its diffusion into adjacent layers, thereby improving interfacial properties.

Figure 3 shows the XPS C1s carbon-peak deconvolution data measured at a depth of 2 nm from the 4H-SiC substrate. This analysis aims to investigate the chemical-bonding states of carbon at the interface between the dielectric layer and 4H-SiC substrate by comparing the (a) BeO/4H-SiC and (b)

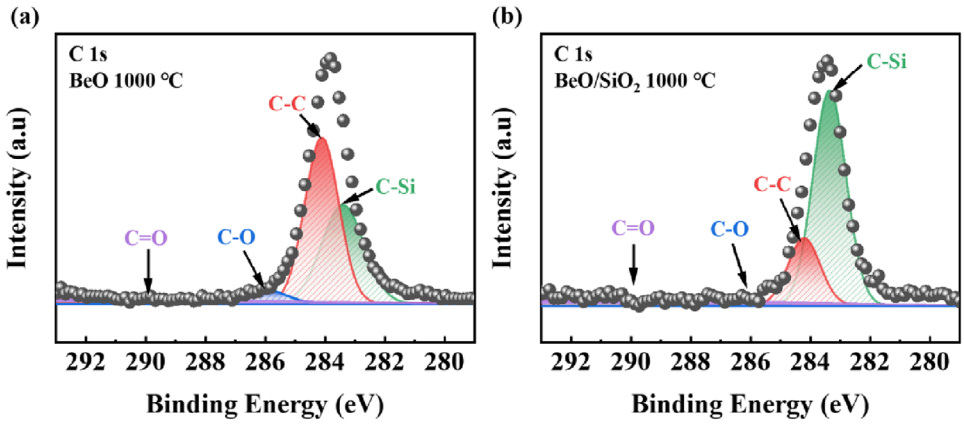

Figure 3. XPS C1s carbon peak deconvolution with a) BeO/4H-SiC and b) BeO/SiO_2/4H-SiC after annealing at 1000 °C.

BeO/SiO_2/4H-SiC structures. The C1s spectra were deconvoluted into different peaks corresponding to various carbon-bonding configurations, including the C—Si (283.0 eV), C—C (284.8 eV), C—O (286.0 eV), and C═O (290.0 eV) bonds.[27,28]

The C—Si bonds originated from the 4H-SiC substrate. During annealing, the 4H-SiC substrate underwent decomposition, leading to the formation of C—C bonds owing to incomplete oxidation.[29] Specifically, the C1s spectrum of the BeO/SiO_2/4H-SiC structure shows a lower intensity of the C—C peak and a higher intensity of the C—Si peak compared to that of the BeO/4H-SiC structure. The lower carbon percentage observed in the SiO_2 sample further supports this conclusion, suggesting that the SiO_2 interlayer effectively mitigates the accumulation of carbon defects. This is because beryllium oxide exhibits strong covalent bonding[30] between the beryllium and oxygen atoms, which hinders the decomposition of BeO and its reaction with carbon during annealing. Consequently, carbon atoms that are not bonded to silicon tend to remain as C—C clusters at the interface when BeO is directly deposited on 4H-SiC. In contrast, the SiO_2 interlayer provides a blocking barrier for the diffusion of carbon atoms from 4H-SiC to BeO.

Figure 4 presents the interface trap-density (D_{it}) distribution as a function of energy within the bandgap (E_c-E_t) for both the BeO/4H-SiC and BeO/SiO_2/4H-SiC structures after annealing at 1000 °C. D_{it} was calculated using the Terman method by comparing the differences between the ideal C–V curves and measured C–V curves at 1 MHZ.[15,31] The D_{it} value for the BeO/SiO_2/4H-SiC structure is approximately mid-10^{11} cm^{-2} eV^{-1} at E_c-E_t = 0.25 eV, which is two orders of magnitude lower than that of direct BeO deposition on 4H-SiC (mid-10^{13} cm^{-2} eV^{-1} at E_c-E_t = 0.25 eV). Although the Terman method provides a practical estimation of D_{it} based on high-frequency C–V measurements, it may underestimate the absolute D_{it} values due to its insensitivity to fast interface states and inaccuracies near the conduction band edge. Alternative techniques, such as the C–ψ_s method[32] and carrier-based analysis using Hall and split C–V measurements,[33] offer more accurate evaluation of interface trap densities. Nevertheless, the relative comparison between the structures remains valid and clearly demonstrates interfacial improvement achieved by incorporating the SiO_2 interlayer. Although the measured D_{it} values did not reach the lowest levels reported in previous studies using more advanced passivation techniques,[34–36] they may be further reduced by implementing optimized surface treatment processes, such as pre-oxidation H_2 etching,[37] NO annealing,[38] $POCl_3$ annealing,[39] or PEALD SiO_2,[40] all of which have been reported to effectively passivate interface states at the SiO_2/SiC interface.

The observed reduction in D_{it} is primarily attributed to the distinct chemical interactions between the dielectric layers and the 4H-SiC substrate. Specifically, the PECVD-deposited SiO_2 interlayer provides an available oxygen source that promotes further thermal oxidation of the 4H-SiC surface during high-temperature processing, resulting in the formation of a high-quality SiO_2 interface layer.[29,41] In contrast, when BeO is directly deposited on 4H-SiC, the strong covalent bonding between Be and O atoms prevents oxygen diffusion from the BeO layer to the underlying 4H-SiC.[42] As a result, interface formation relies mainly on ambient oxygen, which may be insufficient to ensure complete interfacial stability, leading to carbon-related byproducts and a higher D_{it}.

Figure 5 shows the XRR analysis of BeO/SiO_2/4H–SiC, which reveals the structural characteristics of the BeO films deposited

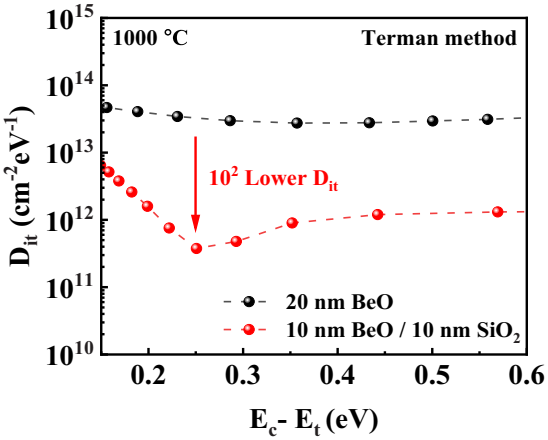

Figure 4. Interface defect (D_{it}) versus E_c–E_t of BeO/4H-SiC and BeO/SiO_2/4H-SiC after annealing at 1000 °C.

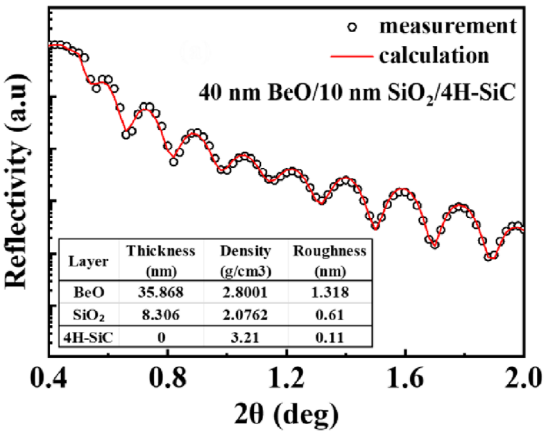

Figure 5. XRR analysis of the BeO/SiO_2/4H-SiC stack, confirming high-density BeO formation with a smooth interface.

on the SiO_2/4H-SiC substrates. The film thickness and density of as-grown BeO and SiO_2 layers were measured to be 35.8 and 8.3 nm, respectively, compared to their nominal thicknesses of 40 and 10 nm. The measured thickness values are in good agreement with the ellipsometry results and expected ALD growth rate of 0.9 Å/cycle, confirming precise thickness control. The density of ALD BeO (2.80 g cm^{-3}) was comparable to that of bulk BeO (3.01 g cm^{-3}) and previous research.[43]

The XRR fringe patterns provided insights into the interface roughness between the BeO and SiO_2 layers. The well-defined interference fringes in the XRR spectra indicate relatively smooth interfaces, which are crucial for maintaining the good electrical properties of the dielectric stack.[44] The low interface roughness of ≈0.6 nm at the SiO_2/4H-SiC interface suggests a highly uniform and smooth interface. Surface roughness scattering, which inversely scales with the square of the roughness ($\mu_{SR} \propto 1/\Delta^2$), is significantly suppressed compared to conventional thermally oxidized SiO_2/4H-SiC ($\Delta \approx 1.2 - 2.4\ nm$)[45] which enhances the electrical characteristics by minimizing interface scattering[46] and enhancing carrier mobility in the final device structure. Furthermore, the polycrystalline nature of BeO on SiO_2 was confirmed by TEM and SAED patterns in our previous study, supporting the structural integrity and densification observed in the XRR profiles.[47]

Figure 6a illustrates the band alignment between BeO and 4H-SiC characterized by XPS using the Kraut method. Among high-k dielectrics, BeO exhibits a high CBO of 2.34 eV, making it an effective gate dielectric material. Furthermore, SiO_2 demonstrated a higher CBO of 2.7 eV, suggesting its potential use as an interlayer to further suppress the leakage current and enhance device performance.[48] The significant band offsets provided by these materials contribute to improved carrier confinement and reliability in electronic applications.

The conduction- and valence-band offsets of the BeO films on 4H-SiC were calculated using the Kraut method.[49,50] While initial estimations of the valence-band offset (ΔE_v) relied on the difference between the valence-band maximum (VBM) values of BeO and 4H-SiC, this approach often led to inaccuracies owing to interface dipole effects. To address these limitations, the Kraut method was employed in this study, as it incorporates corrections for dipole shifts occurring at the interface before and after film deposition. This ensured a more accurate determination of the energy separation between the core levels and VBM values.

The ΔE_V, core-level energy difference (ΔE_{CL}), and ΔE_C were calculated using the following equations:

$$\Delta E_V = \left(E_{Si2p}^{4H-SiC} - E_{VBM}^{4H-SiC}\right) - \left(E_{Be1s}^{BeO} - E_{VBM}^{BeO}\right) - \Delta E_{CL} \quad (1)$$

$$\Delta E_{CL} = \left(E_{Si2p}^{4H-SiC} - E_{Be1s}^{BeO}\right) \quad (2)$$

$$\Delta E_C = \left(E_g^{BeO} - E_g^{4H-SiC}\right) - \Delta E_V. \quad (3)$$

In Equation (1), E_{Si2p} and E_{Be1s} represent the binding energies of core levels in 4H-SiC and BeO, respectively. Similarly, E_{VBM} corresponds to the binding energy of the valence-band maximum, whereas ΔE_{CL} represents the core-level difference between BeO and 4H-SiC. Each term, except for ΔE_{CL}, was derived from bulk-material standards and XPS data obtained from a bare 4H-SiC substrate and 40 nm BeO film on 4H-SiC. ΔE_{CL} was specifically determined from XPS measurements of a 5-nm BeO film on 4H-SiC.

Figure 6b shows the Si 2p core-level and valence band spectra of the bare 4H-SiC substrate. The VBM was determined by extrapolating the leading edge of the valence-band spectrum. The Si 2p peak and VBM of 4H-SiC were measured at 103.0 and 3.0 eV, respectively. Figure 6c illustrates the Be 1s core-level and valence band spectra of the 40-nm BeO film on 4H-SiC, where the Be 1s peak and VBM were observed at 113.3 and 3.5 eV, respectively. Figure 6d highlights the offset between the Si 2p and Be 1s core levels for the 5 nm BeO film on 4H-SiC. The Si 2p and Be 1s core-level binding energies were measured at 102.6 and 114.5 eV, respectively, resulting in a calculated ΔE_{CL} of 11.9 eV using Equation (2). The ΔE_V was determined to be 2.1 eV, with an estimated error margin of ±0.1 eV using Equations (1) and (2).

Figure 6e shows the O-Be1s core level used to determine the bandgap energy (Eg) of the BeO films deposited on a 4H-SiC substrate. The bandgap was calculated from the onset of inelastic energy loss relative to the elastic-peak binding energy. The onset of inelastic energy loss was measured by fitting the intersection of straight lines representing the inelastic loss spectra and the background level. From this analysis, the binding energy of the O-Be 1s elastic peak was observed at 531.4 eV, while the onset of inelastic energy loss was observed at 539.1 eV, yielding an estimated Eg of 7.7 eV.

By combining these results with Equation (3), ΔE_C was calculated as 2.34 eV, with an error margin of ±0.1 eV. Band-alignment results demonstrate that the BeO/4H-SiC interface forms a type I (straddling) heterojunction with significant valence-band offset ($\Delta E_V \approx 2.1$ eV), CBO ($\Delta E_C \approx 2.34$ eV), and a wide bandgap (Eg ≈ 7.7 eV), which is favorable for gate dielectric applications. The large conduction- and valence-band offsets provide effective barriers for both electrons and holes, minimizing carrier injection and improving device reliability.

Additionally, the incorporation of a SiO_2 interlayer increases the CBO by ≈+0.36 eV, resulting in a total CBO of 2.7 eV. This enhanced band offset effectively suppressed the leakage current by providing a higher energy barrier for carrier injection.

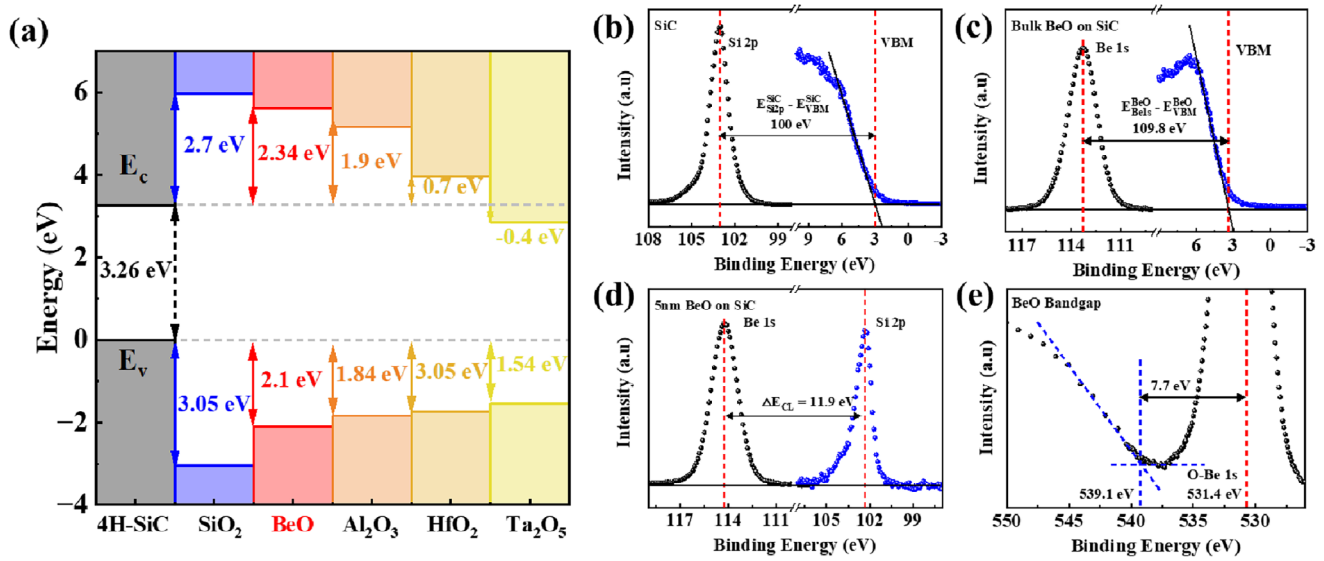

Figure 6. a) SiO_2[51] and high-k (BeO, Al_2O_3,[13] HfO_2,[14] Ta_2O_3[52]) band offset with respect to 4H-SiC. b) Si 2p core-level and VBM XPS spectra for bare 4H-SiC substrate. c) Be 1s core-level and VBM XPS spectra for 40 nm BeO film on 4H-SiC substrate. d) Si 2p and Be 1s core-level XPS spectra for 5 nm BeO on 4H-SiC substrate. e) O 1s energy-loss spectrum of 40 nm BeO on 4H-SiC substrate.

The I–V measurements in **Figure** 7a reveal that the leakage-current density for the 10 nm BeO/10 nm SiO_2 stack (J = 7.7 × 10^{-9} A cm^{-2}) is notably lower than that of 20 nm BeO (J = 1.5 × 10^{-8} A cm^{-2}) at an electric field of 1 MV cm^{-1}. Moreover, the breakdown field is significantly increased more than twice to 7.5 MV cm^{-1}. This reduced leakage current and increased breakdown field can be attributed to the increased CBO and improved interface quality provided by the SiO_2 interlayer. The enhanced conduction barrier effectively suppresses the leakage current through the dielectric stack, enhancing the overall dielectric strength.

As shown in Figure 7b, C–V was measured at 1 MHZ, where the voltage was swept bidirectionally from depletion to accumulation and back. The analysis shows that the 10 nm BeO/10 nm SiO_2 structure exhibits a smaller hysteresis of 0.05 V compared with the direct BeO deposition, indicating a reduction in trapped charges and improved interface stability. The effective dielectric constant (k) of the 10 nm BeO/10 nm SiO_2 stack is ≈5.3, which is close to the ideal value of 5.4 calculated from the combination of dielectric constants of BeO (6.9) and SiO_2 (3.9). In addition, the flat-band voltage (V_{FB}) shows a negative shift from 3.7 V (BeO/4H-SiC) to 1.9 V (BeO/SiO_2/4H-SiC) upon introduction of the SiO_2 interlayer. This leftward shift of the C–V curve is a commonly observed phenomenon in SiO_2/4H-SiC structures and is primarily attributed to the formation of interface dipoles and fixed oxide charges (Q_f) at the SiO_2/SiC interface. Additionally, the incorporation of the SiO_2 layer improves the interfacial quality by reducing Dit, which also contributes to the observed shift toward the ideal flat-band condition.[53]

The decrease in D_{it} reduces the energy states that can trap charges near the interface, thus lowering the effective positive charge near the conduction band edge. To estimate the magnitude of charge variation responsible for the VFB shift, we employ the relation:

$$\Delta V_{FB} = -\frac{Q_{eff}}{C_{OX}} \tag{4}$$

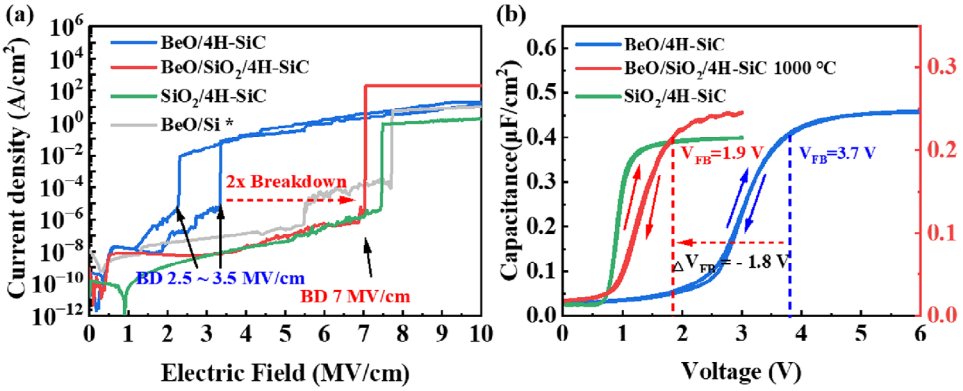

Figure 7. a) Current density–electric field and b) C–V characteristics of BeO/4H-SiC, BeO/SiO_2/4H-SiC, and SiO_2/4H-SiC structures.

where Cox is the equivalent oxide capacitance per unit area. For a 10 nm BeO / 10 nm SiO_2 stack with an effective dielectric constant of ≈5.3, Cox is ≈1.1 μF cm^{-2}, yielding an estimated charge reduction Q_{eff} of ≈2.0 × 10^{12} cm^{-2} corresponding to the 1.8 V shift. This value reflects the combined effects of reduced fixed charges and interface trap densities.

Therefore, the observed V_{FB} shift is likely the result of a combination of interface dipole formation by SiO_2, reduction of positive fixed oxide charge, and improved interface passivation leading to a lower D_{it}. These findings further support the role of the SiO_2 interlayer in modulating the interface charge environment and enhancing the electrical stability of the dielectric/4H-SiC.

In addition to the observed improvements in leakage current and breakdown characteristics, the introduction of BeO also plays a critical role in improving electric field distribution across the gate dielectric stack, which is particularly important for reliable operation under high bias conditions in 4H-SiC. Due to the relatively low dielectric constant of SiO_2 ($\kappa = 3.9$) compared to that of 4H-SiC ($\kappa = 9.7$), a significant portion of the applied voltage is dropped across the oxide layer, resulting in a high electric field concentration and premature dielectric breakdown. In contrast, BeO, with a higher dielectric constant ($\kappa = 6.9$), enables a reduced effective oxide thickness (EOT) for the same physical thickness, leading to more favorable electric field distribution and improved gate performance.

The effective oxide thickness (EOT) is calculated using the relation:

$$EOT = t_{\text{high-k}} \cdot \frac{k_{SiO_2}}{k_{\text{high-k}}} \tag{5}$$

For a physical thickness of 10 nm:

$$EOT_{SiO_2} = 10 \cdot \frac{3.9}{3.9} = 10\,\text{nm}, \quad EOT_{BeO} = 10 \cdot \frac{3.9}{6.9} \approx 5.65\,\text{nm} \tag{6}$$

whereas BeO with $k = 6.9$ yields an EOT of ≈5.65 nm.

This reduction in EOT directly translates to increased gate capacitance and lower electric field per unit thickness, which is essential for enhancing breakdown strength and suppressing leakage current. Furthermore, the use of a high-κ dielectric like BeO in a stacked configuration with SiO_2 can significantly alleviate electric field stress on the SiO_2 layer.

When SiO_2 is used alone, the entire applied voltage is dropped across the thin oxide:

$$E_{SiO_2} = \frac{V}{t_{SiO_2}} \tag{7}$$

For $V = 1\,\text{V}$, $t_{SiO_2} = 10\,\text{nm}$, this yields:

$$E_{SiO_2} = \frac{1}{10} = 1\,\text{MV/cm} \tag{8}$$

In contrast, for a 10 nm SiO_2 / 10 nm BeO gate stack, the voltage is divided according to the permittivity and thickness of each layer. The voltage drop across the SiO_2 interlayer is given by:

$$V_{SiO_2}^{\text{stack}} = \frac{t_{SiO_2}/\kappa_{SiO_2}}{t_{SiO_2}/\kappa_{SiO_2} + t_{BeO}/\kappa_{BeO}} \cdot V \tag{9}$$

Substituting $t_{SiO_2} = t_{BeO} = 10\,\text{nm}$, $\kappa_{SiO_2} = 3.9$, and $\kappa_{BeO} = 6.9$, we obtain:

$$V_{SiO_2}^{\text{stack}} = \frac{10/3.9}{10/3.9 + 10/6.9} \cdot 1 \approx \frac{2.564}{4.014} \cdot 1 \approx 0.639\,\text{V} \tag{10}$$

Hence, the electric field across the SiO_2 layer in the stack becomes:

$$E_{SiO_2}^{\text{stack}} = \frac{0.639}{10} = 0.639\,\text{MV/cm} \tag{11}$$

This represents approximately a 36% reduction in electric field stress on the SiO_2 layer. While the total physical thickness is increased, the inclusion of a high-κ dielectric such as BeO effectively maintains EOT scaling and distributes the electric field more favorably. As the thickness or dielectric strength of the BeO layer increases, the voltage drop across the SiO_2 is further suppressed. This redistribution of the electric field is a key advantage of BeO/SiO_2 stacked gate dielectrics, enabling enhanced breakdown performance and reduced leakage current.

Table 2 provides a comparative overview of key electrical parameters (E_{BD}, leakage current density, D_{it}) as reported for various dielectric configurations on 4H-SiC under similar post-deposition annealing conditions (≈1000 °C).

Thermally grown SiO_2 exhibits excellent breakdown characteristics (8–10 MV cm^{-1}) and moderate leakage current (≈10^{-7} A cm^{-2}), although typically at the cost of high interface trap densities (≈10^{13} cm^{-2} eV^{-1}). In contrast, ALD Al_2O_3 and Al_2O_3/SiO_2 stacks demonstrate improved Dit values (on the order of 10^{12} $cm^{-2}eV^{-1}$), though often at the expense of a lower breakdown field (≈3–5.5 MV cm^{-1}) and higher leakage current, particularly after high-temperature annealing.

In this context, the proposed BeO/SiO_2 bilayer structure achieves a balanced performance: following 1000 °C forming gas annealing, the stack exhibits a significantly reduced Dit (5 × 10^{11} $cm^{-2}eV^{-1}$), a leakage current density (≈5 × 10^{-7} A cm^{-2} at 5 MV cm^{-1}) comparable to thermal SiO_2, and an enhanced breakdown field of ≈7.5 MV cm^{-1}—exceeding prior BeO-only and Al_2O_3-based structures. These results highlight the effectiveness of the SiO_2 interlayer and demonstrate the clear advantages of our approach over existing gate dielectric technologies for 4H-SiC power devices

3. Conclusion

This study demonstrated that the incorporation of a PECVD-deposited SiO_2 interlayer significantly enhances the structural and electrical properties of BeO films on 4H-SiC substrates. The SiO_2 interlayer serves as an oxygen source during high-temperature annealing, promoting the formation of a high-quality SiO_2/SiCxOy interface while suppressing carbon-cluster formation, thereby overcoming interfacial limitations and expanding the applicability of BeO. This modification reduces the interface trap density by two orders of magnitude and improves thermal stability. The BeO/SiO_2/4H-SiC stack exhibits superior dielectric performance, owing to a reduced leakage current, enhanced breakdown field, and optimized band alignment, with high CBO. These improvements highlight the potential of this dual-layer dielectric

Table 2. Comparison of Electrical and Interfacial Properties of Gate Dielectrics on 4H-SiC under annealing temperature over 1000 °C.

Gate Stack [nm]	Annealing Condition	E_{BD} [MV cm^{-1}]	Leakage current [A cm^{-2}]	Dit [cm^{-2} eV^{-1}]
Dry Oxidation SiO_2[54]	O_2 / 1250°C	8–10	≈1 × 10^{-7}	≈1 × 10^{13}
Al_2O_3[55–57]	N_2 / RTA 1050 °C	5.5	1 × 10$^{-6–3}$	1 × 10^{12}
25 nm Al_2O_3/ 15 nm SiO_2[58]	N_2 / RTA 1000 °C	≈3.0	-, 2 × 10^{-7}[59]	6 × 10^{12}
20 nm BeO	Forming gas/ Tube Furnace, 1000 °C	≈3.5	1 × 10^{-6}	5 × 10^{13}
10 nm BeO/10 nm SiO_2	Forming gas/ Tube Furnace, 1000 °C	**≈7.5**	**≈5 × 10^{-7}**	**5 × 10^{11}**

structure for power devices fabricated under high-temperature processing conditions. In addition to the SiO_2 interlayer strategy demonstrated in this work, further improvements may be achieved through surface treatments and optimized ALD and annealing conditions, which can enhance interface quality and dielectric integrity. These approaches merit further study to fully utilize BeO-based dielectrics in high-voltage 4H-SiC MOSFETs.

4. Experimental Section

Sample Preparation: A commercially available highly doped n+ 4H-SiC (0001) wafer was used with epitaxially grown active layers with a thickness of 6.7 µm and an n-type doping concentration of 7.54 × 10^{15} cm^{-3}. Prior to further processing, the substrates were cleaned by sequential immersion in acetone, isopropanol (IPA), and deionized water for 5 min each. After these cleaning steps, the native oxide was removed by immersing the 4H-SiC substrates in a 6:1 buffered oxide etchant (BOE, NH_4 F: HF = 6:1) for 2 min. A 50 nm nickel layer was then deposited on the back of the 4H-SiC substrates using electron-beam evaporation. Ohmic contacts were formed by annealing the substrates in a nitrogen (N_2) atmosphere at 950 °C for 1 min using a rapid thermal-processing system. Before the deposition of the dielectric layers, the substrates were cleaned again with acetone, IPA, deionized water, and buffered oxide etchant (BOE, NH_4 F: HF = 6:1), for 5 min each.

For structural and compositional analyses, a 10 nm SiO_2 film was then deposited onto the 4H-SiC substrates using a PECVD system (SCS-5000, SN-tech, South Korea), utilizing N_2O and SiH_4 gases with a plasma power of 100 W for 300 s. Beryllium oxide (BeO) films were subsequently deposited on the SiO_2/4H-SiC substrates using an ALD system (Lucida M100-PL, NCD Technology) with diethylberyllium (DEB), specifically $Be(C_2H_5)_2$, serving as the precursor. H_2O was used as the reactant in the thermal ALD (ThALD) process. During ThALD, the substrate temperature was maintained at 250 °C, and the precursor temperature was set to 65 °C. The ALD process of BeO consisted of four sequential steps: DEB precursor exposure 5sec, purge 30sec, H_2O reactant exposure 1sec, purge 30sec. Argon gas was introduced to maintain a working pressure of 0.25 Torr and to purge any residual precursor and reactant from the chamber.

For the fabrication of metal-oxide-semiconductor capacitors, BeO films were deposited using ThALD with a growth per cycle of 0.9 Å/cycle onto two types of substrates: SiO_2/4H-SiC and bare 4H-SiC. To systematically investigate the effects of annealing on defect formation and electrical properties, the samples were divided into two groups: as-deposited samples, which did not undergo any thermal treatment, and post-deposition annealed samples, which were subjected to annealing in a tube furnace at 1000°C for 1 h under a forming gas atmosphere(95% N_2 + 5% H_2). A maskless patterning lithography process was used to fabricate a 250 µm-diameter hole pattern for the top-electrode deposition with a photo resist (AZ5214). Subsequently, a 100-nm-thick layer of tungsten was deposited using DC sputtering. The unwanted metal was removed through a lift-off process. Finally, a 100 nm thick gold (Au) layer was deposited on the backside via e-beam evaporation at a rate of 1 Å/sec to improve electrical conductivity.

Characterization: The thicknesses of the BeO thin films were evaluated using ellipsometry (Elli-SE, Ellipso Technology). The crystal structure and film density were investigated by XRD and XRR (SmartLab, Rigaku, Japan). These systems were equipped with an X-ray tube generating Cu Kα radiation, operated at voltages ranging from 20 to 60 kV and a current of 60 mA. XPS was performed using a spectrometer (K-ALPHA, Thermo Fisher Scientific, USA) to analyze the elemental composition and chemical states of the samples. A monochromated Al Kα X-rays with an energy of 1486.6 eV was used at 12 kV and 3 mA with a spot size of 400 µm. survey spectra were acquired at a pass energy of 200 eV (step size 1.0 eV), and detailed core-level spectra were acquired at a pass energy of 40 eV (step size 0.1 eV). The energy resolution, calibrated by the FWHM of the Ag 3d5/2 peak, was 0.7 eV. Prior to the XPS measurements, the sample surfaces were etched with Ar ions at 500 eV with a 2 mm x 2 mm raster to remove any surface contaminants, thereby ensuring an accurate analysis of the intrinsic composition of the BeO film. Both survey and depth-profile analyses were conducted at a take off angle(TOA) of 90°, thereby ensuring a bulk-sensitive analysis for accurate depth profiling. All binding energies were calibrated using the adventitious carbon C 1s peak at 284.8 eV as a reference. Capacitance-voltage (C–V) and current-voltage (I–V) measurements were performed using a power device analyzer/curve tracer (B1505A, Keysight, USA and 4200-SCS, Keithley, USA) equipped with a preamplifier. Finally, the interface trap density (Dit) was extracted from the C–V data using the Terman method, and calculations were performed using MATLAB software.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

atomic-layer deposition, band alignment, beryllium oxide, interface defect, silicon carbide

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