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Efficient thermo-optic phase shifters for photonic integrated circuits based on 500-nm-thick silicon on insulator

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Abstract: Integrated-optical thermo-optic phase shifters (TOPSes) are indispensable components for active light control in photonic integrated circuits (PICs). While mature on standard 220-nm silicon-on-insulator (SOI) platforms, new TOPS designs are required for emerging nonstandard SOI substrates, particularly those with 500 nm silicon and 1 μm buried oxide (BOX) layers, which are appropriate for III-V/silicon hybrid lasers. This paper presents what we believe to be a novel TOPS design specifically engineered for these substrates. Our design incorporates a rib waveguide with a deliberately tailored finite slab width, strategically mitigating the increased power consumption associated with these material specifications. This rib waveguide also ensures seamless, lossless integration with standard single-mode rib waveguides. Through systematic design, fabrication, and characterization, our TOPS achieved an average π phase shift power of 55.9 mW and a rapid response time of 7.09 μs. Comparative analysis against reference TOPSes revealed a remarkable 30% reduction in power consumption and ~42% reduced thermal crosstalk. These superior performance metrics establish our TOPS as a vital building block for advanced silicon PICs on these crucial nonstandard SOI platforms.

1. Introduction

Integrated-optical thermo-optic phase shifters (TOPSes) are indispensable components in modern photonic integrated circuits (PICs), enabling active control of light propagation through the thermal tuning of waveguide phase. Their versatility underpins a wide array of functionalities, from Mach-Zehnder modulators [1] and micro-ring modulators [2] to photonic switches [3], reconfigurable waveguide meshes [4], and optical phased arrays [5]. The mature field of silicon (Si) photonics, predominantly leveraging standard 220-nm-thick Si on insulator (SOI) platforms, has seen extensive development of TOPSes. These typically incorporate either metallic heaters positioned above waveguides or doped Si heaters integrated alongside waveguides [6,7]. Significant research efforts have been dedicated to minimizing the power consumption of these devices through various techniques, including the integration of deep trenches alongside waveguides [8], the suspension of waveguides via selective removal of the underlying buried oxide (BOX) [9], and the strategic utilization of folded, spiral, or multipass waveguide geometries to extend interaction lengths [10–12]. Consequently, the development of TOPSes on standard SOI platforms has reached a high level of sophistication, offering a diverse palette of solutions tailored to specific application requirements concerning response time and power consumption [13,14].

While standard SOI platforms continue to drive significant advancements, the landscape of Si photonics is rapidly expanding into novel application domains, necessitating the emergence of nonstandard SOI substrates. Prominent examples include mid-infrared PICs [15–17] and heterogeneously integrated lasers [18–20]. Operation in the mid-infrared spectrum mandates thicker Si waveguide layers to ensure robust fundamental mode guidance far from cutoff,

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exemplified by the use of SOI with a 400 nm Si layer for PICs at wavelengths around 3.8 μm [21]. High-performance III-V/Si hybrid lasers, which integrate III-V semiconductor films onto Si PICs, critically rely on highly efficient transitions between the waveguide mode in the active region of the laser, predominantly confined in the III-V semiconductor film, and the Si waveguide mode in the passive region. Given that III-V films in these devices are typically 2 μm thick, an optimal Si waveguide thickness of approximately 500 nm is required to facilitate this seamless coupling [22]. Employing standard SOI platforms for these hybrid lasers necessitates the use of complex mode converters. These devices require sophisticated fabrication processes to create tapers from thick III-V semiconductor films, which must be narrowed to less than 200 nm [23]. In contrast, SOI platforms with a 500 nm Si layer alleviate this fabrication challenge due to the higher effective indices of their Si waveguide modes. Furthermore, efficient thermal management in III-V/Si hybrid lasers often necessitates a thinned BOX layer to enhance heat dissipation into the SOI substrate. Consequently, SOI platforms featuring a 500 nm Si layer and a 1 μm BOX layer are becoming increasingly crucial for the realization of these advanced hybrid photonic systems. Despite the growing importance of SOIs with a 500 nm Si layer in these expanding application spaces, a systematic investigation into TOPSes specifically optimized for such nonstandard SOI platforms remains conspicuously absent in the literature.

This paper addresses this critical gap by presenting a comprehensive investigation into TOPSes specifically designed for SOI substrates with a 500 nm Si layer and a 1 μm BOX layer, a configuration directly compatible with III-V/Si hybrid lasers. The inherently thin BOX layer in these platforms presents a significant challenge: enhanced heat dissipation through the substrate, leading to increased power requirements for a π phase shift (P_π). To mitigate this, we propose and rigorously investigate a novel TOPS design, hereafter referred to as the type-1 TOPS. This design integrates a rib waveguide with a precisely defined finite slab width and a metal top heater whose dimensions are carefully optimized to comply with practical maximum voltage limitations. The choice of a rib waveguide facilitates direct and lossless coupling to standard single-mode rib (SMR) waveguides commonly employed on this specific SOI platform. We detail the design, fabrication, and comprehensive characterization of these type-1 TOPSes. Their performance metrics, including P_π, response time, and thermal crosstalk, are systematically compared against reference TOPSes (hereafter denoted as type-2 TOPSes) based on a conventional SMR waveguide, fabricated concurrently on the same chip. Our experimental results demonstrate that the type-1 TOPSes achieve an average P_π of 55.9 mW and a rapid response time of 7.09 μs. Notably, the type-1 TOPS exhibits a remarkable 30% reduction in power consumption compared to its type-2 counterpart. Furthermore, the thermal crosstalk for the type-1 TOPS is reduced by approximately 42% relative to the type-2 TOPS. These findings underscore the superior performance of the proposed type-1 TOPS, positioning it as an essential building block for advanced Si PICs on emerging SOI substrates featuring a 500 nm Si layer and a 1 μm BOX layer.

2. Design of proposed thermo-optic phase shifter

2.1. Device structure

To characterize the type-1 TOPSes, we utilized a symmetric Mach-Zehnder interferometer (MZI) with each arm incorporating a type-1 TOPS. Figure 1(a) illustrates the schematic of the MZI, which comprises input and output waveguides connected to focusing grating couplers (FGCs), 1×2 multimode interference (MMI) splitters, and S-bends. All MZI components are based on a standard SMR waveguide. The type-1 TOPSes are positioned between the S-bends.

Given the 500 nm Si layer thickness, the rib width and slab thickness of the SMR waveguide were optimized to 800 nm and 270 nm, respectively, to ensure single-mode operation. While the TOPS rib waveguide maintains these dimensions, its slab features a finite width (w_s). Due to fabrication processes, remnant Si regions exist on the chip, offset from the slab edges by a distance g, as depicted in Fig. 1(b). For the standard SMR waveguide, the distance between its

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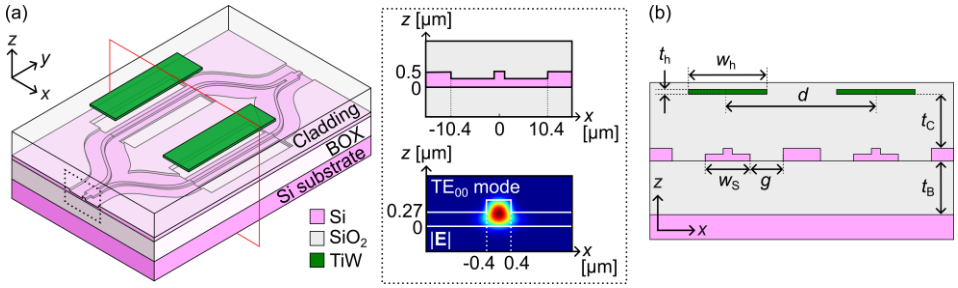

Fig. 1. (a) Schematic of a symmetric MZI with arms incorporating type-1 TOPSes. The black dotted box shows the cross-section of a standard single-mode rib (SMR) waveguide and the electric field distribution of its fundamental transverse electric (TE) mode. (b) Cross-sectional schematic of the MZI, corresponding to the red box in (a). The type-1 TOPS comprises a TiW heater (width w_h) and a rib waveguide with a finite slab width (w_s).

rib edges and these remnant Si regions is 10 μm. Figure 1(a) presents the electric field profile of the fundamental transverse electric (TE) mode of the standard SMR waveguide, confirming that these remnant Si regions do not affect the mode propagation.

The Si patterns are encapsulated by a silicon oxide (SiO_x) cladding, on which titanium tungsten (TiW) heaters are deposited. The width of the TiW heaters is denoted by w_h, and the center-to-center distance between the heaters (or the type-1 TOPSes) is represented by d. A thin SiO_x layer protects the heaters. The thicknesses of the TiW heaters and the SiO_x protection layer are fixed at 200 nm and 300 nm, respectively, by the foundry service. We calculated that the metal-induced propagation loss for the rib waveguide is negligible when the SiO_x cladding is thicker than 0.8 μm. Therefore, we set the SiO_x cladding thickness to 1 μm, a choice that minimizes propagation loss in the rib or SMR waveguide while efficiently coupling heat from the heaters.

2.2. *Determination of TOPS-related parameters*

We determined the optimal structural parameters for the type-1 TOPS—namely, slab width (w_s), heater width (w_h), heater length (L), distance to remnant Si regions (g), and center-to-center distance between TOPSes (d)—to minimize optical loss, power consumption, and thermal crosstalk. This optimization was performed using optical mode and heat simulations with Ansys Lumerical MODE and HEAT softwares.

Table 1. Thermal properties of materials

Material	Density [kg/m^3]	Specific heat [J/kg·K]	Thermal conductivity [W/m·K]	Electrical conductivity [S/m]
Si substrate	2330	711	148	3.11×10^{-4}
Si (500 nm)	2330	711	110 [24]	3.11×10^{-4}
Si (220 nm)	2330	711	90 [24]	3.11×10^{-4}
TiW	19250[a]	134 [a]	11.9 [b]	1.64×10^{6}
SiO_2	2203	709	1.38	1×10^{-15}
Air	1.18	1006	0.0263	1×10^{-12}

[a]TiW, composed of 10% Ti and 90% W by weight, has its density and specific heat estimated using a weighted average of the respective properties of Ti and W.

[b]The thermal conductivity (κ) of TiW is estimated using the Wiedemann-Franz law: $\kappa = \sigma LT$, where σ is the electrical conductivity of TiW, L is the Lorentz number, and T is temperature (298 K).

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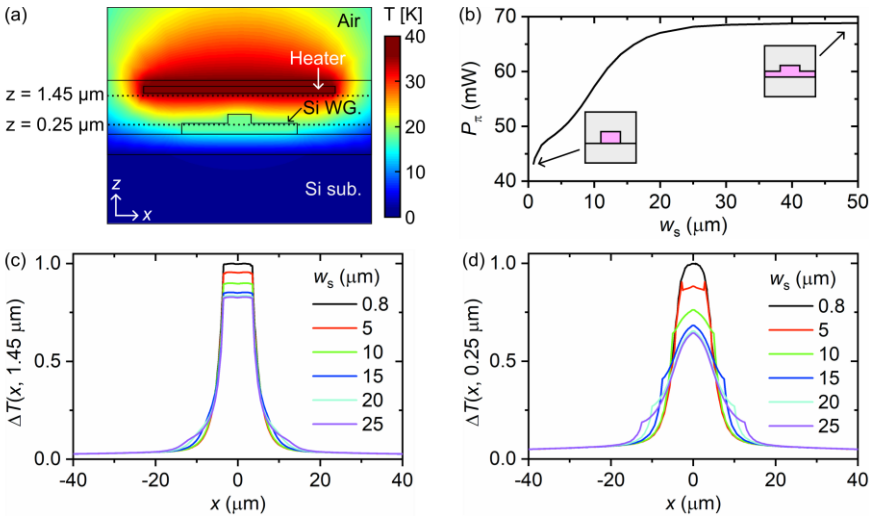

Fig. 2. (a) Temperature change distribution $\Delta T(x, z)$ of the type-1 TOPS with $w_s = 4\,\mu m$, $w_h = 7\,\mu m$, $P = 50$ mW, and $L = 240\,\mu m$. (b) Relationship between P_π and w_s. (c) and (d) $\Delta T(x, z)$ for various w_s values at $z = 1.45\,\mu m$ (c) and $z = 0.25\,\mu m$ (d).

To determine w_s, we first calculated the π-phase shifting power (P_π) as a function of w_s. This calculation began with simulating the temperature change distribution, $\Delta T(x, z)$, across the TOPS cross-section for arbitrary heater power (P) and TOPS length (L). For this simulation, we assumed the TOPS was uniform along the y-axis and that no intact Si regions were present (*i.e.,* $g = \infty$). The simulation domain was set to a width of 700 μm and a height of 350 μm. Boundaries were maintained at a constant temperature of 300 K, and a convection coefficient of 10 W/m^2/K was applied between the SiO_x layer and air. Other thermal properties of the TOPS materials are provided in Table 1.

Figure 2(a) presents the $\Delta T(x, z)$ profile calculated for $w_s = 4\,\mu m$, $w_h = 7\,\mu m$, $P = 50$ mW, and $L = 240\,\mu m$. The corresponding refractive index change distribution, derived from $\Delta T(x, z)$, was then imported into Lumerical MODE to determine the effective index change (Δn_{eff}) of the fundamental TE mode. The phase change ($\Delta\phi$) of the TOPS was subsequently calculated using $\Delta\phi = (2\pi/\lambda)\Delta n_{eff} L$, where λ is the vacuum wavelength. Finally, P_π was determined using $P_\pi = \pi P/\Delta\phi$.

The calculated relationship between P_π and w_s (Fig. 2(b)) indicates that P_π rapidly increases as w_s increases up to approximately 20 μm, beyond which P_π saturates. Figure 2(c) and (d) illustrate $\Delta T(x, z = 1.45\,\mu m)$ and $\Delta T(x, z = 0.25\,\mu m)$ for various w_s values. Immediately below the heater (at $z = 1.45\,\mu m$), ΔT remains significant within a ~20 μm width, irrespective of w_s. Due to Si's higher thermal conductivity compared to SiO_2, the Si slab efficiently conducts and dissipates heat. This is confirmed by the $\Delta T(x, z = 0.25\,\mu m)$ curves: as w_s increases up to 20 μm, ΔT within the Si slab decreases rapidly due to enhanced heat dissipation. However, for $w_s >$ 20 μm, ΔT changes minimally, as the Si slab is wider than the region of significant heat spread. This behavior explains the observed dependence of P_π on w_s in Fig. 2(b). Consequently, a smaller slab width is desirable to reduce the power consumption of the type-1 TOPS.

However, reducing w_s to the rib width of 800 nm could increase the propagation loss of the fabricated rib waveguide due to sidewall roughness from deep Si etching. Furthermore, integrating a mode converter between the rib and SMR waveguides would be necessary due to their different mode field profiles. Such a converter would occupy an additional chip area, potentially introduce excess loss, and could excite higher-order modes if not perfectly designed and fabricated. To address these challenges, the type-1 TOPS is directly connected to the

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SMR waveguide, and w_s is optimized to ensure a lossless transition between the rib and SMR waveguides while simultaneously preventing higher-order mode excitation.

We calculated both the effective index (n_{eff}) of the fundamental TE mode of the rib waveguide and the coupling loss (CL) at the rib-SMR junction. As shown in Fig. 3(a), for $w_s > 3\,\mu m$, n_{eff} converges to that of the SMR waveguide's fundamental TE mode. The inset in Fig. 3(a) displays the electric field profile of the rib waveguide's fundamental TE mode for $w_s = 4\,\mu m$, demonstrating that the relative electric field strength at the silicon slab sidewalls is on the order of 10^{-4}. In contrast, this value increases to the order of 10^{-1} at $w_s = 2\,\mu m$. This significant difference indicates that fabrication-induced slab sidewall roughness would lead to a notable increase in the rib waveguide's propagation loss for $w_s = 2\,\mu m$, a concern that is mitigated at $w_s = 4\,\mu m$. Because the fundamental TE modes of the two waveguides exhibit excellent matching for $w_s > 3\,\mu m$, the CL approaches 0 dB as w_s increases (Fig. 3(b)). Considering these factors, w_s was set to 4 μm to provide a sufficient margin for robust performance.

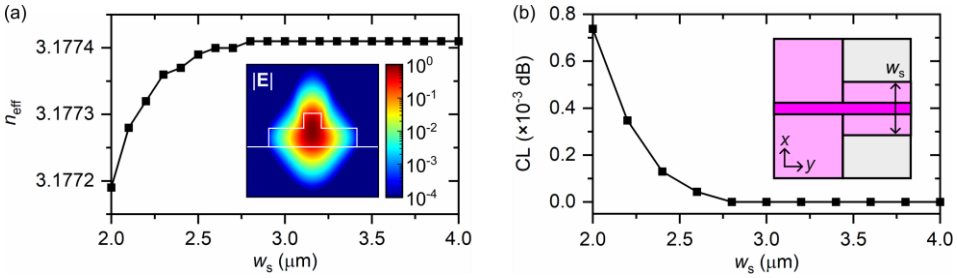

Fig. 3. (a) Calculated effective index (n_{eff}) of the rib waveguide's fundamental TE mode as a function of slab width (w_s). The inset displays the electric field distribution of this mode for $w_s = 4\,\mu m$. (b) Calculated coupling loss (CL) at the junction between the SMR and rib waveguides as a function of w_s. The inset illustrates the waveguide junction.

The heater parameters w_h and L were determined considering the maximum voltage (V_{max}) supplied by the driving integrated circuit. For PICs utilizing TOPSes, such as optical phased arrays, a maximum phase change of at least 2π is typically required. The relationship between P_π, applied voltage ($V_{2\pi}$) for a 2π phase change, and the TOPS resistance (R) is given by $V_{2\pi}^2 = 2P_\pi R$, where $R = \rho L/(w_h t_h)$ (ρ is the heater's resistivity; t_h is the heater thickness; $\rho = 0.61\ \Omega\cdot\mu m$ for TiW), with the constraint $V_{2\pi} \le V_{max}$.

To determine w_h and L using this expression, we first calculated P_π as a function of w_h, given that P_π is independent of L (Fig. 4(a)). As w_h increases, P_π also increases because the heater's power per unit width decreases. Subsequently, $V_{2\pi}$ was calculated using the derived expression and presented with several equi-$V_{2\pi}$ curves in Fig. 4(b). For a constant $V_{2\pi}$, L increases with w_h (Fig. 4(c)). The heater temperature change (ΔT_h) was calculated for (w_h, L) values along the $V_{2\pi} = 3.2$ V curve and is shown in Fig. 4(c). In contrast to P_π, ΔT_h decreases with increasing w_h. To balance P_π and ΔT_h for $V_{max} = 3.2$ V, we set w_h to 7 μm and L to 240 μm, resulting in $P_\pi = 48.6$ mW and $V_{2\pi} = 3.19$ V. For applications requiring a more compact TOPS, L can be reduced. However, shortening L from 240 μm to 150 μm increases both the current and ΔT_h corresponding to $V_{2\pi}$ from 30.5 mA to 38.6 mA and from 71.9 K to 115.1 K, respectively. Therefore, to maintain moderate current and thermal stability, a heater length of 240 μm is a more appropriate choice.

During the determination of w_s, w_h, and L, g was assumed to be infinite. Therefore, g was subsequently determined to ensure the adjacent intact Si regions do not affect P_π. As confirmed by the calculated relationship between P_π and g presented in Fig. 5(a), P_π converges to 48.6 mW for $g \ge 10\,\mu m$. The $\Delta T(x, z = 1.45\,\mu m)$ curves shown in Fig. 2(c) explain this result: if $g \ge 10\,\mu m$, the total width of the slab and gap ($2\,g + w_s$) becomes larger than the range of non-negligible ΔT,

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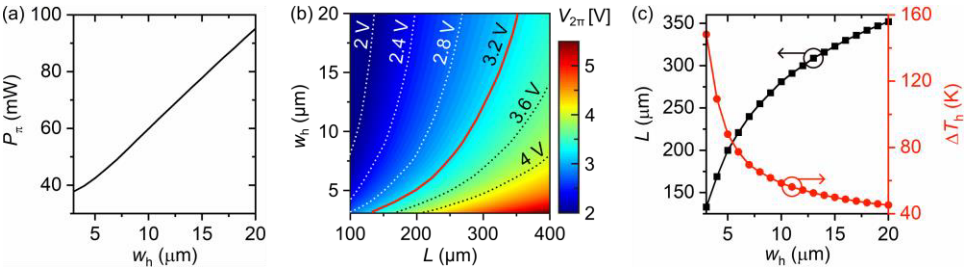

Fig. 4. (a) Relationship between P_π and heater width (w_h). (b) Voltage for a 2π phase change ($V_{2\pi}$) as a function of w_h and heater length (L). Equi-$V_{2\pi}$ contours are illustrated by white dotted curves, with the red line indicating the contour for $V_{2\pi} = 3.2$ V. (c) Heater length (L) required for $V_{2\pi} = 3.2$ V and the corresponding heater temperature change (ΔT_h) as functions of w_h.

ensuring the adjacent intact Si regions are outside this thermal influence zone. Consequently, g was set to 10 μm.

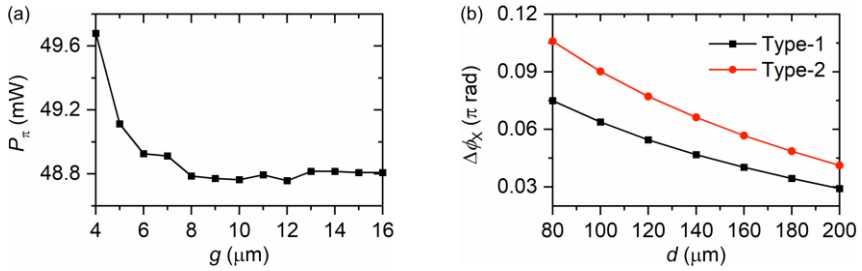

Fig. 5. (a) Relationship between P_π and the slab edge-to-intact Si region spacing (g) for the type-1 TOPS. (b) Relationship between thermal crosstalk ($\Delta\phi_X$) and the spacing between TOPSes (d) for the type-1 TOPS (black squares) and the type-2 TOPS (red circles). The heater length (L) for both TOPS types was set to 240 μm.

Finally, d was determined by calculating the thermal crosstalk ($\Delta\phi_X$) between adjacent TOPSes. $\Delta\phi_X$ is defined as the phase change induced in an adjacent TOPS when the power applied to the primary TOPS is $2P_\pi$ (Fig. 5(b)). As expected, $\Delta\phi_X$ decreases with increasing d, reaching 0.029π (significantly smaller than 2π) for $d = 200$ μm. Therefore, d was set to 200 μm.

In summary, the determined parameters for the type-1 TOPS are: $w_s = 4$ μm, $w_h = 7$ μm, $L = 240$ μm, $g = 10$ μm, and $d = 200$ μm. For comparison, a type-2 TOPS with $w_h = 7$ μm, $L = 240$ μm, and $d = 200$ μm (which can be considered to have $w_s = 20.8$ μm and $g = 0$ μm) was analyzed. This type-2 TOPS exhibits $P_\pi = 69.6$ mW, $V_{2\pi} = 3.19$ V, and $\Delta\phi_X = 0.041\pi$.

3. Experimental results and discussion

Symmetric MZIs incorporating the type-1 and type-2 TOPSes were fabricated using a commercial foundry service (Applied Nanotools Inc.). These devices were implemented on a SOI chip featuring a 500 nm Si layer and a 1 μm BOX layer. Different TOPS lengths (L) of 210 μm, 240 μm, and 270 μm were investigated. The Si patterns were defined through two successive rounds of electron-beam lithography and Si dry etching. The actual etching depth was measured to be 247 nm, which is 17 nm deeper than the design specification of 230 nm. Aluminum (Al) electrodes were formed to be connected to the TiW heater ends through via holes opened in the top SiO_x protection layer. Gold (Au) contact pads were subsequently deposited to be connected to the

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opposing ends of the Al electrodes. For each TOPS length, three identical MZIs were realized on the chip. Optical microscope images of fabricated MZIs with type-1 and type-2 TOPSes are presented in Fig. 6.

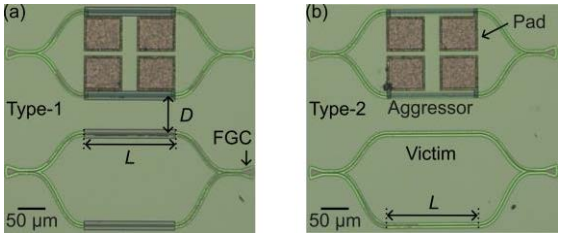

Fig. 6. (a) Optical microscope image displaying a fabricated pair of symmetric (aggressor) and asymmetric (victim) MZIs, with their arms integrating the type-1 TOPSes. (b) Similar optical microscope image, but for MZI pairs with arms incorporating the type-2 TOPSes.

To quantify the thermal crosstalk, an asymmetric MZI, comprising solely of the TOPS waveguides, was positioned adjacent to each symmetric MZI. In this configuration, the symmetric MZI served as the aggressor and the asymmetric MZI as the victim. The lateral separation distance (D) between their nearest waveguides was varied, with values of 100 μm, 150 μm, and 200 μm being explored. The length difference (ΔL) between the victim's SMR waveguides was maintained at 55.7 μm for all measurements.

Optical measurements were performed using a tunable laser source (TLS) and an optical power meter (OPM). Light from the TLS was coupled into the device via an input FGC using a single-mode fiber (SMF). The output light from the device was then collected by another SMF, connected to an output FGC, and subsequently directed to the OPM. The polarization of the incident light was controlled using a fiber polarization controller to ensure efficient launching of the fundamental TE mode into the SMR waveguide. Prior to the main measurements, the SMR waveguide, FGC, and 1×2 MMI splitter were individually characterized. At a wavelength of 1550 nm, the propagation loss of the SMR waveguide was determined to be 1.5 dB/cm. The coupling loss for the FGC was measured as 6 dB, and the excess loss of the MMI splitter was 0.2 dB.

3.1. Static performance

P_π was determined by measuring the transmittance of each symmetric MZI while supplying varying voltage and current to the TOPS heater using a source-measure unit (SMU). The transmittance values were normalized with respect to the transmittance of a reference SMR waveguide connected to the input and output FGCs. The heater power (P) was calculated directly from the voltage and current readings obtained from the SMU.

The measurements were conducted with a maximum heater power of 280 mW and a maximum current of 55.3 mA, flowing through 210-μm-long heaters. At this current level, the heaters operated reliably without failure. The foundry's design rules specify a maximum current density of 70 mA/μm^2, which for our heaters corresponds to a maximum allowed current of 98 mA. Therefore, the measurements were performed well within the safe operating limit, mitigating the risk of heater burnout.

Figure 7 illustrates the measured normalized transmittance (T) as a function of the applied power (P) for both type-1 and type-2 TOPSes with a length $L = 240$ μm. The minimum and maximum transmittances correspond to the insertion loss (IL) of the TOPS and the extinction ratio of the symmetric MZI, respectively. The power difference between two consecutive transmittance dips corresponds to $2P_\pi$. For the $L = 240$ μm devices, the measured P_π values were 55.7 mW for the type-1 TOPS and 80.9 mW for the type-2 TOPS. To ensure statistical robustness, P_π values

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for six identical TOPSes of each length were measured and subsequently averaged. Table 2 summarizes these averaged results, along with the average IL values obtained using the same method.

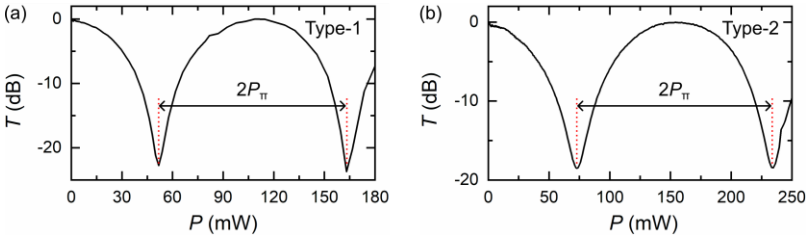

Fig. 7. Measured transmittances (T) of the symmetric MZIs as functions of heater power (P). (a) Result for the MZI with the type-1 TOPSes in their arms. (b) Result for the MZI with type-2 TOPSes in their arms. All TOPSes had a heater length (L) of 240 μm.

Table 2. Measured average P_π and IL values of type-1 and type-2 TOPSes

L [μm]	P_π [mW]		IL [dB]	
	Type-1	Type-2	Type-1	Type-2
210	58.2 ± 2.49	82.5 ± 4.64	0.294 ± 0.090	0.173 ± 0.102
240	54.7 ± 2.68	78.6 ± 2.24	0.256 ± 0.077	0.024 ± 0.091
270	54.6 ± 2.15	77.5 ± 1.09	0.088 ± 0.065	0.058 ± 0.061
Total[a]	55.9 ± 2.99	79.6 ± 3.72	0.193 ± 0.099	0.089 ± 0.107

[a]Average P_π and IL values for all heater lengths

A notable finding is that for all investigated lengths, the type-1 TOPSes consistently exhibit an approximately 30% reduction in P_π compared to the type-2 TOPSes. This experimental observation aligns well with our prior simulation results (as discussed in Section 2) and underscores the crucial role of the type-1 TOPS' rib waveguide with its finite slab width in achieving lower heater power consumption. However, the P_π values for the type-1 TOPSes are larger than those for conventional TOPSes based on standard SOI platforms; an analysis of this difference is explained in the Discussion section.

The IL difference between type-1 and type-2 TOPSes is minimal, with both being approximately 0 dB when accounting for the excess loss of the MMI splitter. This finding suggests that the propagation loss of the type-1 TOPS' rib waveguide is comparable to that of the type-2 TOPS' SMR waveguide. It also confirms that the coupling loss (CL) between the rib and SMR waveguides is negligibly small, validating the simulation results presented in Fig. 3.

The extinction ratios of several symmetric MZIs were measured to be less than 20 dB, regardless of the TOPS type. This reduced extinction ratio is likely due to the nonideal performance of the fabricated MMI splitters. To improve the extinction ratio, MMI splitters with a greater tolerance to fabrication errors should be designed and implemented [25].

While two-dimensional simulations, assuming y-axis uniformity, predict P_π to be independent of L, the experimentally obtained average P_π values show a slight decrease with increasing L. Furthermore, the average P_π values for the type-1 and type-2 TOPSes are experimentally measured to be 5 mW and 7 mW larger, respectively, than their calculated counterparts. These discrepancies are likely attributable, in part, to heat transfer from the heater ends to the measurement probes in contact with the gold pads, leading to localized cooling. As L increases, the influence of this localized cooling on the central part of the heater diminishes, thus leading to the observed slight decrease in P_π.

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Thermal crosstalk ($\Delta\phi_X$) was quantified by measuring the transmission spectra of a victim MZI both with and without $2P_\pi$ supplied to an adjacent aggressor's TOPS. The two obtained spectra were then fitted using the following expression:

$$T = \frac{a^2}{2}\left[1 + m\cos\left(\frac{2\pi L}{\lambda}\Delta n_{\text{eff, X}} - \frac{2\pi\Delta L}{\lambda}n_{\text{eff}}\right)\right], \tag{1}$$

where a represents the victim's attenuation factor, m is the modulation index, and $\Delta n_{\text{eff, X}}$ denotes the effective index change induced in the victim's TOPS waveguide adjacent to the aggressor. $\Delta\phi_X$ is directly determined by $2\pi L\Delta n_{\text{eff, X}}/\lambda$. Figure 8(a) and (b) present the measured and corresponding fitted spectra for the type-1 and type-2 TOPSes, respectively, for devices with $L = 240\,\mu\text{m}$ and a separation distance $D = 100\,\mu\text{m}$. Figure 8(c) and (d) show the extracted $\Delta\phi_X$ values at a wavelength of 1550 nm.

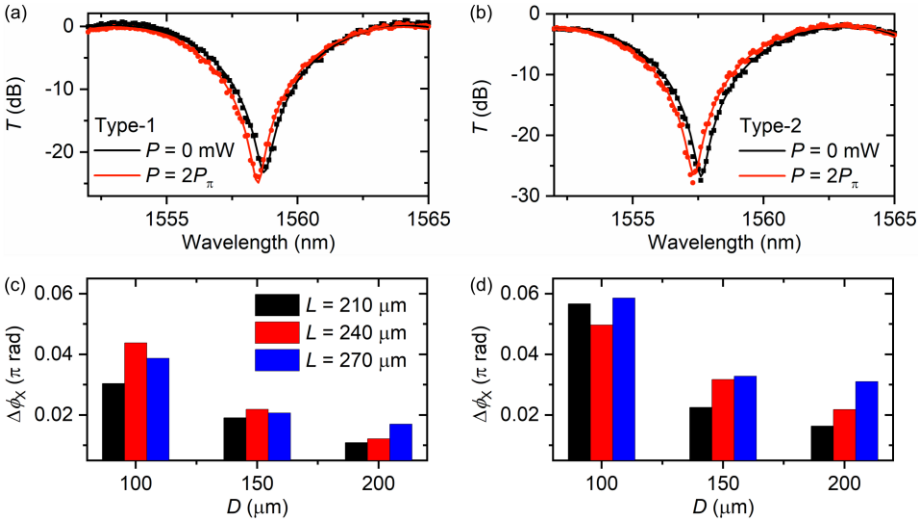

Fig. 8. (a), (b) Measured (symbols) and fitted (lines) transmission spectra of the victim MZIs. The spectra are shown with (red) and without (black) $2P_\pi$ applied to the adjacent aggressor's (a) type-1 and (b) type-2 TOPSes. Both TOPSes had a heater length (L) of 240 μm. (c), (d) Extracted thermal crosstalk ($\Delta\phi_X$) versus the aggressor-victim spacing (D). Results are presented for (c) the type-1 TOPSes and (d) the type-2 TOPSes, with $L = 210$, 240, and 270 μm.

Overall, $\Delta\phi_X$ is observed to decrease with increasing D. Critically, the type-2 TOPSes consistently exhibit larger $\Delta\phi_X$ values compared to the type-1 TOPSes across all tested configurations. For instance, when $L = 240\,\mu\text{m}$ and $D = 200\,\mu\text{m}$, the $\Delta\phi_X$ values for the type-1 and type-2 TOPSes were 0.012π and 0.022π, respectively. This result strongly reinforces the significance of the finite slab region in the type-1 TOPS waveguide for effective reduction of thermal crosstalk between adjacent devices.

3.2. Dynamic performance

The temporal responses of the type-1 and type-2 TOPSes were characterized by applying a rectangular voltage waveform to each TOPS within the symmetric MZIs. This waveform oscillated between 0 V and V_π, where V_π is the voltage corresponding to the determined P_π for each TOPS. The rectangular wave had a frequency of 0.1 Hz and a 50% duty cycle. The optical output power of the MZI was measured using a photodetector (PD) connected to an oscilloscope.

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The PD output voltage waveform was normalized to its maximum output voltage for comparative analysis.

Figure 9 displays the normalized PD output voltage (V_n) transitions, where the falling edge corresponds to the rising voltage step applied to the TOPS heater, and the rising edge corresponds to the falling voltage step. Figure 9(a) and (b) present the temporal responses for the type-1 TOPS with $L = 240\,\mu m$, while Fig. 9(c) and (d) show those for the type-2 TOPS with $L = 240\,\mu m$. From these curves, the fall and rise times for the type-1 TOPS were determined to be 7.24 μs and 7.00 μs, respectively. The type-2 TOPS exhibited comparable fall and rise times of 7.14 μs and 7.33 μs, respectively. Table 3 summarizes the average fall and rise times obtained from measurements on six TOPSes for each length. Consistent with the P_π measurements, the temporal response times do not exhibit a significant dependence on L. Interestingly, and in contrast to the P_π values, both type-1 and type-2 TOPSes demonstrate similar fall and rise times.

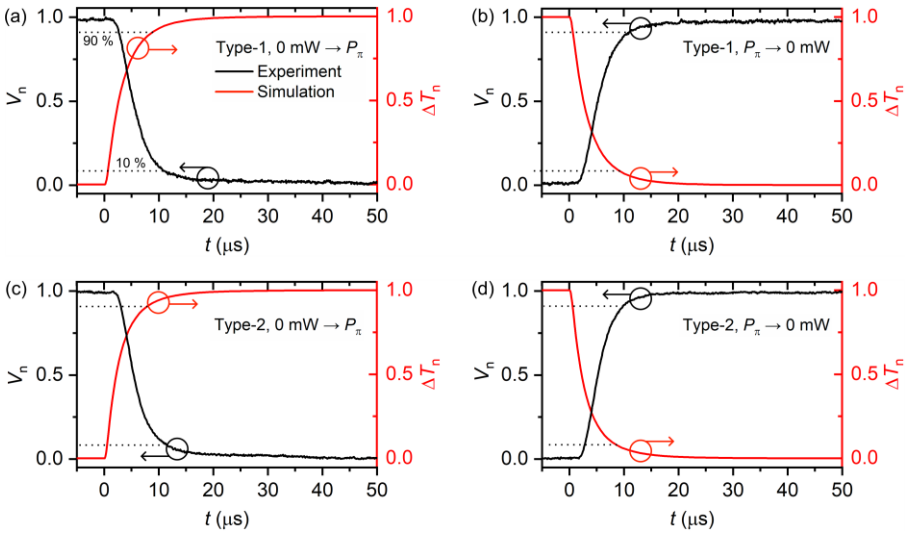

Fig. 9. Measured temporal changes in normalized PD output voltage (V_n) (black lines) and calculated temporal changes in normalized temperature change (ΔT_n) (red lines). (a) and (b) show the falling and rising transitions of V_n (the rising and falling transitions of ΔT_n), respectively, corresponding to rising and falling voltage steps applied to the type-1 TOPS with $L = 240\,\mu m$. (c) and (d) present the same transitions for the type-2 TOPS with $L = 240\,\mu m$.

Table 3. Measured average rise (τ_r) and fall (τ_f) times of the type-1 and type-2 TOPSes

L [μm]	Type-1		Type-2	
	τ_r [μs]	τ_f [μs]	τ_r [μs]	τ_f [μs]
210	7.74 ± 2.33	6.92 ± 1.80	5.85 ± 0.363	7.56 ± 2.58
240	7.09 ± 1.15	6.93 ± 1.07	6.67 ± 0.796	7.22 ± 1.36
270	8.51 ± 2.61	7.06 ± 2.68	7.78 ± 1.90	7.12 ± 1.70

For comparison, theoretical temporal responses of the TOPSes were calculated based on a two-dimensional simulation, assuming y-axis uniformity. Initial simulations with large domains (*e.g.*, 700 μm × 350 μm) produced inaccurate results, including long rise and fall times and slow saturation. Consequently, the simulation domain was optimized to 70 μm × 100 μm. In these simulations, the power supplied to the heater was modeled as a step increase from 0 to P_π or

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a step decrease from P_π to 0 at $t = 0$ s. The temperature change (ΔT) at the specified point (x, z) = (0, 0.240) μm was calculated as a function of time and normalized to its maximum value (ΔT_n). The calculated rising and falling edges of ΔT_n are superimposed with the corresponding falling and rising edges of the measured V_n in Fig. 9.

The simulated fall and rise times for the type-1 TOPS, which correspond to the rise and fall times of ΔT_n, were both calculated to be 7.81 μs. For the type-2 TOPS, both the calculated fall and rise times were 7.11 μs. These simulated temporal response times are similar to the experimentally measured values listed in Table 3. However, the simulation predicts that the type-2 TOPS has a slightly shorter rise time than the type-1 TOPS, which contradicts our experimental observation that the corresponding fall time of V_n for the type-2 TOPS is slightly longer. Investigations are ongoing to identify the potential reasons for this discrepancy.

3.3. Discussion

Conventional TOPSes fabricated on standard SOI platforms, typically employing a 220 nm Si layer and a 2 μm BOX layer, are reported to exhibit a P_π of approximately 21.4 mW and a response time of around 26.9 μs [6]. Our type-1 TOPS shows a higher P_π and shorter response time. These differences can be attributed to the distinct layer thicknesses of the type-1 TOPS, specifically the thinner BOX and SiO_x cladding layers compared to those of the conventional foundry TOPSes.

To substantiate this, we performed simulations to investigate the calculated relationships of P_π and the response time (defined as the rise time of ΔT_n) with respect to the BOX thickness (t_B) and the SiO_x cladding thickness (t_C). As shown in Fig. 10(a), with t_C fixed at 1 μm, an increase in t_B leads to a decrease in P_π. This is because a thicker BOX layer provides enhanced thermal isolation from the substrate, reducing heat dissipation into the substrate and thus improving heating efficiency. Conversely, as t_C increases with t_B fixed at 1 μm (Fig. 10(b)), P_π increases. A thicker cladding layer impedes heat flow from the heater to the waveguide, thereby necessitating more power to achieve the desired temperature change. In both scenarios (increasing t_B or t_C), the thermal capacity of the BOX or cladding layer increases, which consequently leads to an increase in the thermal response time.

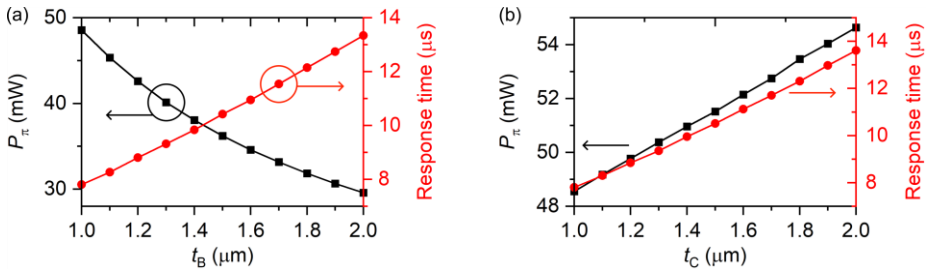

Fig. 10. Calculated type-1 TOPS' P_π (black curves) and response time (red curves) as functions of (a) the BOX thickness (t_B) and (b) the cladding thickness (t_C). All other parameters are consistent with the design values.

To directly compare our type-1 TOPS with conventional foundry TOPSes, we simulated a type-1 TOPS assuming a BOX thickness of 2 μm and a cladding thickness of 2 μm, which are typical dimensions for conventionally used foundry TOPSes. Under these conditions, the simulated P_π and response time for the type-1 TOPS are 34.4 mW and 20.5 μs, respectively. Furthermore, the heater width also plays a role in determining both P_π and response time. Our simulations indicate that if the heater width were reduced from 7 μm to 5 μm, P_π decreases to 30.9 mW, and the response time becomes 20.1 μs. Consequently, the residual differences in P_π and response time between our type-1 TOPS and conventional TOPSes, after accounting for

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BOX and cladding thicknesses, are primarily attributable to the thicker Si patterns employed in the type-1 TOPS. The larger thermal mass associated with thicker Si patterns requires more energy to heat, contributing to a higher P_π, and can also influence the response time.

Despite the thicker Si patterns, the P_π for the type-1 TOPS can be made comparable to that of conventional TOPSes by reducing t_C. For example, a type-1 TOPS with $w_h = 5\,\mu m$, $t_B = 2\,\mu m$, and $t_C = 1\,\mu m$ is theoretically predicted to have a P_π of 26.8 mW and a response time of 12.9 μs. Furthermore, the power consumption of the type-1 TOPS could be reduced even further by incorporating deep trenches alongside the rib waveguide or by utilizing a folded or spiral rib waveguide geometry.

4. Conclusion

In this work, we have thoroughly investigated a novel TOPS specifically designed for SOI platforms featuring a 500 nm Si layer and a 1 μm BOX layer, a configuration primarily utilized for III-V/Si hybrid lasers. A key innovation of our TOPS design is its foundation on a rib waveguide with a finite slab width. This design element proved critical in effectively reducing both P_π and thermal crosstalk by strategically restricting lateral heat transfer within the finite Si slab. The TOPS was meticulously designed to ensure lossless coupling with standard single-mode rib waveguides, avoiding higher-order mode excitation while simultaneously achieving favorable performance metrics. Our fabricated TOPS demonstrates an average P_π of 55.9 mW, a thermal crosstalk of 0.012π at a separation distance of 200 μm, and a rapid response (rise) time of 7.09 μs. For comparative analysis, a reference TOPS based on a standard single-mode rib waveguide was also fabricated. This reference device exhibited an average P_π of 79.6 mW, a substantially higher thermal crosstalk of 0.022π, and a comparable response (rise) time of 6.67 μs. The direct comparison between these two TOPSes unequivocally highlights the paramount importance of incorporating a finite slab in mitigating both P_π and inter-device thermal crosstalk. Given its demonstrated low P_π, suppressed thermal crosstalk, and rapid response time, the proposed TOPS is envisioned to be a cornerstone component for various PICs, including III-V/Si hybrid laser-integrated PICs, mid-infrared PICs, and PICs leveraging vertical higher-order modes, all of which benefit from or necessitate the 500 nm Si layer SOI platform.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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