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LETTER

Ultra-low power and 1.5 bit/cell ternary-SRAM stability modeling for always-on applications

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Abstract We present an ultra-low power ternary SRAM (T-SRAM) with a storage capacity of 1.5 bit/cell, using a commercial 110-nm CMOS foundry for always-on applications, along with an analysis of its stability. By designing T-CMOS with SPICE compact model parameters, which are body-effect coefficient (m), peak electric field coefficient (C_{EP}), and gate width (W), band-to band tunneling current (I_{BTBT}) can be reduced to hundreds of fA range and it allows V_{DD} to scale down to 0.55 V. Finally, we experimentally demonstrate T-SRAM cell which static and dynamic powers are decreased to 4.5×10^{-2} and 1.3×10^{-7}, respectively.

Keywords: ternary-CMOS, SRAM, ultra-low power, data retention, dynamic robustness

Classification: Electron devices, circuits and modules (silicon)

1. Introduction

Ternary logic systems are proposed as a solution to overcome the power scaling limits of conventional CMOS technology by reducing circuit complexity [1, 2]. For the design of ternary digital systems such as microprocessors and artificial intelligence (AI) accelerators, various ternary memory cell designs using different ternary logics and devices have been proposed [3–6]. However, the additional third state increases the number of devices, which can significantly overload power efficiency.

Instead of the conventional ternary scheme design [7–14], a power-scalable single-V_{T} ternary inverter design has been proposed [15] and demonstrated using commercial CMOS processes [16], showing the scalability in 3-D fin field effect transistor (FinFET) structure [17]. Furthermore, short-channel effect immunity and variation tolerance of T-CMOS have been verified on 300-mm wafer [18]. In previous work, T-CMOS-based ternary SRAM (T-SRAM) design was proposed [19], which offers ultra-low power consumption and bit-density efficiency for ternary systems. This design enables storage of 1.5 bits per SRAM cell, and thus the memory capacity can be enhanced without increasing the cell area.

In this paper, we experimentally demonstrate ternary SRAM fabricated using a 110-nm commercial foundry, operating at a low V_{DD} of 0.55 V with enhanced power saving capability compared to binary SRAM at the same process node. We also present the stability analysis of T-SRAM cells using T-CMOS SPICE compact model. In read operation, the voltage of internal nodes (Q, QB) can be increased by charge sharing with bit lines that can affect cell stability. Conventional static noise margin (SNM) [20–24] does not capture the dynamic behavior of SRAM operation. Therefore, we apply the dynamic operating margin concept as with binary SRAM [25–30] to analyze the stability of T-SRAM accurately. Through an assessment of dynamic read margin based on T-CMOS compact model parameters, we propose optimized T-SRAM designs that improve stability and performance.

2. Scalability of T-CMOS technology

T-CMOS, which can be integrated with conventional CMOS, is an energy efficient ternary device technology. T-CMOS structure is shown in Fig. 1(a), with retrograde well doping for highly doped p-n junctions between drain (D) and body (B), which generate band-to-band tunneling current (I_{BTBT}).

Figure 1(b) presents the schematic of the standard ternary inverter (STI) using T-CMOS, with its operation illustrated in Fig. 1(c). The tunneling-based constant I_{OFF} (= I_{BTBT}) and subthreshold current (I_{sub}) enable three-valued trit-state in T-CMOS. The equations for T-CMOS (1)–(3) are realized as follows:

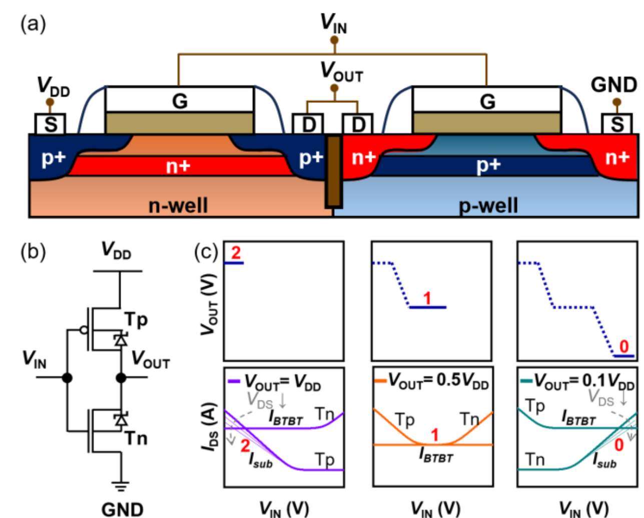

Fig. 1 (a) Device structure and (b) schematic of Ternary-CMOS. (c) Operation principle of the T-CMOS inverter. Trit-state can be made by subthreshold current and band-to-band tunneling current.

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Table I Description of the parameters used in T-CMOS compact model.

Parameter	Description	Parameter	Description
A	Junction cross-sectional area, $A = T_j \times W$	C_{ox}	Oxide capacitance
T_j	Standard deviation of the implanted body dopant distribution	γ	Junction abruptness parameter ($0 < \gamma < 1$)
W	Channel width	μ_{eff}	Effective mobility
L	Channel length	m	Body-effect coefficient
q	Electrical charge	k_B	Boltzmann's constant
m^*	Reduced effective tunnel mass	T	Absolute temperature
V_R ($= \lvert V_{DS} \rvert$)	Reverse biased drain voltage	V_T	Threshold voltage
E_g	Band-gap energy in silicon	ψ_{bi}	Built-in potential
E_p	Peak field as a function of V_{DS}	ε_{si}	Permittivity of Si

$$I_{BTBT} = A \frac{\sqrt{2m^*} q^3 E_P V_R}{4\pi^3 \hbar^2 E_g^{1/2}} \exp\left(-\frac{4\sqrt{2m^*} E_g^{3/2}}{3qE_P \hbar}\right) \quad (1)$$

$$E_P(V_{DS}) = \gamma \sqrt{2q\left(\frac{N_{body} N_{HDD}}{N_{body} + N_{HDD}}\right) \frac{(\lvert V_{DS} \rvert + \psi_{bi})}{\varepsilon_{si}}} = C_{EP} \sqrt{(\lvert V_{DS} \rvert + \psi_{bi})} \quad (2)$$

$$I_{sub} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) \left(\frac{kT}{q}\right)^2 \exp\left[\frac{q(V_{GS} - V_T)}{mkT}\right] \cdot \left(1 - \exp\left(-\frac{qV_{DS}}{kT}\right)\right) \quad (3)$$

where the included parameters are defined in Table I. Here, T-CMOS drain current consists of two off-state currents, given by $I_{DS} = I_{sub} + I_{BTBT}$.

In the intermediate state, a V_{IN}-independent I_{BTBT} flows in both T-nMOS (Tn) and T-pMOS (Tp), which results in voltage division and produces a stable $V_{DD}/2$ in each transistor. As shown in Fig. 2(a), I_{BTBT} is decreased depending on gate width (W) because of area reduction. In addition, I_{BTBT} decreases exponentially depending on V_{DS} (as shown in Fig. 2(b)). The optimal SNM is designed at $NM_H = NM_{MH}$, as demonstrated in the measured voltage transfer curve (VTC) of T-CMOS STI at $V_{DD} = 0.7$ V (see in Fig. 2(c)) with I_{BTBT} in the hundreds of fA range. Furthermore, scaled I_{BTBT} by a factor of $\times 1/10$ enables V_{DD} reduction to 0.55 V while maintaining the optimal SNM condition (see in Fig. 2(d)), which indicates feasible static and dynamic power scaling within the T-CMOS framework.

3. Ultra-low power T-SRAM demonstration

As illustrated in Fig. 3(a), the 6T T-SRAM consists of two cross-coupled T-CMOS STIs with two access Tn transistors, which results in ultra-low power efficiency. Figure 3(b) provides a top-view photograph of the packaged T-SRAM

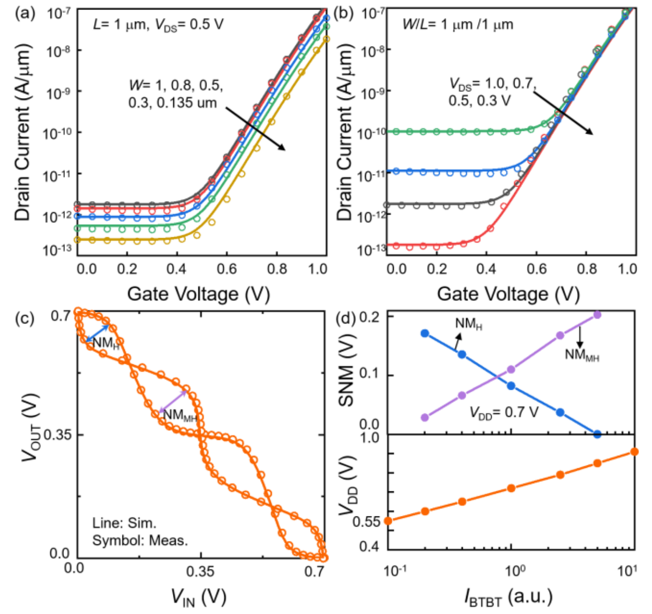

Fig. 2 Characteristics of T-CMOS I_{BTBT} of (a) width dependency and (b) V_{DS} dependency. The measured VTC of (c) T-CMOS inverter. (d) SNM and V_{DD} according to I_{BTBT}. NM_H represents noise margin at high level, NM_{MH} is noise margin at middle-high level.

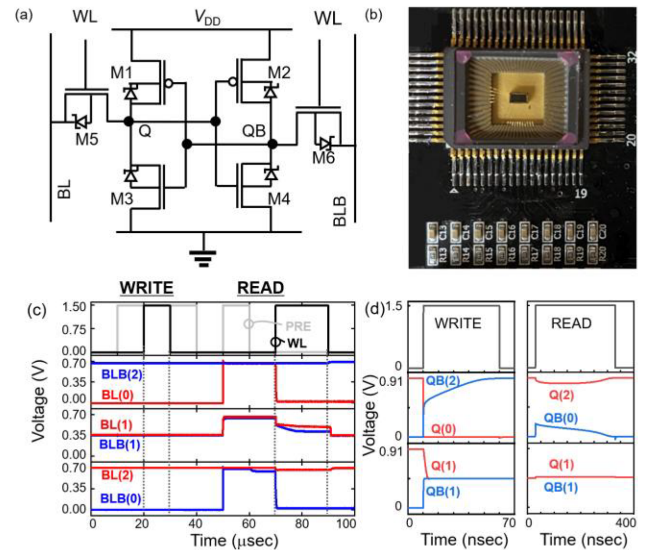

Fig. 3 (a) T-SRAM configuration based on T-CMOS and (b) photograph of packaged T-SRAM. (c) Measured write and read transient response of T-SRAM and (d) waveform with half-V_{DD} pre-charge scheme.

cell on board. Figure 3(c) shows the write/read operations at $W/L = 400$ nm/130 nm, successfully storing trit-state where Q = GND (0), Q = $V_{DD}/2$ (1), or Q = V_{DD} (2) within a compact 6T tritcell. The three possible states for Q and QB are: (Q/QB) = (2/0), (1/1), or (0/2). By scaling down transistor dimensions to minimum sizes, ultra-low power write/read operations are achieved. With a half-V_{DD} pre-charge applied to the bit lines, both the read delay and bit line power efficiency are improved, as the maximum delay occurs in the 0/2 operation shown in Fig. 3(d).

Figure 4(a) shows various SNMs for T-SRAM. In the T-SRAM cell, ensuring stability across hold, read, and write operations requires the evaluation of critical noise margins. Write Noise Margin (WNM) is defined as the minimum

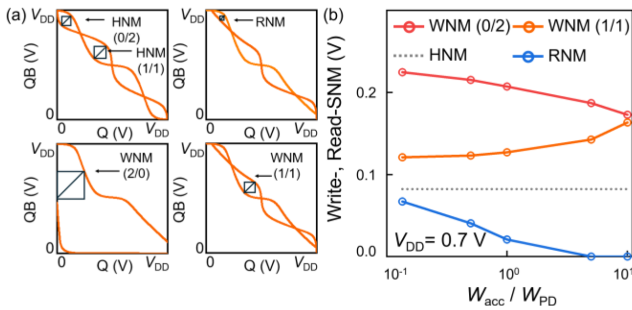

Fig. 4 (a) SNMs for T-SRAM operation (b) SNM of T-SRAM with ratio of W_{acc}/W_{PD}.

noise voltage that the cell can tolerate in a write operation without causing an unintended state change. Read Noise Margin (RNM) is the maximum noise voltage that the cell can endure in a read operation without disturbing the stored data. Hold Noise Margin (HNM) refers to the highest noise voltage the cell can sustain in the hold state, ensuring reliable data retention. The 0/2 WNM is defined when WL = V_{DD}, BL = V_{DD} (or GND), and BLB = GND (or V_{DD}) in T-SRAM configuration as shown in Fig. 3(a), while the WNM (1/1) occurs when WL = V_{DD} and BL = BLB = $V_{DD}/2$. HNM is defined when WL = GND, and RNM occurs when WL = V_{DD} and BL = BLB = $V_{DD}/2$. Figure 4(b) illustrates the stability of write, read, and hold operations for T-SRAM at V_{DD} = 0.7 V. Off-state current in the latch results in a lower RNM and a higher WNM. Therefore, it is necessary to analyze whether adequate RNM is achieved through a compact model. In addition, the cell can be optimized by adjusting the width of the access transistor and pull-down transistor to scale I_{BTBT}. A smaller W_{acc}/W_{PD} ratio, which indicates the width ratio between the access and pull-down transistors, is preferred for stable read operation with higher noise margin. Consequently, ultra-low power for write and read operations are achieved by reducing the width and length of all transistors to the minimum feature size.

4. Dynamic read stability

SNM is used to assess SRAM operation failure due to simple interpretation. However, SNM is unable to capture the nonlinear dynamics of cell operation. To address this limitation, dynamic stability analysis is proposed to account for time-dependent behavior. Read failure occurs when the previously stored data is corrupted. During the read operation, any increase in the node voltages of Q and QB, caused by charge sharing, is recovered by positive feedback mechanism, which works to restore the original state. However, if the recovery fails, data distortion occurs. In Fig. 5(a), M1 and M2 are pull-up transistors in the latch, while M3 and M4 are pull-down transistors in the latch. M5 and M6 are access transistors. Suppose the initial state of the SRAM is Q = V_{DD} and QB = 0, BLB discharges through M6, causing QB to rise while BL and Q remain unchanged. In Fig. 5(b), we define the minimum node voltage difference between Q and QB as a dynamic read margin (DRM). In 110-nm T-CMOS process, recovery fails when DRM is smaller than 0.112 V with C_{BL} = 672 fF.

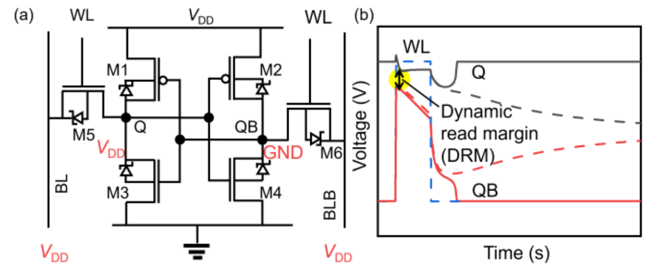

Fig. 5 Method to analyze read margin. (a) Schematic at 2/0 read and (b) waveform during dynamic analysis.

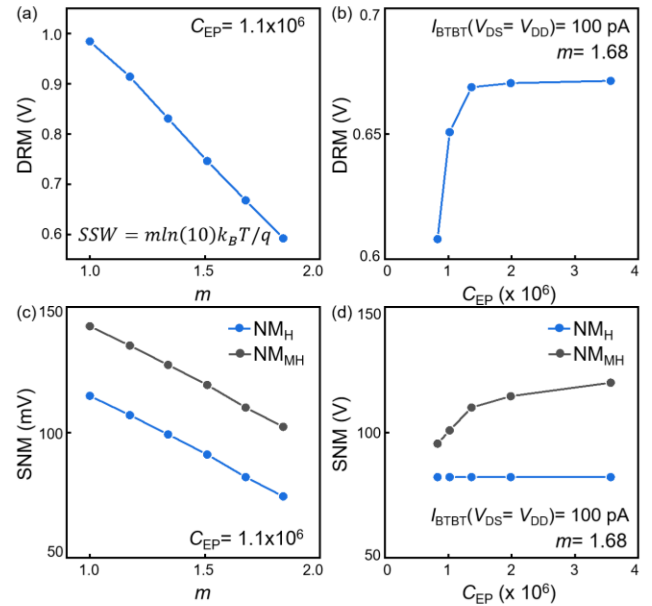

Fig. 6 DRM characteristics for T-CMOS compact model parameters (a) m and (b) C_{EP}. SNM properties by controlling (c) m and (d) C_{EP}.

Figure 6 shows the impact of the compact model parameters on T-SRAM stability. We modeled the currents I_{BTBT} and I_{sub} of T-CMOS to analyze T-SRAM cell characteristics, which covers the basic cell characteristics through SNM and advanced stability for the additional 1/1 state using DRM. Figure 6(a) illustrates the DRM as a function of the body-effect coefficient m. As m decreases representing an improvement in SSW, more stable read operations are observed. This is because a decrease in m leads to an increase in maximum current I_{MAX} (I_{sub} at V_{DS} = V_{DD}), and the recovery operation relies on the I_{MAX}. As the process node improves, SSW is enhanced to increase DRM. Fig. 6(b) presents DRM as a function of peak electric field coefficient C_{EP}, which represents the increase in I_{BTBT} with respect to V_{DS}. As the process node advances, the junction between the drain and channel doping to generate I_{BTBT} becomes more abrupt due to the lower thermal budget process, resulting in a higher C_{EP} value. When I_{BTBT} (V_{DS} = V_{DD}) is fixed at 100 pA, the value of I_{BTBT} at V_{DS} = $V_{DD}/2$ changes based on the C_{EP}. As C_{EP} increases, I_{BTBT} at V_{DS} = $V_{DD}/2$ decreases, making the recovery current I_{MAX}, which aims to return to 0/2, becomes dominant. Therefore, as C_{EP} increases, DRM also increases. Figure 6(c) and 6(d) illustrate the impact of compact model parameters on SNM. As m decreases, SSW improves because I_{sub} influences the transition regions

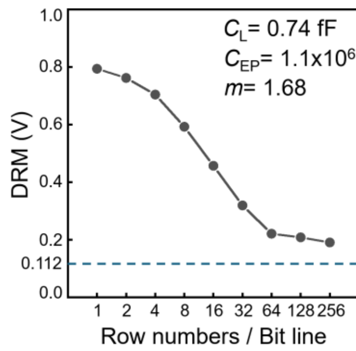

Fig. 7 DRM as the number of T-SRAM cells per local bit.

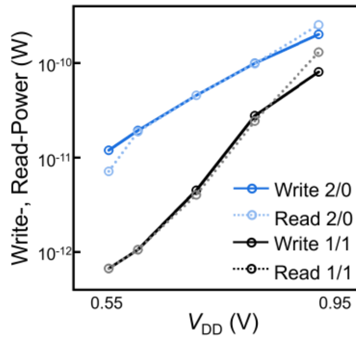

Fig. 8 Write and read powers of T-SRAM as a function of V_{DD} according to trit-state.

Table II Power efficiency comparison.

	V_{DD} (V)	$P_{D,Write}$ (W)	$P_{D,Read}$ (W)	$P_{S,Write}$ (W)	$P_{S,Read}$ (W)
SRAM bitcell	1.5	3.8x10^{-5}	3.1x10^{-5}	3.0x10^{-5}	6.2x10^{-11}
T-SRAM	0.55	1.7x10^{-6}	3.6x10^{-6}	3.9x10^{-12}	5.7x10^{-12}
T-SRAM/SRAM ratio	0.37	4.5x10^{-2}	0.17	1.3x10^{-7}	9.2x10^{-2}

for both 2 to 1 and 1 to 0. In addition, NM_{MH} increases with higher C_{EP} values due to the influence of the modified I_{BTBT} at V_{DS} = $V_{DD}/2$ on the 1-state region. Both static and dynamic stability are enhanced as C_{EP} increases and m decreases, which can be improved with the advanced process node. Figure 7 shows DRM of T-SRAM cell when varying the row numbers per bit line, with the loading capacitance (C_L) of T-CMOS set to 0.74 fF. Although the number of T-SRAM cells in bit line is increased, DRM remains higher than 0.112 V to operate stable read function.

Figure 8 shows the variations in write and read power with respect to V_{DD}. The power significantly reduces as V_{DD} decreases because I_{BTBT} exponentially depends on V_{DS}. Table II compares the power efficiency of T-SRAM with conventional 6T SRAM at the same process node. P_D represents dynamic power, and P_S denotes static power. The average power for T-SRAM is calculated as $(P_{0\text{-state}} + P_{1\text{-state}} + P_{2\text{-state}})/3$, given that T-SRAM has trit-state. Due to the off-state operation, which reduces the current flowing between the latch and access transistors, the proposed T-SRAM improves up to a 4.5×10^{-2} reduction in dynamic power. Additionally, the static power of the proposed T-SRAM is reduced by approximately 1.3×10^{-7} compared to the conventional bitcell.

5. Conclusion

We have experimentally demonstrated an ultra-low power and high density T-SRAM processed by a commercial 110-nm CMOS foundry. The significant effects of I_{BTBT} on noise margin and dynamic read stability enhancement have been analytically investigated based on the compact model. V_{DD} can be scaled down in the advanced process node due to the independent controllability of I_{BTBT} and V_T. Also, the dynamic read margin can be enhanced with improved compact model parameters C_{EP} and m in the scaled CMOS technology node. By using scaled V_{DD} and I_{BTBT}, dynamic and static powers are reduced compared to CMOS SRAM at the same process node. These results can provide the possibility of power scaling for always-on mobile/edge applications with higher bit density.

Acknowledgments

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