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Largely-Tuned Effective Work-Function of Al/Graphene/SiO_2/Si Junction with Electric Dipole Layer at Al/Graphene Interface

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The effective work-function of metal electrode is one of the major factors to determine the threshold voltage of metal/oxide/semiconductor junction. In this work, it is demonstrated experimentally that the effective work-function of the Aluminum (Al) electrode in Al/SiO_2/n-Si junction increases significantly by ≈1.04 eV with the graphene interlayer inserted at Al/SiO_2 interface. The device-physical analysis of solving Poisson equation analytically is provided when the flat-band voltage is applied to the junction, supporting that the large tuning of Al effective work-function may originate from the electric dipole layer formed by the off-centric distribution of electron orbitals between Al and graphene layer. Our work suggests the feasibility of constructing the dual-metal gate CMOS circuitry just by using Al electrodes with area-specific underlying graphene interlayer.

1. Introduction

The metal/oxide/semiconductor (MOS) structure has been used as an essential element in electronic device applications. It can function as a voltage-dependent variable capacitor (varactor). However, the most prominent usage is to work as the gate stack and current channel of MOS field effect transistor (MOSFET). In the real-world applications, both n- and p-channel MOSFET are used in combinatorial manners for minimizing the power consumption during device operation, bearing the name of complementary MOS (CMOS). There has been a tremendous amount of researches for improving and optimizing the operational characteristics of MOSFET.[1] In particular, the threshold voltages to form inversion channels in n- and p-channel MOSFET are strongly preferred to be symmetric from zero, meaning the same magnitude but opposite polarity, as much as possible.[2,3] These threshold voltages depend primarily on the work-function of gate metal electrode. More practical quantity for the MOS structure is the so-called effective work-function which is defined as the energy difference between the Fermi-level of metal and vacuum level of semiconductor in the flat-band situation.[4,5] Thus, the various layer-structural and chemical methods modulating the effective work-function of gate metal have been employed including metal interdiffusion,[6] post-treatment of insulating layer,[2,3,7–9] chemical reaction of metal and insulator,[10] and multiple oxide layers.[11] Recently, it has been reported that the work-function of a metal film can be modulated when the metal film being in contact with a graphene monolayer.[12–14]

In this work, we demonstrate experimentally that the flat-band voltage of metal/SiO_2/n-Si junction, interlocked with the effective work-function of gate metal, can change noticeably with a graphene interlayer inserted at metal/SiO_2 interface. We also show that the effective work-function change of metal/graphene stack can stem from the electric dipole layer formed between metal and graphene by solving the Poisson equation analytically to obtain the electron energy band profile of junction.[12–14] Most relevantly, the effective work-function of Al/graphene stack is found to increase quite a lot compared with Al, low work-function (≈4.08 eV)[15] metal suitable for n-channel MOSFET gate electrode, enough to be used as a gate electrode of p-channel

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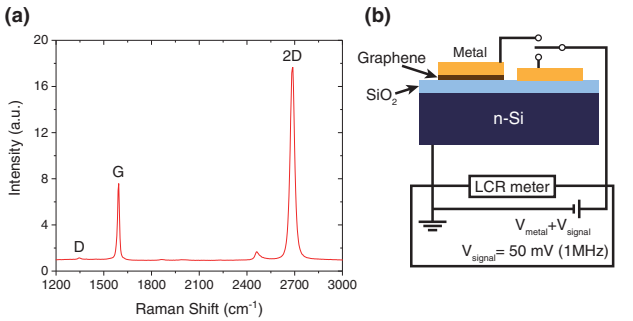

Figure 1. The structural quality of graphene and schematics of capacitance measurement. a) Raman spectrum measured on transferred monolayer graphene with D, G, and 2D peaks being indicated. b) Schematic view of MOS and MGOS junctions where the capacitance-voltage measurement configuration using LCR meter is drawn. The AC signal voltage V_{signal} is applied with the *rms* magnitude of 50 mV and the frequency of 1 MHz while DC bias V_{metal} is applied.

MOSFET. This implies that it will be possible to form the gate electrodes for both n- and p-channel MOSFET just with the Al metallization process.[2,3,16]

2. Results

The metal/graphene/oxide/semiconductor (MGOS) junctions for investigating the effective work-function modulation were prepared as follows. A ~30 nm thick SiO_2 layer was grown on an n-type Si wafer (donor concentration $N_D \approx 3\times10^{15}$ cm^{-3}) by using the dry oxidation and the SiO_2/Si substrate was cleaned in acetone and methanol, each for 5 min sequentially. Then, a graphene layer grown with chemical vapor deposition (CVD), purchased from the Graphene Supermarket Inc., was transferred partly onto the substrate by using the semi-dry transfer method reported previously.[17] After transferring the graphene layer, Raman spectroscopy was performed to evaluate the quality of the graphene layer. As shown in **Figure 1a**, the ratios of D peak to G peak and 2D peak to G peak are estimated to be ~0.03 and ~2.52, respectively. These indicate that the transferred graphene is a monolayer having a negligible number of defects.[18,19] To form the MOS and MGOS structures under the same metallization condition, circular metal electrodes with their diameter of ~500 μm and thickness of ~50 nm were deposited on the SiO_2/Si and graphene/SiO_2/Si areas simultaneously through a shadow mask. Then, the sample was exposed to O_2 plasma for isolating electrically individual metal electrodes underlined with the graphene interlayer. We first used aluminum (Al) electrodes to form the MOS and MGOS structures which were deposited by using thermal evaporation in high vacuum under ~5×10^{-6} Torr. The surface morphologies of deposited Al electrodes were investigated with the scanning electron microscope images, appearing to be similar on both structures (see the Supporting Information). The interaction of Al with graphene has been reported to be relatively weak enough to preserve the electronic structure of graphene around the Dirac point, meaning that the so-called physisorption occurs at the interface.[12–14] Hence, it is possible for us to use the linear density-of-states relation of graphene in calculating the energy band profile across the MGOS junction.[20,21]

After the sample preparation, we performed the capacitance-voltage (C–V) measurements in air and at room temperature to obtain the flat-band voltages (V_{FB}) of Al/SiO_2/Si and Al/graphene/SiO_2/Si junctions by using the Agilent E4980A LCR meter. The small AC voltage for probing the capacitive response of junction was set to be 50 mV (rms) at the frequency of 1 MHz and the DC bias voltage (V_{metal}) applied onto the metal electrode varies from −5 to 5 V as illustrated in Figure 1b. The C-V measurements were performed on three different junctions for each of Al/SiO_2/Si and Al/graphene/SiO_2/Si junctions. **Figure 2a** shows the measured *C–V* curves for Al electrode where the typical capacitance characteristics of p-channel MOS are observed. Here, the *C–V* curve is found to be shifted to the right with the graphene interlayer, implying that the effective work-function of Al electrode increases. The measured capacitance is maximized when the Si substrate has NO depletion region developed (accumulation state). The maximum capacitance, typically called the accumulation capacitance (C_{acc}), was obtained to be ~6.89×10^{-4} F m^{-2} on average for the Al/SiO_2/Si junction. Likewise, the averaged accumulation capacitance of the Al/graphene/SiO_2/Si junction was obtained to be ~6.38×10^{-4} F m^{-2}.

By estimating the flat-band capacitance in the measured *C–V* curve, we extracted the V_{FB} of each junction.[22] The average V_{FB} of Al electrode measured over three different junctions for each

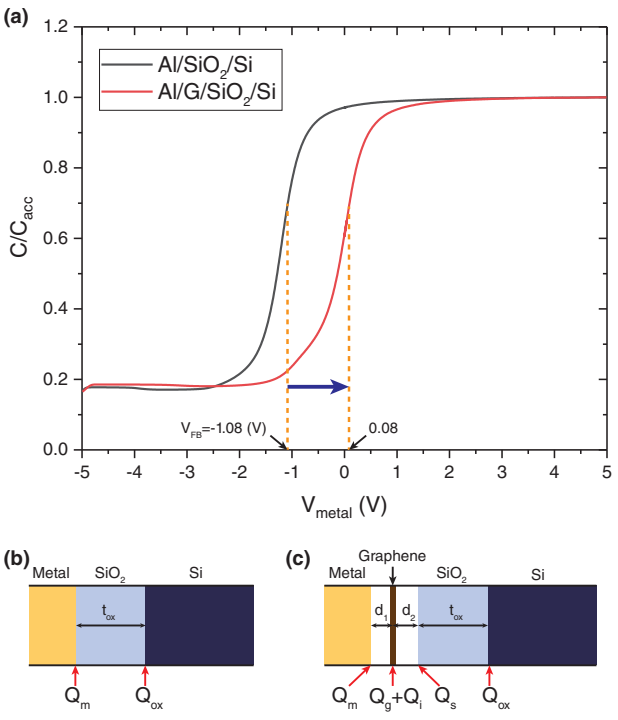

Figure 2. Capacitance-Voltage characteristics for Al electrode. a) Capacitance (*C*), normalized to accumulation capacitance (C_{acc}), measured as a function of voltage applied on metal (V_{metal}) for Al/SiO_2/Si and Al/graphene/SiO_2/Si junctions. The measurements were performed on multiple junctions for both cases and one specific measurement outcome is shown for each case. The V_{FB} of each junction is indicated with the orange dotted lines. Al/graphene electrode is written shortly as Al/G. Charge distributions of b) Al/SiO_2/n-Si and c) Al/graphene/SiO_2/n-Si junctions at $V_{metal} = V_{FB}$.

Table 1. Material parameters used in analytical electrostatic modeling. Metal work-function (ϕ_m), electron affinity of Si (χ_s), dielectric constant of SiO_2 (ϵ_{ox}) and Si (ϵ_s), effective density-of-states for the conduction band of Si (N_C), intrinsic work-function of graphene (ϕ_g), and Fermi-velocity of graphene (ν_F) used in the calculation.

ϕ_m (Al)[15]	ϕ_m (Pt)[32]	χ_s[34]	ϵ_{ox}[33]	ϵ_s[34]	N_C[34]	ϕ_g[26]	ν_F[26]
4.08 eV	5.65 eV	4.05 eV	3.9	11.7	2.82×10^{19} cm^{-3}	4.50 eV	10^6 m s^{-1}

of Al/SiO_2/Si and Al/graphene/SiO_2/Si junctions was found to be −0.98 and 0.06 V, respectively, indicating that the V_{FB} shift is quite significant to be 1.04 V. From the extracted V_{FB}, the effective work-function of metal electrode can be obtained with the conventional MOS capacitance formalism assuming the existence of fixed charges (Q_{ox}) in the SiO_2 layer. If V_{metal} is equal to the V_{FB}, there should be NO depletion or inversion charges on the semiconductor side. Then, the Q_{ox} including bulk electron traps and ionic impurities can be obtained from Equation (1) below reflecting the charge distribution shown in Figure 2b.[23,24]

$$\phi_m = \chi_s + V_n + V_{FB} + \frac{Q_{ox}t_{ox}}{\epsilon_{ox}\epsilon_0} \quad (1)$$

where ϕ_m is the metal work-function, χ_s is the electron affinity of Si, V_n is the electrostatic potential amounting to the difference between the conduction band minimum and the Fermi level of bulk n-Si, t_{ox} is the thickness of SiO_2 layer, ϵ_0 is the vacuum permittivity and ϵ_{ox} is the dielectric constant of SiO_2. V_n is calculated with $(k_BT/q)\ln(N_C/N_D)$ where k_B is the Boltzmann constant, T is the temperature, q is the elementary charge, and N_C is the effective density-of-states for the conduction band of Si. Here, we note that the energy unit is eV and energy and voltage can be treated equally in algebraic calculation. Q_{ox} is assumed to be located effectively at the SiO_2/Si interface.[2,8,22,25] It is also reasonable to assume that Q_{ox} is the same for MOS and MGOS junctions because both junctions are formed on the identical SiO_2/Si substrate.

As described before, the effective metal work-function ϕ_m^e of MOS capacitor represents the energy difference between Fermi-level of metal and vacuum level of semiconductor in the flat-band situation.[4,5] Then, the flat-band voltage should be equal to the difference of ϕ_m^e and work-function of semiconductor ϕ_s. That is, $V_{FB} = \phi_m^e - \phi_s$. Here, ϕ_s can be expressed as a sum of χ_s and V_n. Hence, the effective metal work-function becomes $\phi_m^e = \chi_s + V_n + V_{FB}$. From the extracted V_{FB}, the effective work-function of Al electrode is obtained to be ∼3.31 and ∼4.35 eV for Al/SiO_2/Si and Al/graphene/SiO_2/Si junctions, respectively. The increase of effective work-function with the graphene interlayer, amounting to over 1.00 eV, is quite significant as mentioned previously. Since the intrinsic work-function of graphene (ϕ_g) is ∼4.50 eV[26] larger just by ∼0.42 eV than that of Al, it seems not feasible to allocate the graphene work-function as the origin for such a large increase of effective work-function. We need to explore other physical mechanisms to explain this large tuning in the effective work-function of Al electrode. Similar phenomena have been reported in several previous researches including metal/graphene/GaAs junctions[14] and metal/graphene/Ge junctions.[27] One plausible way is to adopt the existence of an electric dipole layer formed at the metal/graphene interface stemming from the off-centric distribution of the overlapped electron wave functions between metal and graphene layers.[12–14] According to the density functional theory (DFT) calculation done by Khomyakov et al.,[12] the electrons mediating the bonding between metal and graphene are distributed more closely to the metal side for all physisorbed metals. Identical conclusions are made from another DFT calculation done by Gong et al.[13] This implies that an electric dipole layer forms at the metal/graphene interface with its direction pointing from metal to graphene. If denoting Q_i as the charge on the graphene side of the interface dipole layer, Q_i should be positive for all physisorbed metals. However, the polarity of Q_i was reported to be inverted when metals with relatively low work-function were contacted to graphene, observed in metal/graphene/GaAs junctions containing local patches of weak Fermi-level pinning.[14] By relying on the observation in metal/graphene/GaAs junctions, the Q_i is expected to be negative for the Al/graphene contact as well.

For more quantitative investigation on how the electric dipole layer at Al/graphene interface influences the measured C-V curves, we have performed the analytical electrostatic modeling to obtain the electron energy band profile across both MOS and MGOS junctions under the flat-band conditions. Figure 2b,c shows the charge distributions used in the modeling for MOS and MGOS junctions, respectively. Here, Q_m is the metal surface charge and Q_g is the doping charge in the graphene layer reflecting the free charge carrier transfer between metal and graphene layers due to the Fermi-level difference of them. The gap between metal and graphene layer d_1 is chosen to be ∼3.3 Å reported previously with the DFT calculation.[12] The gap between graphene and SiO_2 layer d_2 is assumed to be ∼5.0 Å, somewhat larger than the theoretically-predicted value ∼3.0 Å,[28] by considering the unavoidable existence of various wrinkles formed during the graphene transfer process. The wrinkles will reduce the overall flatness of transferred graphene, making the graphene and SiO_2 layers further apart from each other and increasing the average spacing between the two layers for the entire junction.[29] More detailed discussion about the rationale for assuming d_2 to be ∼5.0 Å can be found in the Supporting Information. It is well-known that the graphene layer transferred on the SiO_2 surface is p-type doped due to the electron transfer from the graphene layer to the surface states of SiO_2.[30] The negative charge density residing on the SiO_2 surface is labeled as Q_s which originates from the O-dangling bond states of SiO_2. The energy of O-dangling bond state is reported to be ∼1.5 eV below the Dirac point of graphene.[31] Hence, it is reasonably assumed that the O-dangling bond states are completely filled with electrons and Q_s stays constant regardless of what metal being used as the gate electrode and the range of gate voltage used in this work. Figure S1a, Supporting Information).

Based on the charge distributions shown in Figure 2, we first calculate the electrostatic potential $U(x)$ by solving the 1D Poisson equation $d^2U(x)/dx^2 = -\rho/\epsilon_r\epsilon_0$ where ϵ_r is the dielectric constant of either SiO_2 (ϵ_{ox}) or Si (ϵ_s).[21,23] Then, we derived the analytical expression of Q_i as shown in EQUATION (2) below (more detailed description for the electrostatic potential calculation including boundary conditions and charge densities can be found in the Supporting Information). The material parameters used in the calculation such as dielectric constant, metal work-function,

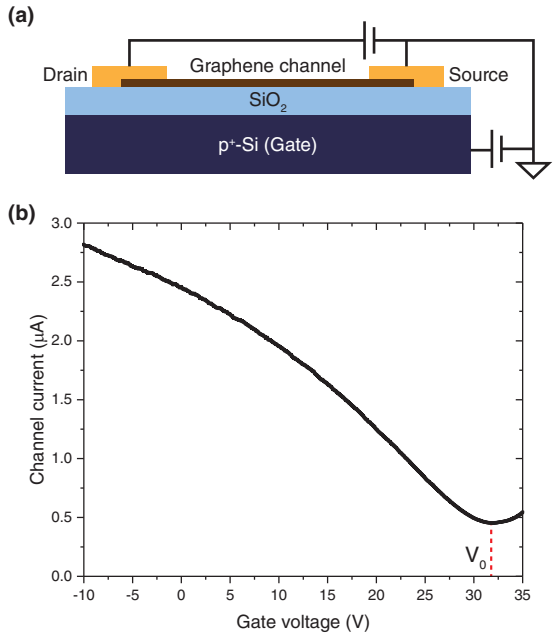

Figure 3. Device structure and electrical properties of GFET. a) Schematic cross-sectional view of GFET and b) measured source-drain current vs. gate voltage.

and bandgap were referred to the literature and are listed in **Table 1**.

$$Q_i = -Q_s - Q_{ox} - \frac{\epsilon_0}{d_1}\left(V_{FB} - \phi_m + \chi_s + V_n\right) - \frac{d_2}{d_1}\left(Q_s + Q_{ox}\right) - \frac{t_{ox}}{d_1 \epsilon_{ox}} Q_{ox} - Q_g \quad (2)$$

Here, the graphene doping charge is quantified as $Q_g = (q\Delta E_F|\Delta E_F|)/(\pi\hbar^2 v_F^2)$ where ΔE_F is the difference between Fermi-level and Dirac point of graphene layer and v_F is the Fermi-velocity of graphene.[20,21] Q_g can be determined by substituting $\Delta E_F = -\phi_g + V_{FB} + \chi_s + V_n + (d_2/\epsilon_0)(Q_s + Q_{ox}) + (t_{ox}/\epsilon_{ox}\epsilon_0)Q_{ox}$ derived from the calculated $U(x)$. Here, ϕ_g is the intrinsic work-function of graphene chosen to be 4.50 eV. Then, the only undetermined quantity is Q_s and it can be obtained experimentally from the transfer curve (source-drain current vs gate voltage) of graphene field effect transistor (GFET).[17] A GFET was fabricated on a highly p-doped Si substrate with a 100 nm thermally-grown SiO_2 layer on top. First, a graphene layer was transferred onto the substrate, then the source and drain electrodes were formed by e-beam evaporating Ti/Au film stacks through a shadow mask. After that, the graphene channel was defined with photolithography and subsequent O_2 plasma etching processes. Finally, the remaining photoresist was removed with acetone. The schematic illustration of fabricated GFET is shown in **Figure 3a**. The transfer curve of fabricated GFET shown in Figure 3b was obtained by sweeping the gate voltage from −10 to 35 V with the drain voltage of 0.1 V. In Figure 3b, the gate voltage inducing the minimum channel current (Charge Neutrality Point, CNP) is labeled as V_0 and its average value is obtained to be ~32.3 V from the measurements on three different GFETs. At $V_g = 0$ V, the net charge density in the graphene channel, amounting to its initial p-type (hole) doping density, is supposed to be equal to the surface charge density on the SiO_2 layer (Q_s). When the gate bias reaches the CNP ($V_g = V_0$), the net charge density in the graphene channel becomes nearly zero. Then, the Q_s will be compensated by the dielectric charge density induced on the SiO_2 surface, leading to $Q_s = \epsilon_{ox}\epsilon_0 V_0/(100\text{nm})$ where 100 nm is the thickness of gate insulator (SiO_2) for GFET. From the known or experimentally-obtained values of the accompanied parameters, it is obtained that $Q_s = -1.12\times10^{-6}$ C cm^{-2}. Subsequently, the Q_i of Al/graphene interface is calculated to be -2.85×10^{-7} C cm^{-2} from equation (2). Here, it is noted that the Q_i is found to be negative consistently with the previous experiments on Al/graphene/GaAs junctions.[14]

Based on the calculation above, the flat-band diagrams for Al/SiO_2/Si and Al/graphene/SiO_2/Si junctions are obtained as shown in **Figure 4** and the values of relevant parameters are summarized in the Supporting Information. One important point to make is that the increase of effective work-function (~1.04 eV) is quite close to the bandgap of Si (~1.12 eV) and the work-function of Al electrode (~4.08 eV) is very similar to the electron affinity of Si (~4.05 eV). This implies that the Al electrode suitable for n-channel MOSFET due to its relatively small work-function can also be used for p-channel MOSFET with a graphene interlayer. Hence, it will be possible to realize the dual-metal gate CMOS system just with Al electrodes.[2,3,16]

For comparing with a metal electrode of high work-function, MOS and MGOS junctions using Pt electrodes were also prepared by following the fabrication procedures identical to the Al electrode case. The work-function of Pt is ~5.65 eV, higher than that of graphene (~4.50 eV). Similarly to Al, the bonding between Pt and graphene is reported to be weak (physisorption). From the C-V measurements shown in **Figure 5**, the effective work-function of Pt electrode is found to decrease with the graphene interlayer. Specifically, the averaged effective work-function is measured to decrease from ~4.85 to ~4.66 eV manifested in the relatively small V_{FB} shift from ~0.57 to ~0.37 V.[32] The Q_i for Pt/graphene interface was calculated to produce the shift of ef-

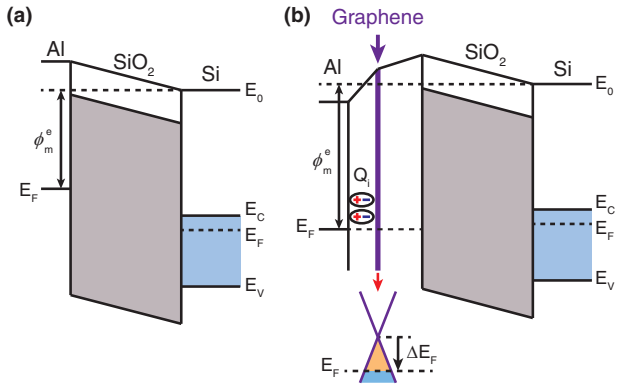

Figure 4. Modulation of energy band profile with graphene interlayer. Energy band profiles for a) Al/SiO_2/Si and b) Al/graphene/SiO_2/Si junctions under the flat-band voltage condition. Here, E_0 is the vacuum level, E_C is the conduction band minimum, E_V is the valance band maximum, and E_F is the Fermi-level.

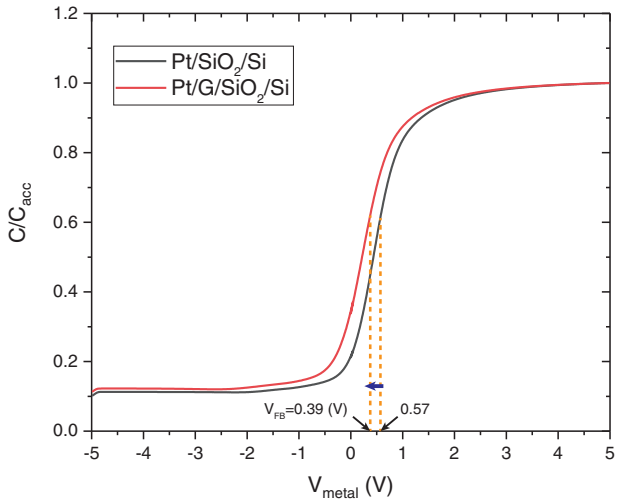

Figure 5. Capacitance-Voltage characteristics for Pt electrode. Capacitance (C), normalized to accumulation capacitance (C_{acc}), measured as a function of voltage applied on metal (V_{metal}) for Pt/SiO_2/Si and Pt/graphene/SiO_2/Si junctions. The measurements were performed on multiple junctions for both cases and one specific measurement outcome is shown for each case. The V_{FB} of each junction is indicated with the orange dotted lines.

fective work-function extracted from C-V measurements and it is listed in **Table 2**. The effective work-function decrease (~0.19 eV) with the aid of positive Q_i seems consistent with the previous work for Pt/graphene/GaAs junction where the Schottky barrier of junction was found to decrease substantially with the graphene interlayer.[14] The synergetic implication of the measurements with the two metals (Al, Pt) is that the effective work-function shifts observed for them cannot be explained altogether just by considering the free carrier doping of graphene layer. More concretely, if we don't include the Q_i, the other varying parameter d_2 needs to be different by an unreasonably large amount between the two metals in order to generate the shifts of effective work-function correctly for both metals. Hence, it seems inevitable to adopt the existence of Q_i for analyzing the measured data properly. The further detailed discussion on this point can be found in the Supporting Information.

The polarities of Q_i obtained for Al and Pt electrodes are consistent also with the theoretical model developed by Tung[35] which quantifies the electric dipole layer accompanied by atom-atom interaction at the metal/semiconductor interface. By noting that graphene can be treated as a semiconductor with zero energy bandgap, the model predicts that Q_i will be negative for a metal electrode with its work-function smaller than $\phi_g = 4.50$ eV (intrinsic work-function of graphene) such as Al and Q_i will be positive for the opposite case that Pt belongs to. Just as a reminder, the work-function of Al is 4.08 eV and that of Pt is 5.65 eV. By relying on the Tung's theoretical model matching with our experimental works, the work-function modulation of a metal layer in contact with a graphene layer is anticipated to change its sign when the work-function of metal is ~4.50 eV (inflexion of modulation).

Table 2. Measured and calculated device parameters. Averaged values of flat-band voltage, effective work-function, and interaction dipole charge obtained for Al and Pt electrodes *with* and *without* the graphene interlayer inserted at the metal/SiO_2 interface of metal/SiO_2/Si junction where Q_i value can be obtained only for metal/graphene/SiO_2/Si junctions.

	Al	Al/G	Pt	Pt/G
V_{FB} (V)	−0.98	0.06	0.57	0.37
ϕ^e_m (eV)	3.31	4.35	4.85	4.66
Q_i (10^{-7} C cm^{-2})	–	−2.85	–	15.98

The idea of incorporating other 2D materials as interlayers to modulate the electrical properties of interface has also been explored. One specific example is the theoretical work done by Su et al.[36] According to their DFT calculations, the Schottky barriers at metal/interlayer/MoS_2 junctions are associated primarily with the electric dipole layer formed at the metal/interlayer interface. The electric dipole layer at the interlayer/MoS_2 interface is negligible. Alongside our experimental findings, this work also indicates that the electric dipole layer at the metal/interlayer interface is the main factor determining the energy band profile across the junction with an interlayer being inserted.

Previously, Song et al.[37] investigated how the work-function of graphene varies with a metal overlayer also by comparing the C–V curves of MOS and MGOS junctions, very similarly to our approaches. Differently from our junctions, they mainly used so-called chemisorped (hybridization of electron orbitals between metal and graphene layer) metals including Pd, Ni, and Au/Cr. Hence, it is somewhat inappropriate to compare their experimental findings with ours directly. Indeed, they did NOT observe any significant difference in the work-function extracted from the C-V curve between MOS and MGOS junctions. More concretely, the Au/Cr electrode where the Cr layer in direct contact with graphene is relevant was found to have almost identical work-function to the bare (no graphene layer) Cr electrode, slightly below 4.3 eV. In the case of Ni electrode, the work-function was found to be slightly below 5.0 eV which is again very similar to the bare Ni electrode. Based on Song et al.'s and our works, it seems reasonable to conclude that the systematic formation of electric dipole layer at the metal/graphene interface occurs only for the physisorped metals.

3. Discussion

In conclusion, we have observed a significant increase of effective work-function (~1.04 eV) of metal electrode in Al/graphene/SiO_2/n-Si junction in comparison with Al/SiO_2/n-Si junction. The large tuning of effective work-function was revealed in C-V measurements and the analytical calculation of solving 1D Poisson equation at flat-band voltage was performed to figure out its physical origin. In the calculation, an electric dipole layer was adopted to form between metal and graphene, originating from the off-centric distribution of electron orbitals in the gap between the two layers. A similar effective work-function shift was observed also with Pt electrode. This time, the effective work-function was found to decrease by ~0.19 eV. In order to account for the observed shifts of effective work-function within the reasonable range of the spacing between graphene and SiO_2 layer, the interaction dipole layer is found to have its negative side toward the graphene layer for Al while the polarity is flipped over (the positive side toward the graphene layer) for Pt. If

considering the commonness and compatibility with the existing CMOS processes of Al as additional advantages, our work suggests that it will be possible to construct the dual-metal gate CMOS circuitry just with the single metallization process forming Al electrodes with area-specific underlying graphene interlayers in cost-effective and reliable manners.[2,3,16]

4. Experimental Section

Device Fabrication (More detailed): The metal/oxide/semiconductor (MOS) and metal/graphene/oxide/semiconductor (MGOS) junctions were fabricated simultaneously on a piece of SiO_2/Si substrate as follows. A ~30 nm thick SiO_2 layer was grown on an n-type Si wafer (donor concentration $N_D \approx 3\times10^{15}$ cm^{-3}) by using the dry oxidation and the SiO_2/Si substrate was cleaned in acetone and methanol each for 5 min sequentially. Then, a graphene layer grown with chemical vapor deposition (CVD), purchased from the Graphene Supermarket Inc., was transferred partly, about the half area, onto the substrate by using the semi-dry transfer method reported previously.[17] More concretely, a PMMA film is first spin-coated on the surface of the graphene grown on a Cu foil at 5000 rpm for 60 s. The graphene on the backside of the Cu foil is etched by using oxygen plasma in a reactive ion etching system. Then, a flexible Kapton tape is attached firmly on the PMMA side of the PMMA/graphene stack and the Cu foil is etched with ammonium persulfate. After removing the Cu foil, the Kapton/PMMA/graphene stack is rinsed with DI water several times. Then, the graphene side of the stack is blown with N_2 gas while being heated (70 °C for 15 min on a hot plate) to eliminate water molecules on the surface as completely as possible. After the N_2 blowing and heating step, the graphene side of Kapton/PMMA/graphene stack adheres to the surface of SiO_2/Si substrate. In order to obtain uniform adhesion, N_2 gas is blasted onto the center of Kapton/PMMA/graphene stack for ensuring the sequential pressing effect from the stack center toward its edge. After the graphene is transferred to the SiO_2/Si substrate, the sample is heated on a hot plate at ~150 °C for 15 min to improve the adhesion between the graphene and SiO_2 surface. After heating, the whole sample is dipped into acetone to remove the PMMA layer and the Kapton tape altogether. Finally, the sample is rinsed with isopropyl alcohol (IPA) and baked on the hot plate at ~200 °C for 15 min to dry off any solvent residues from the graphene surface. To form the MOS and MGOS structures under the same metallization condition, circular metal electrodes with their diameter of ~500 μm and thickness of ~50 nm were deposited on the SiO_2/Si and graphene/SiO_2/Si areas simultaneously through a shadow mask. Then, the sample was exposed to O_2 plasma for isolating electrically individual metal electrodes underlined with the graphene interlayer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

W.S., G.C., and K.P. performed conceptualization of device structure and experiments. W.S., J.-Y.L., JunK, and J.P. performed Device fabrication. W.S., J.J., E.H., JiK, and H.P. performed measurements. W.S., D.E., G.C., and K.P. performed data analysis. G.C. and K.P. performed supervision. W.S., G.C., and K.P. wrote the original draft. W.S., J.-Y.L., JunK, J.P., J.J., E.H., JiK, H.P., D.E., G.C., and K.P. wrote, reviewed, and edited.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

capacitance-voltage curve, dipole layer, effective work-function of gate electrode, electric, flat-band voltage, graphene interlayer, MOS junction

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[1] R. K. Ratnesh, A. Goel, G. Kaushik, H. Garg, Chandan, M. S., B. Prasad, *Mater. Sci. Semicond. Process.* **2021**, *134*, 106002.
[2] C. Zhao, J. Xiang, *Appl. Sci.* **2019**, *9*, 2388.
[3] A. Fet, V. Häublein, A. J. Bauer, H. Ryssel, L. Frey, *Appl. Phys. Lett.* **2010**, *96*, 053506.
[4] H. Zhu, R. Ramprasad, *Phys. Rev. B* **2011**, *83*, 081416.
[5] X. Ma, H. Yang, W. Wang, H. Yin, H. Zhu, C. Zhao, D. Chen, T. Ye, *J. Semicond.* **2014**, *35*, 096001.
[6] I. Polishchuk, P. Ranade, T.-J. King, C. Hu, *IEEE Electron Device Lett.* **2001**, *22*, 444.
[7] J. Tao, C. Z. Zhao, C. Zhao, P. Taechakumput, M. Werner, S. Taylor, P. R. Chalker, *Materials* **2012**, *5*, 1005.
[8] M. Ťapajna, K. Hušeková, J. Espinos, L. Harmatha, K. Fröhlich, *Mater. Sci. Semicond. Process.* **2006**, *9*, 969.
[9] I. Lundstrom, *Sens. Actuators* **1981**, *1*, 403.
[10] J. Lin, Y. Y. Gomeniuk, S. Monaghan, I. M. Povey, K. Cherkaoui, E. O'Connor, M. Power, P. Hurley, *J. Appl. Phys.* **2013**, *114*, 144105.
[11] X. J. Liu, L. Zhu, M. Y. Gao, X. F. Li, Z. Y. Cao, H. F. Zhai, A. D. Li, D. Wu, *Appl. Surf. Sci.* **2014**, *289*, 332.
[12] P. A. Khomyakov, G. Giovannetti, P. C. Rusu, G. Brocks, J. van den Brink, P. J. Kelly, *Phys. Rev. B* **2009**, *79*, 195425.
[13] C. Gong, G. Lee, B. Shan, E. M. Vogel, R. M. Wallace, K. Cho, *J. Appl. Phys.* **2010**, *108*, 123711.
[14] H. H. Yoon, W. Song, S. Jung, J. Kim, K. Mo, G. Choi, H. Y. Jeong, J. H. Lee, K. Park, *ACS Appl. Mater. Interfaces* **2019**, *11*, 47182.
[15] P. A. Tipler, R. A. Llewellyn, *Modern Physics*, Ed: W. H. Freeman, Wiley, New York, **2008**, Vol. *5*, p. 130.
[16] Y. C. Yeo, Q. Lu, P. Ranade, H. Takeuchi, K. J. Yang, I. Polishchuk, T. J. King, C. Hu, S. C. Song, H. F. Luan, *IEEE Electron Device Lett.* **2001**, *22*, 227.
[17] S. Jung, H. H. Yoon, H. Jin, K. Mo, G. Choi, J. Lee, H. Park, K. Park, *J. Appl. Phys.* **2019**, *125*, 184302.
[18] A. C. Ferrari, *Solid State Commun.* **2007**, *143*, 47.
[19] A. Das, B. Chakraborty, A. K. Sood, *Bull. Mater. Sci.* **2008**, *31*, 579.
[20] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, A. K. Geim, *Rev. Mod. Phys.* **2009**, *81*, 109.
[21] W. Kim, C. Li, F. A. Chaves, D. Jiménez, R. D. Rodriguez, J. Susoma, M. A. Fenner, H. Lipsanen, J. Riikonen, *Adv. Mater.* **2016**, *29*, 1845.

[22] K. Piskorski, H. M. Przewlocki, In *The 33rd International Convention MIPRO*, IEEE, Opatija, Croatia **2010**, 37–42.
[23] S. M. Sze, K. K. Ng, *Physics of Semiconductor Devices*, ed. 3, Wiley, New York **2007**, pp 213.
[24] D. K. Schroder, *Semiconductor Material and Device Characterization*, ed. 3, Wiley, New York **2006**, pp. 319–374.
[25] C. Cobianu, F. Nastase, N. Dumbravescu, O. Buiu, B. Serban, M. Danila, R. Gavrila, O. Ionescu, C. Romanitan, *Rom. J. Inf. Sci. Technol.* **2019**, *22*, 41.
[26] Y. J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, P. Kim, *Nano Lett.* **2009**, *9*, 3430.
[27] S.-h. C. Baek, Y.-J. Seo, J. G. Oh, M. G. Albert Park, J. H. Bong, S. J. Yoon, M. Seo, S.-Y. Park, B.-G. Park, S.-H. Lee, *Appl. Phys. Lett.* **2014**, *105*, 073508.
[28] W. Gao, P. Xiao, G. Henkelman, K. M. Liechti, R. Huang, *J. Phys. D: Appl. Phys.* **2014**, *47*, 255301.
[29] H. Zhong, Z. Liu, L. Shi, G. Xu, Y. Fan, Z. Huang, J. Wang, G. Ren, K. Xu, *Appl. Phys. Lett.* **2014**, *104*, 212101.
[30] X. F. Fan, W. T. Zheng, V. Chihaia, Z. X. Shen, J.-L. Kuo, *J. Phys.: Condens. Matter* **2012**, *24*, 305004.
[31] H.-J. Sung, D.-H. Choe, K. J. Chang, *New J. Phys.* **2014**, *16*, 113055.
[32] H. B. Michaelson, *J. Appl. Phys.* **1977**, *48*, 4729.
[33] C. M. Tanner, Y. C. Perng, C. Frewin, S. E. Saddow, J. P. Chang, *Appl. Phys. Lett.* **2007**, *91*, 203510.
[34] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, Springer, New York **2010**, p. 24.
[35] R. T. Tung, *Phys. Rev. Lett.* **2000**, *84*, 6078.
[36] J. Su, L. Feng, W. Zeng, Z. Liu, *Nanoscale* **2017**, *9*, 7429.
[37] S. M. Song, J. K. Park, O. J. Sul, B. J. Cho, *Nano Lett.* **2012**, *12*, 3887.