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Field Induced Off-State Instability in InGaZnO Thin-Film Transistor and its Impact on Synaptic Circuits

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Charge storage synaptic circuits employing InGaZnO thin-film transistors (IGZO TFTs) and capacitors are a promising candidate for on-chip trainable neural network hardware accelerators. However, IGZO TFTs often exhibit bias instability. For synaptic memory applications, the programming transistors are predominantly exposed to asymmetric off-state biases, and a unique field-dependent on-current reduction under off-scenario is observed which may result in programming current variation. Further examination of the phenomenon is conducted with transmission line-like method and degradation recovery tests, and current reduction can be attributed to contact resistance increase by charge trapping in the source and drain electrode and the channel region. The current decrease is subsequently formulated with a stretched exponential model with bias-dependent parameters for quantitative circuit analysis under off-state degradation. A neural network hardware acceleration simulator is utilized to assess the complicated impact the off-state current degradation could instigate on on-chip trainable IGZO TFT-based synapse arrays. The simulation results generally demonstrate deteriorated training accuracy with aggravated off-state instability, and the accuracy trend is elucidated from the perspective of weight symmetry point.

1. Introduction

The recent emergence of giant neural networks has accentuated the limitation of the conventional von Neumann computing architecture due to the matrix-vector multiplication intensive training and inferencing nature of the networks. With the exponentially increasing number of parameters used in deep neural networks,[1,2] analog computing in crossbar arrays of synaptic memories has risen as a powerful alternative.[3,4] However, for accurate training and inferencing acceleration of neural networks on memory arrays, various synaptic characteristics including controllable linearity and symmetry of weight updates, fast programming, low noise, and high on/off ratio must be simultaneously satisfied.[5] Non-volatile memristors such as phase change random access memory[6–8] or resistive random access memory[9] have the advantage of long data retention time, thus being energy efficient. However, even with the recent enhancements, the emerging memristors often fall short of fulfilling essential performance criteria necessary for attaining optimal training accuracy, especially in terms of linearity and symmetry of weight updates with identical pulses, high on/off ratio, endurance, or device uniformity.[10] Dynamic random access memory-like (DRAM-like) charge storage memory composed of a storage capacitor and Si complementary metal oxide semiconductor (CMOS) transistors has also been suggested for precise training, but its volatile nature stemming from the transistors' large leakage current prevents its usage in large, practical networks.[11,12]

A variety of capacitor and amorphous InGaZnO (a-IGZO) thin-film transistor (TFT) based charge storage synaptic circuits[13–15] have proven to be a prominent solution to this shortage of adequate synapse devices capable of analog in-memory computing. a-IGZO TFT has gained attention as a back-end-of-line (BEOL) compatible transistor with several advantages, offering high mobility[16] for high-frequency operation and also providing extremely low leakage current leading to low power consumption circuits.[17] Thus, the encoding of weight through the charged state of storage capacitors regulated by transistors offers benefits such as controlled weight updates and enhanced endurance in contrast to the atomic-scale conductance modulation mechanism

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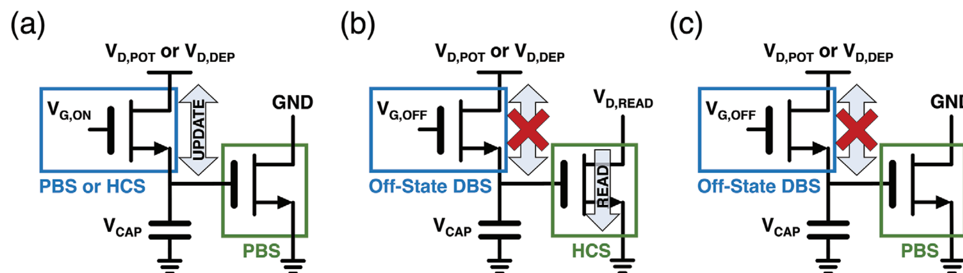

Figure 1. Three operation scenarios and stress modes of charge storage synapse circuits, where the weight is stored as a form of voltage of the storage capacitor. While various configurations of charge storage synapses exist, 2T1C circuit is selected as an example for simplicity. a, b, and c each represents weight update, read, and weight hold operation. The weight update process consists of potentiation (weight increase) and depression (weight decrease), achieved by turning on the update transistor serially connected to the storage capacitor, thereby charging or discharging the capacitor. During the weight update scenario, the update transistor suffers from positive bias stress or hot carrier stress, and the read transistor is under positive bias stress. The read operation is achieved by applying drain-source the electric field to the read transistor, where its gate is connected to the top electrode of the storage capacitor. When the read transistor functions in the linear region, the read current is proportional to the stored voltage. The update transistor is under off-state stress during both read and weight hold scenarios, and the read transistor suffers from hot carrier stress or positive bias stress. $V_{D,\ POT}$ and $V_{D,\ DEP}$ each represent the upper and lower limit of voltage stored in the capacitor (V_{CAP}). $V_{G,\ ON}$, and $V_{G,\ OFF}$ are turn on and off voltage of the update transistor respectively, and $V_{D,\ READ}$ is a small read voltage to induce read current proportional to storage capacitor voltage.

of non-volatile memristors, and longer retention time compared to Si CMOS transistor-based counterparts.

Despite these desirable characteristics, bias instability is one of the major aspects impeding the implementation of various high density, high performance, and power efficient a-IGZO TFT-based circuits.[18,19] IGZO TFTs are known to suffer from bias-induced unstable threshold voltage (V_{th}), subthreshold swing (S.S.), off leakage, or on-current, resulting in significantly degraded circuit performance. The bias stress applied to TFTs can be categorized into four different scenarios: positive bias stress (PBS), hot carrier stress (HCS), negative bias stress (NBS), or off-state drain bias stress (DBS), and understanding each instability phenomenon is imperative for advanced application of IGZO TFT circuits. Unlike digital devices, the synaptic devices not only store data but also perform computations in analog forms, making them more vulnerable to the aforementioned bias instability issue. Therefore, a thorough examination of the impact of bias instability on IGZO TFT-based synaptic circuits is crucial.

There have been abundant studies on the degradation phenomenon and mechanisms of PBS,[20,21] HCS,[22] and NBS.[23,24] However, most investigations were limited to single transistor-level analysis, and few studies were conducted on the TFT stability under the DBS scenario. The influence of off-state instability is particularly pronounced during neural network operation, as the weight updates are infrequent (**Figure 1**). Further, to our knowledge, no analysis of synaptic circuit stability has been conducted, and the instability impact on neural network training accuracy remains unclear.

The purpose of this work was to investigate the unique current reduction after the off-scenario and analyze the degradation impact on neural network training. First, the on-current reduction rate was studied under various off-state bias conditions, and the mechanism of the current decrease was suggested. Second, informed by our experimental findings, we have developed an analytical model that addresses the observed current degradation. The model showed a good agreement with the results obtained from the cycling endurance test conducted on the synapse circuit. Finally, with the proposed model, the off-state impact on neural network training accuracy was explored.

2. Results and Discussions

The stability of the devices under off-state bias stress was evaluated by comparing their transfer and output characteristics before and after the application of bias stress. Changes in the threshold voltage (V_{th}), subthreshold swing (S.S.), and on-current of the transistors were extracted over stress time. The constant current method was used to determine the threshold voltage, where V_{th} was defined as the gate-source voltage at which the drain current is equal to 10^{-10} A. S.S. was determined by S.S. = $d(V_{GS})/d(\log(I_{DS}))$ and on current corresponds to the drain current observed at V_{GS} = 1.5 V and V_{DS} = 0.1 V. **Figure 2a,b** respectively depict the time evolution of the transfer curves of the IGZO TFTs (W/L = 2 μ*m*/5 μ*m*) and the time-dependent behavior in V_{th} and S.S under off-state bias stress. Off-stress of V_{GS} = -2 V, V_{DS} = 1.5 V was applied at room temperature for 10 ks. Previous works generally report an on current decrease caused by a positive shift in V_{th} due to charge trapping at the gate insulator or gate insulator/channel interface.[25,26] However, a noticeable on current decrease to approximately half of its initial value after off-state bias stress was observed, while V_{th} and S.S demonstrated a negligible change in this study.

Since the off-state stability evaluation involved an asymmetric bias condition, forward and reverse output curve measurements were examined to investigate the symmetry of the current degradation. The forward sweep is where the drain electrode during the stress application is used as the drain in output curve measurements. On the contrary, the reverse sweep is where the source electrode during stress application is used as the drain in output curve measurement.[27,28] While the on current was identical for both forward and reverse sweeps prior to off-state stress application, the reverse sweep current showed aggravated degradation after the asymmetric off-stress as depicted in Figure 2c. However, when NBS was applied to the transistor, the current reduction asymmetry was not apparent (Figure 2d). The exclusive observation of asymmetric current degradation and the severe degradation of reverse sweep indicates that the degradation is electric field-dependent, and the magnitude of the applied field

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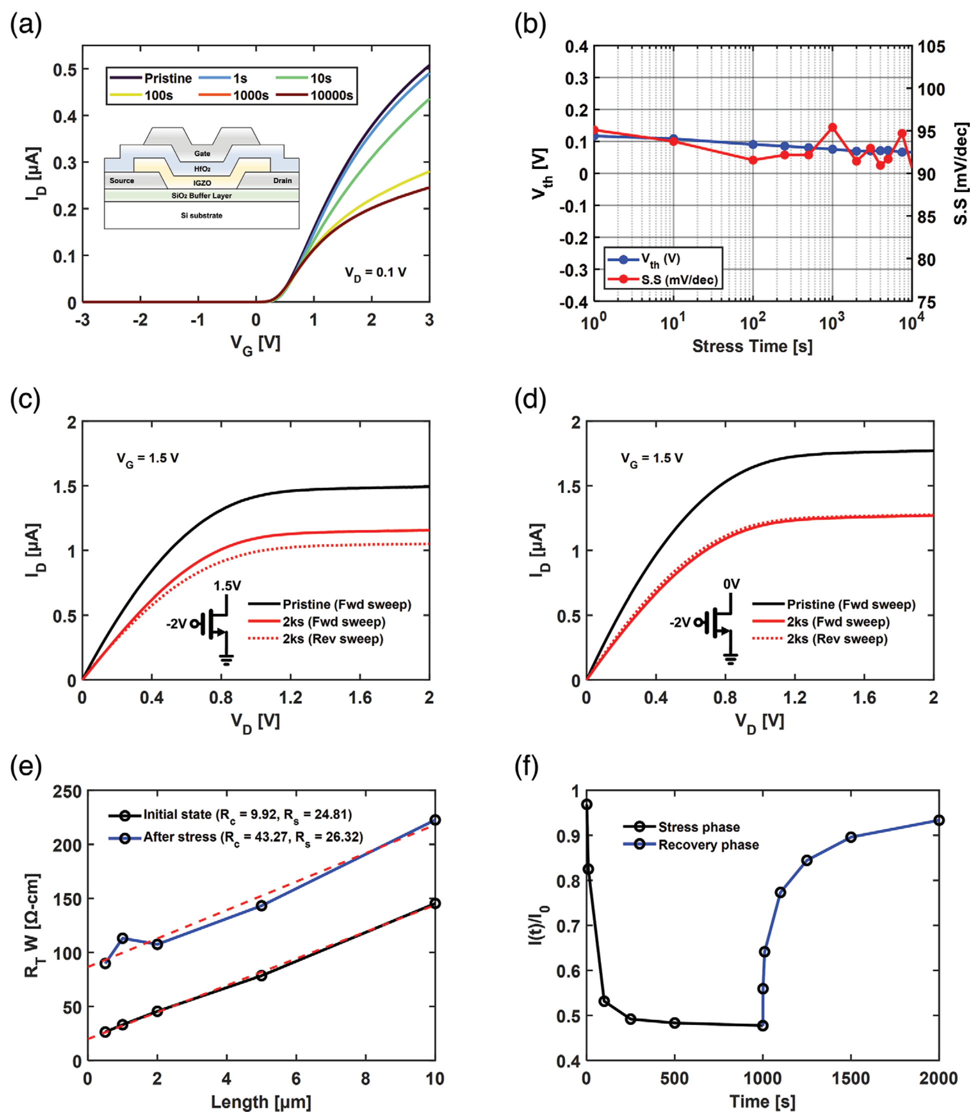

Figure 2. Current degradation under off-bias stress. a) Halved on current was evident in transfer curves post-stress. b) In contrast to previous studies reporting current decrease, threshold voltage and subthreshold swing remained relatively unchanged. c) Contrast in degradation between forward (Fwd) and reverse (Rev) sweeps after asymmetric stress, while no discernible contrast was observed with symmetric off-stress (NBS) as depicted in (d). e) Comparison using transmission line-like method demonstrates consistent linear fit slope and a dramatic increase in y-axis intercept post-stress, indicating contact resistance increase only. f) Reversible current degradation with recovery time of ≈1 ks-scale.

at the source side has a dominant impact on the degradation behavior.

A significant factor contributing to the on current reduction with minimal changes in V_{th} and S.S.[29] could be the shift in contact resistances at the source and drain. To clarify the exact cause of the on current reduction, the contact resistance was extracted by a transmission line-like method before and after the off-state bias stress tests.[30] The bias stress could not be properly applied to the conventional transmission line method (TLM) structure. Therefore, we conducted a transmission line-like method using different transistors of different channel lengths. Although different devices were used, total resistance was linearly proportional to the channel length. As depicted in Figure 2e, the slopes remained consistent regardless of applied stress, while the y-axis intercept after bias stress increased significantly, approximately four times its initial value. This finding suggests that the on-current degradation after off-state bias stress is primarily attributed to an increase in contact resistance rather than a change in the active channel. To further elucidate the mechanism of the abnormal degradation, a stress recovery test was also conducted. The recovery test was conducted by disconnecting the voltage supply to the device (i.e. floating) after completing the bias stress test while measuring transfer curves over time. As illustrated in Figure 2f, the on-current exhibited a rapid recovery within a relatively short period. Restoration exceeding 90% of the initial on-current level was observed within a 1 ks recovery phase. This recovery behavior implies that on-current reduction is more likely due to charge trapping rather than atomic rearrangements,[31,32] such as hydrogen migration. This assertion is also supported by the anticipated time scale of charge

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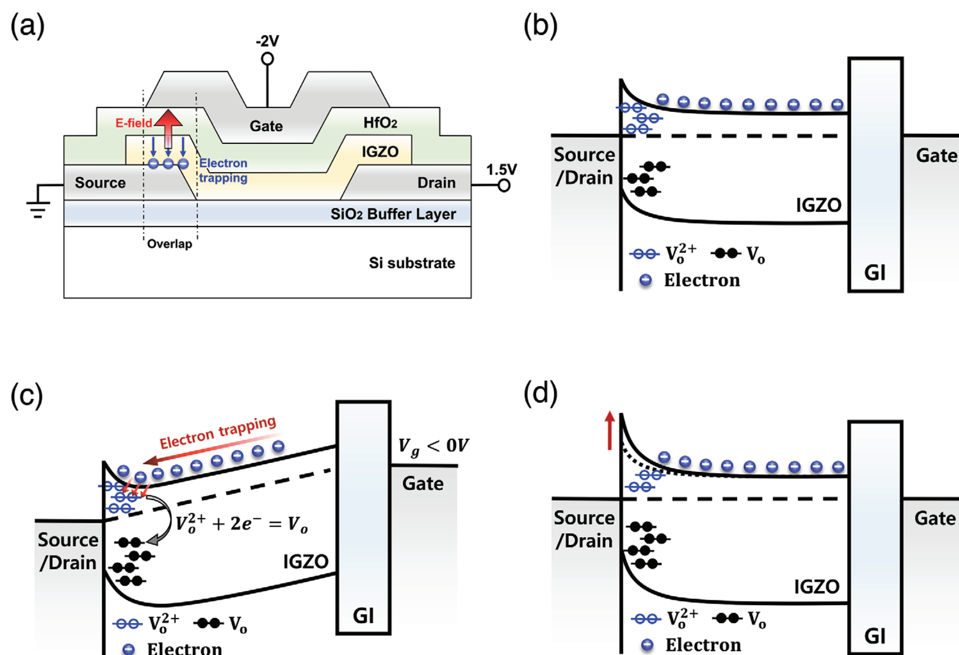

Figure 3. Contact resistance increase originating from charge trapping in channel/electrode interface was suggested as the degradation mechanism. a) Electric field is focused in the overlapped region between the gate and the source/drain electrode. b) The pristine transistor has lowered Schottky barrier, screened by the positively charged oxygen vacancies in the IGZO channel side. c) Off-state bias forces electrons to the interface side and induces occupation of the interfacial states. d) The lack of charged states reduces the screening effect, increasing the Schottky barrier height and impeding carrier injection from the metal electrodes.

trapping and hydrogen migration with positive bias stress test results[33] shown in Figure S2, Supporting Information.

We investigated the underlying mechanism of the degradation to facilitate subsequent device enhancement. From the experimental results, we attributed the abnormal on-current reduction to contact resistance increase by charge trapping in the interface between the IGZO channel layer and the metal electrodes. The structure of the IGZO TFTs studied in this research has an overlap between gates and source/drain, where a large electric field is applied under the off-state bias conditions. As shown in **Figure 3a**, electron trapping at the interface could be induced by the applied field. It has been reported that a Schottky barrier can be formed at the IGZO-tungsten contact.[34] The Schottky barrier height (SBH) of the IGZO/W can be predominantly determined by the density of charged states at the IGZO side of the interface.[35–43] A relatively low SBH should be formed in the pristine transistor attributed to the high density of charged states, and possibly charged oxygen vacancy (V_O^{2+}) states.[44–46] With the application of the off-state bias stress, the electric field toward the gate electrode direction induces electron trapping to V_O^{2+} at the interface, and the transition occurs from ionized V_O^{2+} to neutralized V_O[47] (Figure 3b). As a result of the occupation of the charged states, the shielding effect is gradually reduced and the barrier is pinned to a higher energy level, increasing the SBH which results in higher contact resistance (Figures S3–S5 and Table S1, Supporting Information).

The current reduction caused by IGZO TFT instability can significantly impact the performance of IGZO TFT-based VLSI circuits. Analyzing this impact is simpler for digital circuits than for analog circuits. For instance, when using IGZO TFTs in digital memories like DRAM, there are only two bias scenarios (data high or low), and the impact of on-current reduction is simply slower circuit operation. However, in synaptic circuits as in Figure 1, the update transistors experience an infinite number of bias conditions because the stored synaptic weight is analog, not digital. This complicates the prediction of circuit performance stability since IGZO TFT instability is highly dependent on electric field or bias conditions. Moreover, the on-current reduction in synaptic circuits not only alters the amount of weight update but also affects the weight update symmetry,[48] which can significantly impact the on-chip training accuracy of deep learning models. To understand this rather complex phenomenon in IGZO TFT-based synaptic circuits, we developed a detailed behavioral current reduction model that captures the time and voltage dependence of the instability. This model was integrated into a simulator for analog in-memory computing systems to study the bias instability impact on neural network training accuracy.

The stretched exponential function has been often utilized to model the threshold voltage shift by charge trapping in previous reliability studies.[49,50] Since the contact resistance increase was attributed to charge trapping at the channel/electrode interface, we used a modified stretched exponential function with a saturation point to fit the current reduction (Equation 1). The current reduction ratio was well-fitted with the proposed model, and the instability behavior was well captured for all stress conditions (**Figure 4a**). The current reduction behavior can be represented using three stress parameters, τ, β, and C. τ is the time constant of the instability phenomenon, and a higher τ value means slower current reduction. C is the saturation point and may be related to the maximum SBH achieved by reduced screening due

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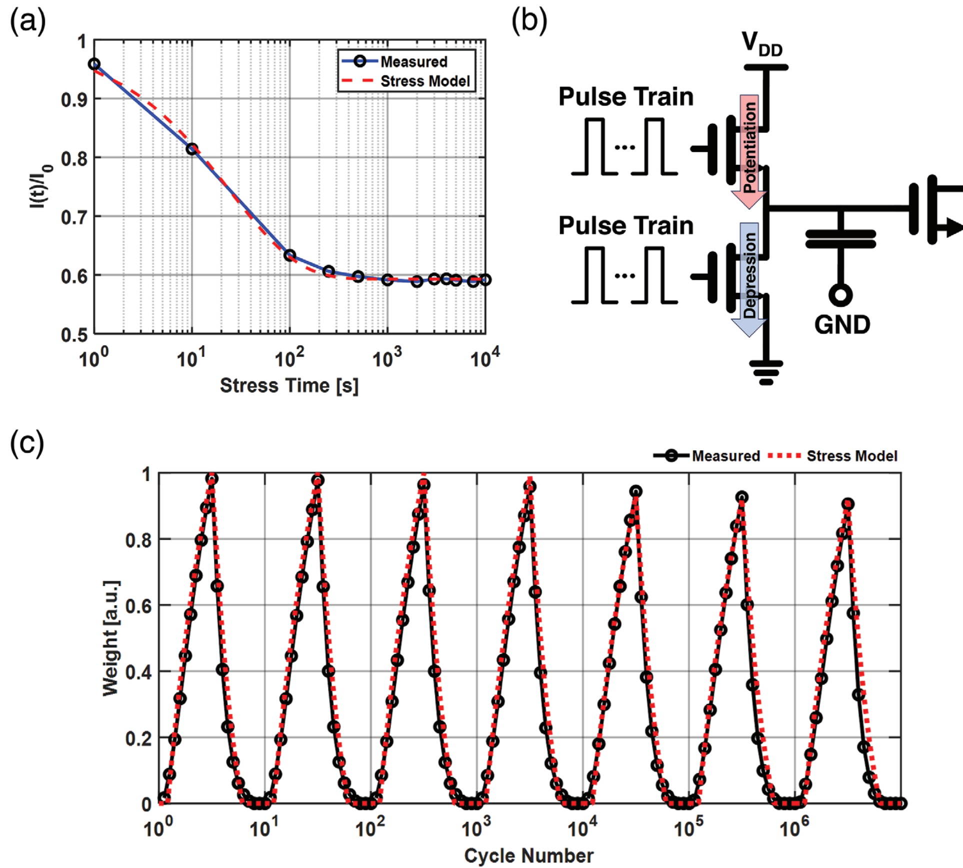

Figure 4. Device modeling and model validation on synapse experimental data. a) Time-dependent on-current reduction was well-fitted with the stretched exponential function with a saturation point for all stress conditions. b) Schematic of the synapse circuit, which consists of two update transistors (potentiation and depression) and a read transistor. Each node of the transistors has well-defined voltages, and the update current only flows in one direction. c) The gradual maximum weight decrease during cycling endurance test is well represented by the proposed stress model. V_{DD} =1.5 V, $V_{G, ON}$ = 1.5 V, $V_{G, OFF}$ = -2 V, and $V_{D, READ}$ = 0.2 V were used for synaptic circuit cycling endurance test, and values of τ and β from unit transistor experiments were used to fit the measured data points. A slightly higher C value of 0.9 was utilized instead of 0.6 from unit transistor off-stress tests.

to trapping. Finally, β is the stretch parameter and may represent trapping modes or conduction mechanisms at the interface barrier. A thorough study of the physical meaning of the parameters is out of the scope of this work and should be studied in future works.

The bias dependence of each parameter was experimentally extracted by measuring the degradation at different gate and drain biases. β and C were considered relatively consistent regardless of applied off-state stress, and τ showed exponential dependence to both gate and drain biases. The fitted result is as Equation (2). Applying more negative gate bias and positive drain bias resulted in faster degradation, and the gate-source off-voltage showed more influence on the time constant (Figure S6, Supporting information). Combining Equation (1) and Equation (2), a simplified stress model could be formulated.

$$\frac{I(t)}{I_0} = (1 - C) \times exp(-(t/\tau)^{\beta}) + C \tag{1}$$

$$\tau(V_{GS}, V_{DS}) = \tau_0 \times exp(k_1 V_{GS}) \times exp(k_2 V_{DS}) \tag{2}$$

Although the proposed exponential relations have a good representation of the measured data, validation must be preceded before the generalization of the model. Since the stability analysis is a destructive experiment, only a few data points could be acquired in the whole off-bias and time-space. Therefore, attempts were made to predict the off-state instability-related phenomenon in actual device operation. The simulation was done on an IGZO charge storage synapse circuit with two updated transistors and a read transistor for the simplicity of model application (Figure 4b). In this synapse circuit, all nodes of the transistors have well-defined voltages. Furthermore, current only flows in one direction for all transistors, and the forward-reverse asymmetry could be disregarded.

During the continuous potentiation-depression of the synapse circuits (cycling endurance test), a decreasing trend of maximum weight was observed. As the off-state instability is thought of as the dominant source of the cycling degradation behavior, it should be explainable with the proposed off-state instability model. Applying the degradation model on the NMOS drain current equation weight update model, the complicated weight-dependent stress scenario could be simulated. As the result

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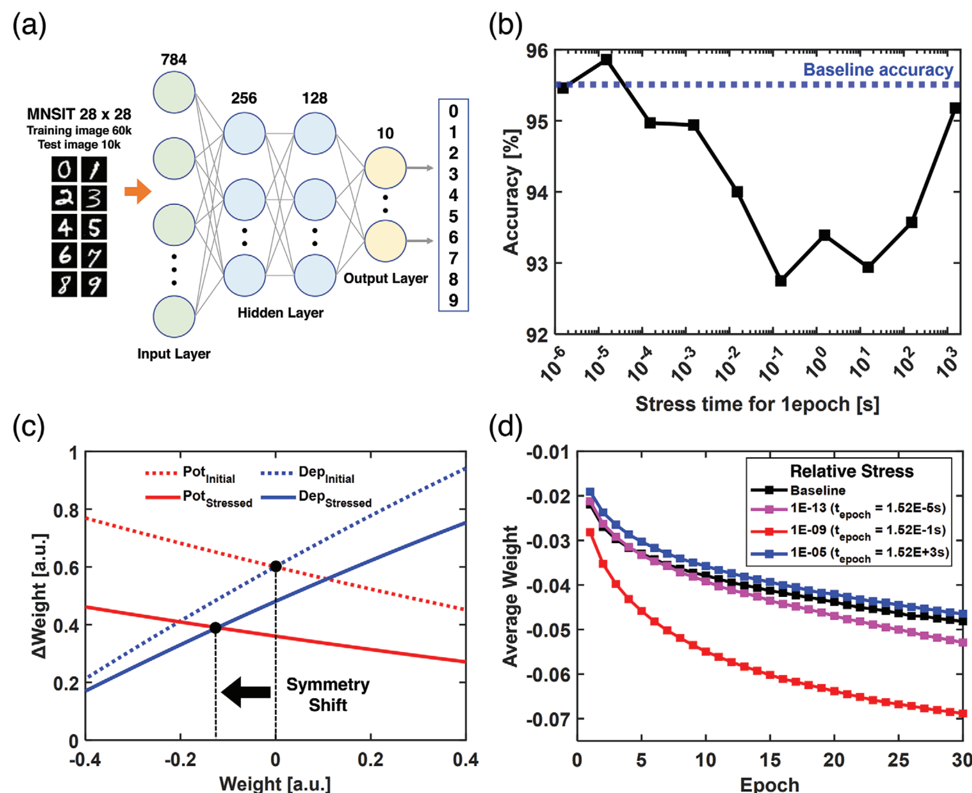

Figure 5. Stress model integrated neural network training simulation results. a) Multi-layer perception network with two hidden layers was used to train the MNIST handwritten digit dataset. b) Maximum training accuracy trend to the approximate off-stress time per single epoch of training. Each stress condition was simulated for 30 training epochs. The accuracy predominantly deteriorated until a certain degree of instability, then showed a recovery for longer relative stress time. c) The difference in current reduction between potentiation and depression transistors causes a shift in the symmetry point of weight updates, which is the main factor of accuracy deterioration (V_{DD} = 2 V, V_{off} = -2 V, V_{CAP} =1 V). d) Average weight tends to decrease compared to the ideal hardware baseline (relative stress 1E-13, 1E-09). If the degradation is severe enough (relative stress 1E-05), the current reduction is already saturated, and the average weight lags the baseline due to reduced update currents.

shown in Figure 4c, the cycling weight decrease phenomenon was well represented with the proposed degradation-included weight update model. The stress parameter used to fit the measurement data was similar to that of the extracted values from the unit transistor experiment, with only a slight difference in the C value. With this congruence of experimental result and the proposed model, further complex on-chip training acceleration analysis could be conducted.

Network scale on-chip training simulation was conducted on a customized aihwkit simulation tool,[51] which is an open-source hardware neural network simulator provided by IBM. The simulation was done on a simple multi-layer perceptron (MLP) model with two hidden layers (**Figure 5**a). The stochastic gradient descent algorithm was utilized for the optimizer, and the effect of stress was applied with the relative stress which was defined as the ratio of time required for inference and backpropagation and the τ_0 value ($t_{stress,\ relative} = (t_{inference} + t_{backpropagation})/\tau_0$). More information on the training simulation can be found in the Table S2 (Supporting Information).

The simulation results show an accuracy deterioration to a certain point of off-state instability and recovery when the stress becomes critically severe (Figure 5b). While the gradual reduction of programming current could bring some degree of positive impacts, acting as some variant of learning rate scheduler, the deviation of the weight 0 from the weight symmetry point seems to be the dominant factor in the training accuracy.[52] The weight update symmetry point is the weight where a single potentiation and depression programming pulse induces an identical magnitude of weight change. The weights tend to converge to the symmetry point if the stochastic weight update scheme[53] is used, and setting the symmetry point as the weight 0 is crucial for achieving high training accuracy.[48]

The weight 0 is physically represented with a storage capacitor voltage of $V_{DD}/2$ and potentiation transistors are generally exposed to harsher gate-source negative field stress if identical off-voltages are applied. Since the gate-source side field stress is the dominant factor in determining the degradation speed, potentiation transistors suffer from more severe current reduction compared to depression transistors. This leads to relatively enhanced depression, and the weight symmetry point is formed in a lower-weight region (Figure 5c). The extra negative-direction force during weight update hinders weight convergence to answer weights, leading to a gradual deterioration of training accuracy. This is verified by the stress-dependent decrease of average weight values as described in Figure 5d. On the other hand, if the degradation is rapid enough, both update transistors are already degraded to the saturation point, thereby maintaining the symmetry point due to identical ratios of current decrease. This is well

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illustrated in Figure 5d, where the weight evolution lags the non-degraded case due to the decreased update amount per applied programming pulse. Consequently, there is a restoration of training accuracy, while the slight accuracy decrease compared to the no-stress baseline accuracy can be attributed to a less-optimized learning rate, i.e., deviation from optimal learning hyperparameter.

This field-induced instability is an obstacle in transistor dimension scaling, as smaller devices might lead to harsher focused electric fields and pronounced contact resistance-induced short-channel effects.[54] While initial deliberate degradation saturation may mitigate some effects of the current reduction, this approach would result in slower training and require long initialization periods for each training event. Hence, a fundamental solution of this instability behavior must be followed. Alteration of the transistor structure from bottom contact to top contact may alleviate the field-focusing effect, and various contact engineering methods should be explored to prevent contact resistance increase.

3. Conclusion

IGZO TFT-based synaptic circuit, which is a promising candidate for neural network acceleration, lacks reliability study and we have conducted tests on the dominant off-state stress scenario. After stress, an unusual on-current reduction was observed, and it was attributed to charge injection barrier height increase by charge trapping at the electrode/channel interface. The current reduction was modeled for advanced analysis and then applied to a neural network simulator to evaluate the TFT instability effect on training accuracy. It was concluded from the simulation results that the shift in symmetry point provoked by varied degradation of potentiation and depression transistors acted as the primary factor in the deterioration of training accuracy. Mitigation methods such as an alternative transistor structure or optimal source/drain electrode material must be researched for chip-level implementation of IGZO transistors. Overall, this work should direct future research by providing a framework for TFT instability analysis and circuit level performance evaluation, its significance amplified with the emerging novel transistor structures[55] aimed at reducing circuit area.

4. Experimental Section

Device Fabrication: All transistors were fabricated following the identical step as in the previous work.[15] 10 nm thick InGaZnO (In:Ga:Zn = 1:1:1) thin film was sputtered followed by tungsten source and drain patterning on thermal silicon oxide. 10 nm thick atomic layer deposited HfO_2 was used as the gate insulator and the capacitor dielectric material. Lastly, a tungsten gate electrode was deposited and patterned. Transistors of 2 μm wide, 5 μm long channel was used as a reference device.

Device Characterization: All experiments were conducted in a dark box and air ambiance. Stress application and transistor performance evaluation were conducted with a B1500A semiconductor parameter analyzer. A microcontroller unit (MCU) and custom PCB peripheral circuit were utilized for synapse device operation. Detailed device operation schemes can be found in the supporting information.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

capacitor-based memory, contact resistance, InGaZnO (IGZO), off-state stress, on current reduction

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