Single-electron transistor based on a silicon-on-insulator quantum wire fabricated by a side-wall patterning method

D. H. Kim, S.-K. Sung, J. S. Sim, K. R. Kim, J. D. Lee, B.-G. Park, B. H. Choi, S. W. Hwang, and D. Ahn

---

Articles you may be interested in

Single-electron transistors based on self-assembled silicon-on-insulator quantum dots
Appl. Phys. Lett. **96**, 142108 (2010); 10.1063/1.3383235

Single-electron transistor structures based on silicon-on-insulator silicon nanowire fabrication by scanning probe lithography and wet etching
J. Vac. Sci. Technol. B **20**, 2824 (2002); 10.1116/1.1523017

Fabrication of single-electron tunneling transistors with an electrically formed Coulomb island in a silicon-on-insulator nanowire
J. Vac. Sci. Technol. B **20**, 1410 (2002); 10.1116/1.1491551

Single-electron tunneling in highly doped silicon nanowires in a dual-gate configuration
J. Appl. Phys. **89**, 8159 (2001); 10.1063/1.1368399

Single-electron transistors fabricated from a doped-Si film in a silicon-on-insulator substrate
Appl. Phys. Lett. **72**, 795 (1998); 10.1063/1.120896

Single-electron transistor based on a silicon-on-insulator quantum wire fabricated by a side-wall patterning method

D. H. Kim, S.-K. Sung, J. S. Sim, K. R. Kim, J. D. Lee, and B.-G. Park[a]
Inter-University Semiconductor Research Center (ISRC) and School of Electrical Engineering, Seoul National University, San 56-1, Shinlim-dong, Kwanak-gu, Seoul 151-742, Korea

B. H. Choi, S. W. Hwang, and D. Ahn
Institute of Quantum Information Processing and Systems (iQUIPS), University of Seoul, 90 Jeonnong-dong, Dongdaemun-gu, Seoul 130-743, Korea

We propose and implement a promising fabrication technology for geometrically well-defined single-electron transistors based on a silicon-on-insulator quantum wire and side-wall depletion gates. The 30-nm-wide silicon quantum wire is defined by a combination of conventional photolithography and process technology, called a *side-wall patterning* method, and depletion gates for two tunnel junctions are formed by the doped polycrystalline silicon sidewall. The good uniformity of the wire suppresses unexpected potential barriers. The fabricated device shows clear single-electron tunneling phenomena by an electrostatically defined single island at liquid nitrogen temperature and insensitivity of the Coulomb oscillation period to gate bias conditions. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1421081]

Single-electron transistors (SETs) have been extensively studied in with the hope of applying them to ultralarge-scale integrated circuits due to their high integration density and low power consumption. Moreover, the operation temperature of silicon-based SETs has been increased to room temperature,[1,2] and their application to logic circuits such as inverters[3] and exclusive-OR gates[4] operating at 20 K has already been reported. Although the combination of Si technology and the novel structure makes further miniaturization of the Si island possible, reproducible fabrication technology and controllable device characteristics are still being sought by many researchers for realistic application. In the case of most single-electron tunneling phenomena in Si nanosize channels, the formation mechanisms of tunnel junctions and islands have not been clarified. Although localized electron states by impurity potential or trapped charge,[5,6] channel depletion in the constricted part,[7] thickness fluctuation of the gate oxide or Si film,[2] the quantum confinement effect,[8,9] or electron-beam irregularity[10] are considered the origin of tunnel junctions, there have been no obvious artifacts which form tunnel junctions and islands.

We feel that it is worth considering the reproducible structure of Si based SETs whose electron transport is controlled by a geometrically well-defined Si island in order to optimize their device characteristics (i.e., voltage gain, operation voltage, switching speed, and integration density) and to estimate the usefulness of their future room temperature counterparts.

In this letter, we propose and implement a promising fabrication technology, called a *side-wall patterning* method, for SETs based on a silicon-on-insulator (SOI) quantum wire and an electrostatically defined island beyond the limit of lithography resolution. Operation of fabricated SETs with total capacitance of 2.86 aF is demonstrated at 77 K.

The devices were fabricated on the $4 \times 10^{15} \, \text{cm}^{-3}$ p-doped 60-nm-thick top layer of a SOI wafer prepared by separation by implanted oxygen. This top layer is separated from the Si substrate by a 415-nm-thick buried oxide. Si quantum wires are formed by the side-wall patterning method, which is key to fabrication.[11,12] Figure 1 shows schematics of the process sequence of the side-wall patterning method. It consists of six major steps. First, a 40-nm-thick oxide is deposited on the top layer, and then a 80-nm-thick nitride layer is deposited on the SOI wafer at 750 °C and patterned by conventional photolithography. Next, amorphous silicon is deposited at 550 °C using a low pressure chemical vapor deposition system and annealed at 800 °C for 30 min, so that the edge of the nitride layer is fully covered. Then, the amorphous silicon layer is anisotropically etched using Cl_2 reactive-ion plasma until the whole layer is removed except the part at the corner of the edge of the nitride layer. This amorphous silicon strip serves as an etch mask for definition of the Si quantum wire. Subsequent chemical etch-
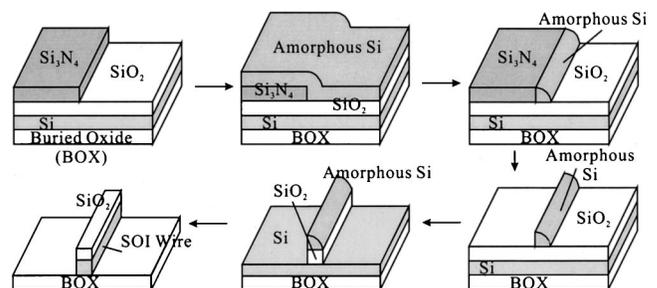

FIG. 1. Schematics of the process sequence of the side-wall patterning method. Using the good selectivity in reactive-ion plasma between Si and SiO_2, a 30-nm-wide amorphous Si side-wall pattern is transferred into a SOI layer.

[a]Author to whom correspondence should be addressed; electronic mail: bgpark@snu.ac.kr
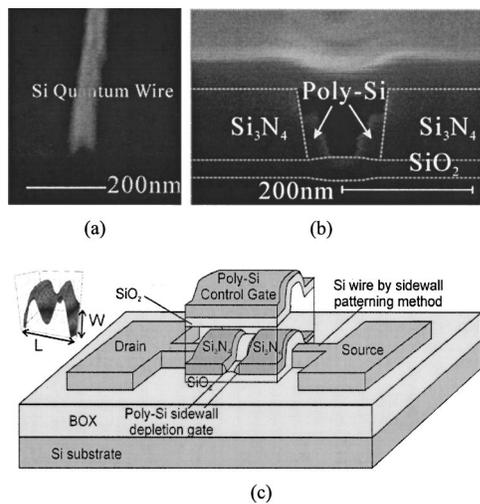
(a)   (b)

(c)

FIG. 2. (a) Scanning electron microscope image of a SOI quantum wire patterned by the side-wall patterning method after gate oxidation. (b) Scanning electron microscope image of the cross section of the fabricated device. Two polysilicon side-wall depletion gates formed at the edge of the nitride groove. The width of the side-wall gate and the separation between the two side-wall gates S_{sg} are 30 and 37 nm, respectively. (c) Final device schematics. The inset shows the electron potential profile of a SOI wire calculated by three-dimensional device simulation. The simulation result showed that the barrier height is 100 meV when S_{sg} is 37 nm, V_{cg} is 1 V, V_{sg} is −0.1 V, and V_{bg} is 14 V.

ing of the nitrides in H_3PO_4 solution, anisotropic etching of the oxides in CHF_3/CF_4 reactive-ion plasma, and anisotropic etching of Si in Cl_2 reactive-ion plasma form a Si quantum wire.

After stripping off the remainder of the oxide layer on the Si wire in HF solution, 30 nm of oxide is subsequently grown in dry O_2 at 950 °C to form the side-wall depletion gate oxide. Figure 2(a) shows a scanning electron microscope image of a Si wire patterned by the side-wall method after the gate oxidation. Very uniform 30-nm-wide Si wires surrounded by gate oxide with no irregularities can be created by this method.

For the electrostatically defined Si island, two polycrystalline silicon side-wall depletion gates are subsequently formed on a Si quantum wire as follows. The 80-nm-thick nitride layer is deposited on the side-wall depletion gate oxide, and then a 100-nm-wide groove is defined in the nitride layer by poly-methylmethacrylate electron-beam resist. After growth of 8 nm of oxide in dry O_2 at 800 °C for damage curing, during which the gate oxide becomes thicker locally only under the nitride groove, two polysilicon sidewalls are formed around the edge of the nitride groove by the deposition and etching of 35-nm-thick phosphorus-doped polysilicon, shown in Fig. 2(b). These side-wall depletion gates wrap around the quantum wire in order to control the potential within the Si quantum wire. After deposition of the control gate oxide, subsequent formation of the polysilicon control gate, ion implantation into regions of the source/drain and the control gate, and the formation of aluminum electrodes were performed. This sequence is compatible with conventional complementary metal–oxide–semiconductor process technology. The final width of the SOI wire W_{ch}, its thickness, the thickness of the control gate oxide, and the
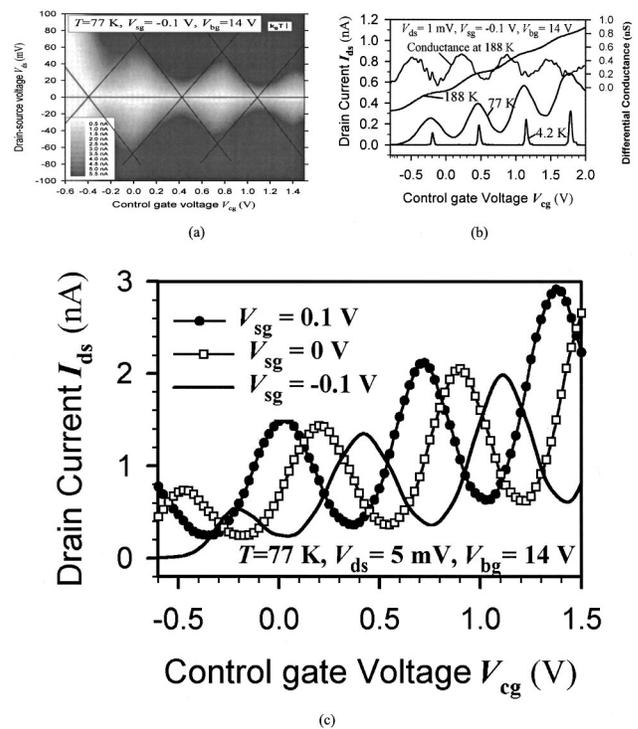

(a)   (b)

(c)

FIG. 3. (a) Contour plot of the drain current I_{ds} as a function of V_{cg} and V_{ds} at 77 K. (b) $I_{ds}-V_{cg}$ characteristics as a function of the temperature. ΔV_{cg} is constant at various temperatures, and the conductance oscillation is clearly observed even at 188 K. (c) $I_{ds}-V_{cg}$ characteristics as a function of V_{sg} at 77 K. ΔV_{cg} of 675 mV is constant at fixed V_{sg}. On the other hand, ΔV_{cg} is nearly unchanged and the current level decreases as V_{sg} increases in the negative direction.

separation between two side-wall gates S_{sg} is controlled to 23, 45, 60, and 37 nm, respectively.

Figure 2(c) shows a schematic diagram of the devices fabricated. The electron channel in the Si wire is induced by biasing the back gate V_{bg}. Two tunnel barriers are induced by biasing the polysilicon side-wall depletion gates V_{sg}, and the potential in the Si island is controlled by biasing the polysilicon top control gate V_{cg}.

The device was characterized by a precision semiconductor parameter analyzer (HP 4155A). Figure 3(a) shows the drain current I_{ds} measured at 77 K as a function of the control gate voltage V_{cg} and the drain–source voltage V_{ds}. The Coulomb gap is clearly modulated by V_{cg}, and Coulomb gap voltage of 104 mV was observed in the blockade region. Clear multiple Coulomb oscillation peaks with periodicity ΔV_{cg} of 675 mV can be seen in the $I_{ds}-V_{cg}$ curves. From the results measured, the average capacitances are evaluated as follows: control gate capacitance $C_{cg}=0.24$ aF, drain tunnel junction capacitance $C_d=1.32$ aF, source tunnel junction capacitance $C_s=1.30$ aF, and total capacitance of quantum dot $C_{total}=2.86$ aF. If we assume the island has a spherical shape, the C_{total} corresponds to the self-capacitance of a sphere with a diameter of 13 nm. Therefore, the effective size of the quantum dot is estimated to be smaller than 13 nm, which is essentially shrunken by the field effect of V_{sg}. The C_{cg} of 0.24 aF corresponds to 50% of the gate capacitance obtained by approximation of the two parallel electrodes of area $W_{ch} \times S_{sg}$.

When S_{sg} was controlled to 37, 88, 134, and 185 nm by varying the width of the nitride groove, ΔV_{cg} was 675, 210,

123, and 80 mV, respectively. This suggests that the single-electron phenomena observed can be attributed to the two electrically induced tunnel junctions and the single Si island between them. The evaluated C_{total} of 2.86 aF also corresponds to a single-electron charging energy of 28 meV and is consistent with operation at 77 K. Figure 3(b) shows the $I_{ds}-V_{cg}$ curves as a function of the temperature. The conductance oscillation is clearly observed even at 188 K, and no splitting of the oscillation peak is observed at 4.2 K. Considering that recently demonstrated SETs based on doped Si have shown complicated behavior such as multiple periods from multiple tunnel junctions[13] and unpredictable splitting of the oscillation peak from the discrete energy level in a dot,[14] our devices showed reliable single dot characteristics according to the geometrical design, which is an advantage for practical integration. Reliable single dot characteristics of Si based SETs have already been demonstrated by Takahashi *et al.*,[15] but our devices have the advantage that the side-wall gates can be used for control of the peak position.

Figure 3(c) shows the $I_{ds}-V_{cg}$ curve as a function of V_{sg} at 77 K. At fixed V_{sg}, ΔV_{cg} of 675 mV is maintained in sweeping V_{cg}. This implies that the effective size of the island is predominantly controlled by geometrical factors (i.e., W_{ch} and S_{sg}) and is not influenced by the gate bias condition of V_{cg}. At negative V_{sg}, the tunneling resistance increases, but the Coulomb oscillation period seldom varies. On the other hand, the position of the Coulomb oscillation peak is controlled by V_{sg}, which is attributed to sharing of the island charge between the control gate and side-wall gate, as shown in Fig. 3(c).

We now consider this insensitivity of ΔV_{cg} to gate bias conditions. In general, SETs with depletion gates[16,17] have the drawback that the switching performance is seriously degraded as the gate bias voltage increases, so a small number of peaks are observed only in the subthreshold region. This is due to the complicated competition between electric fields of various gates. Positively large control gate bias alleviates the barrier by the depletion gate, so the oscillation peak vanishes at constant temperature.[17] Moreover, the slight variation of the oscillation period reflects not only the depletion width varied by the depletion gate bias[18] but also the discrete electron energy level separation.[19] SETs based on doped polysilicon nanowires also show a change of a factor of a few times at the same device.[20]

In our system, however, the polysilicon side-wall depletion gate wraps the Si channel three dimensionally, and the top control gate becomes further separated from the Si wire than the side-wall depletion gates. So, the shape of the tunnel barriers is strongly controlled by V_{sg}, and the potential in the island is independently controlled by V_{cg} at fixed V_{sg}. Weaker coupling with V_{cg}, however, means a small gain in the SETs, which is 0.185 as shown in Fig. 3(a). Thus, the thickness of the control gate oxide and SOI layer, the width of the side-wall gate, and S_{sg} must be further optimized for the high operating temperature, the high gain, and the island shape to be immune to bias conditions. In the case of varied V_{sg} with fixed V_{cg}, the variation of the depletion width reflects the size of the deviation of the Si island.

But, as V_{sg} is varied from 0.1 to -0.1 V, the V_{cg} at the oscillation peak increases. In other words, at the current's peak, expansion of the depletion region is compensated for by an increase of V_{cg}, and the size of the island remains more or less the same, as can be seen in Fig. 3(c). Therefore, the fabrication technology proposed can design the size of the island precisely by controlling W_{ch} and S_{sg}, which depend not only on the lithographical limitations but also on control of the chemical vapor deposition and the plasma etching process.

In conclusion, we have proposed and implemented a promising fabrication technology for SETs based on a uniform SOI wire using conventional lithography and processing technology, called the *side-wall patterning* method. The devices fabricated show clear single-electron tunneling phenomena by an electrostatically well-defined single island and two tunnel junctions at liquid nitrogen temperature and advantages that are applicable to practical integration of SETs, such as the insensitivity of the Coulomb oscillation period to gate bias conditions and the formation mechanism of tunnel junctions and the Si island by the conventional process technology.

[1] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, Electron. Lett. **31**, 136 (1995).

[2] K. Uchida, J. Koga, R. Ohba, and A. Toriumi, Tech. Dig.-Int. Electron Devices Meet. 863 (2000).

[3] Y. Ono, Y. Takahashi, K. Yamazaki, M. Nagase, H. Namatsu, K. Kurihara, and K. Murase, Appl. Phys. Lett. **76**, 3121 (2000).

[4] Y. Takahashi, A. Fujiwara, K. Yamazaki, H. Namatsu, K. Kurihara, and K. Murase, Appl. Phys. Lett. **76**, 637 (2000).

[5] R. A. Smith and H. Ahmed, J. Appl. Phys. **81**, 2699 (1997).

[6] M. Sanquer, M. Specht, L. Ghenim, S. Deleonibus, and G. Guegan, Phys. Rev. B **61**, 7249 (2000).

[7] H. Ishikuro and T. Hiramoto, Appl. Phys. Lett. **71**, 3691 (1997).

[8] H. Ishikuro and T. Hiramoto, Appl. Phys. Lett. **74**, 1126 (1999).

[9] K. Shiraishi, M. Nagase, S. Horiguchi, H. Kageshima, M. Uematsu, Y. Takahashi, and K. Murase, Physica E (Amsterdam) **7**, 337 (2000).

[10] L. Zhuang, L. Guo, and S. Y. Chou, Appl. Phys. Lett. **72**, 1205 (1998).

[11] R. S. Burton and G. M. Grivna, U.S. Patent No. 5,667,632 filed (16 September 1997).

[12] S.-K. Sung, Y.-J. Choi, J. D. Lee, and B.-G. Park, J. Korean Phys. Soc. **35**, 693 (1999).

[13] R. Augke, W. Eberhardt, C. Single, F. Prins, D. Wharam, and D. P. Kern, Appl. Phys. Lett. **76**, 2065 (2000).

[14] H. Ishikuro, T. Fujii, T. Saraya, G. Hashiguchi, T. Hiramoto, and T. Ikoma, Appl. Phys. Lett. **68**, 3585 (1996).

[15] Y. Takahashi, H. Namatsu, K. Kurihara, K. Iwadate, M. Nagase, and K. Murase, IEEE Trans. Electron Devices **43**, 1213 (1996).

[16] Y. Satoh, H. Okada, K. Jinushi, H. Fujikura, and H. Hasegawa, Jpn. J. Appl. Phys., Part 1 **38**, 410 (1999).

[17] D. H. Kim, J. D. Lee, and B.-G. Park, Jpn. J. Appl. Phys., Part 1 **39**, 2329 (2000).

[18] H. Matsuoka, T. Ichiguchi, T. Yoshimura, and E. Takeda, Appl. Phys. Lett. **64**, 586 (1994).

[19] A. Dutta, S. Oda, Y. Fu, and M. Willander, Jpn. J. Appl. Phys., Part 1 **39**, 4647 (2000).

[20] A. C. Irvine, Z. A. K. Durrani, H. Ahmed, and S. Biesemans, Appl. Phys. Lett. **73**, 1113 (1998).