Master's Thesis

Relaxation Oscillator Based CMOS Temperature Sensor with Capacitor Flipping

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Changyong Shin

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Approved by

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Abstract

Temperature can be a factor that affect any kind of system so measuring and predicting temperature is necessary for stable system. In bio-signal acquisition or artificial viscera, body is vulnerable to heat, so monitoring temperature is necessary. Not only human's body but also electronic device and chip are vulnerable to heat. For overheating protection applications, temperature must be monitored. In environmental and industrial system, temperature is important factor. For better performance and preventing accident, temperature must be adjusted stably. If temperature changes suddenly, we must observe it and adjust temperature properly.

Method for measuring temperature is so various. In real life, people mostly use mercury thermometer. The characteristic of temperature dependence is utilized. However, it is hard to communicate with the electronic device. That's why we need smart temperature sensor. Temperature sensor needs to be integrated in electronic device.

Most of the passive devices show temperature dependency. Using that characteristic, electronic smart temperature sensor is invented. Resistors, BJTs, MOSFETs, diodes, are the examples. It has its pros and cons so selection should be considered smartly. Resistor is power effective, but it wastes area, and temperature dependency is poor so multi-point trimming is necessary. MOSFET is power effective, but its temperature dependency is poor, so we need additional technique that can compensate non-linearity. However, BJT still shows poor temperature dependency.

If we observe the base-emitter voltage with change of temperature, curvature is observed. Nevertheless, it shows better dependency than others Generally, BJT is widely utilized as smart temperature sensor because of its linearity. However, it shows better performance relatively with other passive devices, but it still lacks accuracy and dependency. That's why solution for reducing non-linearity is significant. Trimming or calibration technique is needed for that problem. In circuit, trimming can be done with adjusting biasing current or voltage. However, it can be a burden and the production cost increases. Today's trend does calibration or trimming at the back stage digitally. It gives simplicity and cost effective.

Not only the sensing type but also analog circuit itself can be error source. In the layout, mismatch of the devices and the parasitic capacitance can degrade the performance of circuit Amplifier and comparator can be affected by offset. Mismatch of the current mirror can give the incorrect bias current ratio. To reduce these errors, many efforts are done. Many techniques are utilized in the circuit. Chopping can mitigate the error caused by offset. DEM(Dynamic Element Matching) can reduce the error of current source mismatch. Various techniques are included in this CMOS smart temperature sensor.

Readout circuit as well as bias circuit is significant. Input type can be current, voltage, time, frequency.

Readout circuit can also be many kinds of circuits. ADC(Analog-to-digital converter), FDC(Frequency-to-digital converter), TDC(Time-to-digital converter) can be connected to get a output. Each readout circuits include their own pros and cons, so we must choose the readout circuit with our expected spec.

Calibration and trimming can be important factor in CMOS temperature sensor. It has direct relationship with the production cost. The more calibration and trimming is needed, the much money is payed. Effort to reduce calibration point or simplifying trimming is in progress.

Chapter 1. Introduction

To begin with, CMOS smart temperature sensors show better performance compared to conventional temperature sensors. However, it has problem : Relatively poor accuracy. Various techniques will be discussed to improve accuracy. In the state of art, inaccuracy of ±0.1℃ over -40~125℃ temperature sensor is achieved.

In chapter 1, the motivation will be discussed. Then, basic principles of CMOS temperature sensors will be explained. Finally, short overview of previous work will be described.

1.1 Motivation and Objectives

Sensor is defined as ‘A device, module, machine, or sub-system whose purpose is to detect events or changes in its environment and send the information to other electronics, frequently a computer processor.’ There can be many things to sense environmental things. (ex : temperature, proximity, gas, light, humidity etc.) Temperature is a significant factor in many fields from simple household machines to complex industrial system monitoring. Temperature sensors must be integrated in coffee machine, heating system. For better agriculture, temperature must be adjusted within proper range. Temperature sensor has very large market and wide fields. So, it is important to be produced in low cost. Then, temperature sensor must be integrated on a single chip with other electronic devices. ‘Smart’ sensor can communicate with other device digitally and then difficulty will be reduced in the system.

For low cost, smart temperature sensors are produced in CMOS technology. However, because of its inaccuracy, CMOS temperature sensor’s spec is worse than other kind of temperature sensors. So through this research, I’d like to improve the accuracy of the CMOS temperature sensor.

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1.2 Basic principles

As we know, many kind of electronic integrated device have temperature dependent characteristics, so its characteristic is utilized to sense temperature. Resistors, MOSFETs, time-delay, diodes, BJT are utilized as temperature sensor. Its temperature dependent output signal is analog. It is expressed as various type. Voltage, current, time, period, frequency can be given examples. To compare this temperature dependent value, we must compare it with time-independent value.

For temperature measurement, we need two voltages that gives information in BJT. The thermal voltage (Known as $\frac{kT}{q}$ where k is Boltzmann's constant, T is the absolute temperature, and q is the charge of an electron) is used to generate PTAT (Proportional to absolute temperature) voltage, if we bias two BJTs with different current ratio. Bandgap voltage is for generating temperature independent reference. Their ratios will be determined at the back stages.

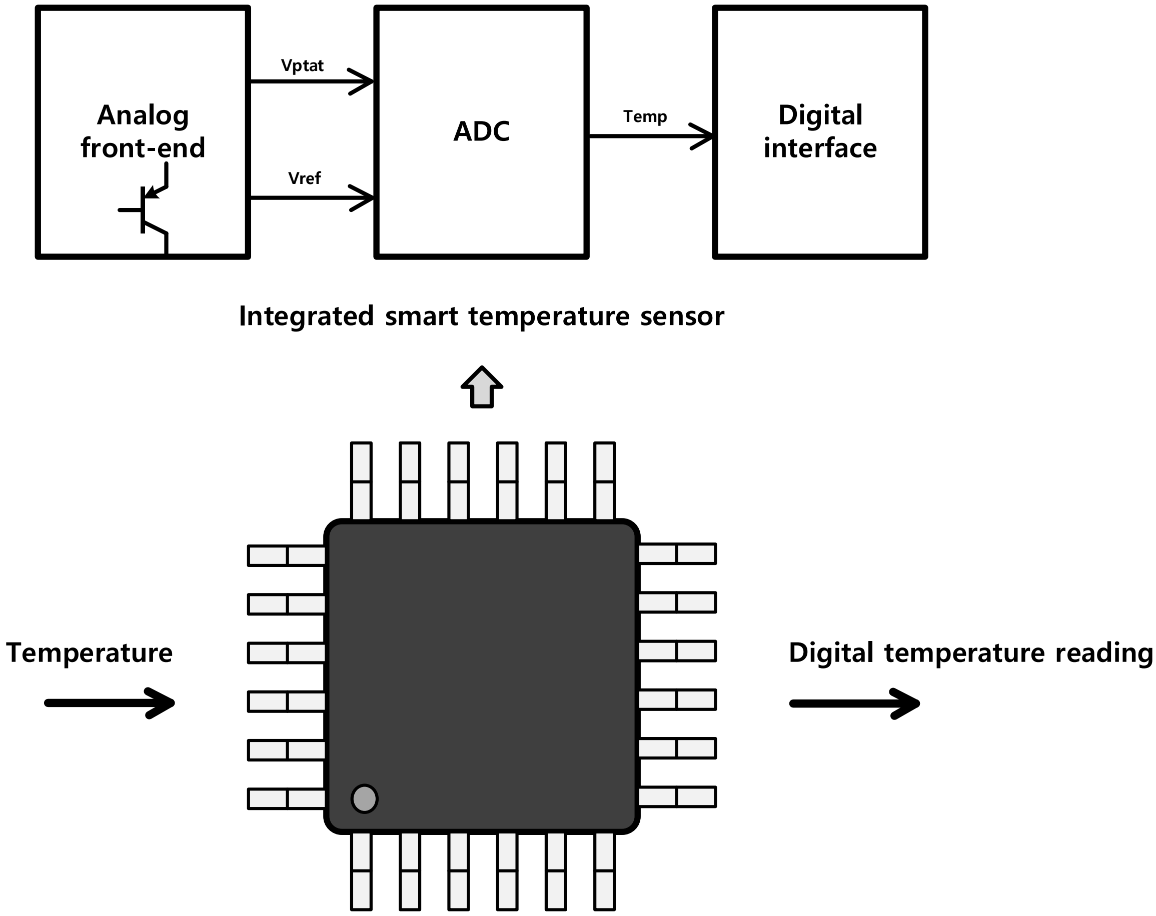

Figure 3.1 Block diagram of smart temperature sensor.

Figure describes the operating principle of the bias stage. The PTAT voltage is generated from the difference in base-emitter voltage between two BJTs biased with different current ratios. If we have accurate and linear ratio p, we can sense the temperature more accurately. However, its sensitivity is small (0.1~0.25mV/K) so we must utilized signal with amplification.

The reference voltage which is temperature independent, is called as 'bandgap reference' because

Vref is equal to the silicon bandgap voltage. The base-emitter voltage is equal to 1.2V if it is extrapolated to 0K, and voltage decreases by about 2mV/K. For the temperature independent voltage, we must add $\alpha \times \Delta Vbe$ voltage so Vref voltage is generated.

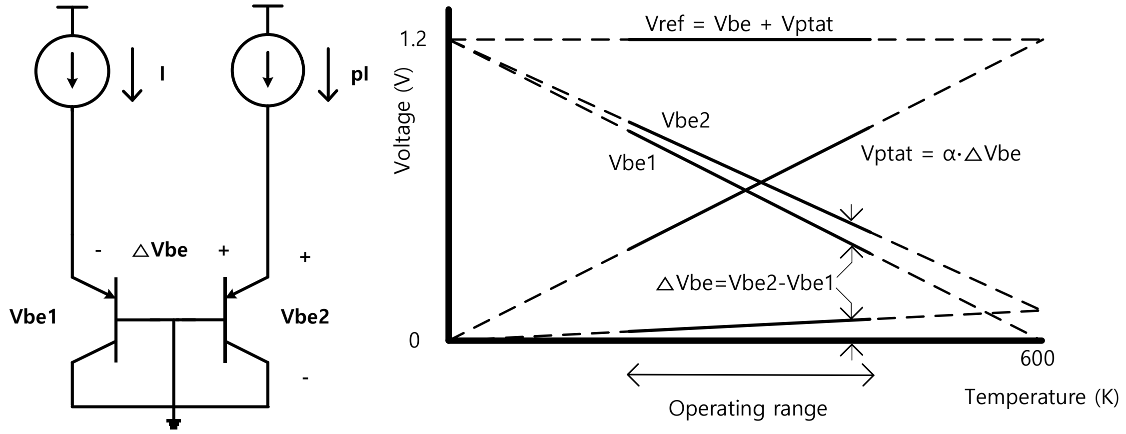

Figure 1.2 Measurement principle of temperature

1.3 Context of the research

Temperature sensors are composed of bias core, readout circuit, and the digital backend. Each stage has further works to do. First, at the bias circuit, sensing core must be chosen with the purpose of the temperature sensor. The BJT type is utilized broadly, but there are many efforts to modify the sensing core like resistor, MOSFET, delay of the inverters. With these cores, techniques which can reduce errors are included.

Second, the readout circuit can be divided into 3 types. ADC, TDC, FDC. In ADC, delta-sigma ADC is broadly utilized because of its high resolution and accuracy. Temperature doesn't need to be measured quickly so speed is not issue. Its problem comes from the power and complexity. For delta-sigma ADC, many amplifiers and the decimation filter are needed so it can be a burden. For the simplicity, TDC and FDC are utilized. It senses the time or frequency. Its information will be converted to temperature.

1.4 Organizations

Researching conventional CMOS smart temperature sensor is necessary to improve the circuit design. At first, we have to know how we can measure temperature from the electric information. There are various ways (current, voltage, delay, period, frequency etc.), so explanation about conventional measurement method and proposed method will be discussed.

Chapter 4 describes the proposed circuit design deeply. In order to reduce the complexity of readout, temperature is measured by the frequency. Conventional CMOS smart temperature sensor's readout is composed of Sigma-delta ADC. Its resolution and accuracy performance is good but its complexity can be burden. Frequency is generated by relaxation oscillator based readout circuit. Flipping capacitor technique is added to cancel the error by offset. The error sources which are discussed in chapter 3 should be compensated to reduce temperature error. Techniques for compensating error are also discussed.

In chapter 5, measurement results are described. At first, simulation results and the expected error will be shown. Then, the measurement results and the temperature error will be figured. For proving the effect of capacitor flipping technique, comparison chip will result will be compared with the measurement result. After that, α adjustment effect will be shown.

Finally, chapter 6 makes conclusion and discuss about the further works of smart temperature sensor. It will review the technique and the results briefly and review the works.

Chapter 2. Temperature measurement principle

CMOS smart temperature sensor's output value will be digital number. To acquire digital temperature, ratio-metric measurement must be utilized. Comparing reference voltage (Temperature independent) with PTAT voltage (Temperature dependent) can get the information of their ratio. With the ratio value, digital representation of temperature is read.

2.1 Conventional temperature measurement method

In chapter 1, principle of temperature measurement is discussed briefly. There are two ways to generate PTAT voltage which is proportional to temperature. First, if different bias current is applied with two BJTs (Successive current bias with different ratio with one BJT is also possible), the voltage difference is utilized as temperature measurement. Second, by adjusting emitter ratio can generate PTAT voltage with identical bias current. With r : 1 emitter area ratio and 1 : p bias current ratio can generate linear ratio 1 : pr. Equation of the base-emitter voltage difference is proportional to temperature :

$$\Delta \mathrm{Vbe} = \frac{kT}{q}\ln\left(\frac{pI1}{Is}\right) - \frac{kT}{q}\ln\left(\frac{I1}{rIs}\right) = \frac{kT}{q}\ln(pr)$$

Is is the saturation current of BJT and I1 is the unit bias current. PTAT voltage's term is defined with constant k and q, and the ratio p and r. They are temperature independent. As a result, T is temperature, so PTAT voltage has very accurate temperature dependency ideally.

The sensitivity of $\Delta \mathrm{Vbe}$ is about 0.1 ~ 0.25 mV/K (3<pr<16). We can change this sensitivity with changing bias current ratio or emitter area ratio. There can be trade-off with this sensitivity. Increasing sensitivity can reduce the burden of the readout stage (ADC, TDC, FDC). However, increasing sensitivity is done by increasing current ratio or increasing emitter area. Then, the complexity increases with error reduction technique. (Dynamic Element Matching). Proper sensitivity should be considered for circuit design.

With PTAT voltage, CTAT voltage is needed to make bandgap reference. At 0K, extrapolated value is 1.2V and it decreases almost linearly.(About -1.8~2mV/K).

$$V_{be} = \frac{kT}{q}\ln\left(\frac{I1}{Is}\right)$$

Is is the saturation current and I1 is the bias current. However, CTAT voltage shows worse performance than PTAT voltage. If we observe CTAT term, non-ideal parameter is observed. Is and I1. Because of processing spread, variation of I1 and Is will be error source. Compensating this non-linearity technique will be discussed later. Trimming, calibration is well-known method. The non-linearity error shown in CTAT voltage is called 'curvature error'. Curvature correction will be stated at later chapter. After some compensation techniques, Vbe voltage is considered as ideal linear voltage with temperature. Bandgap reference is generated by adding Vbe voltage(CTAT) and the amplified $\Delta \mathrm{Vbe}$ voltage(PTAT).

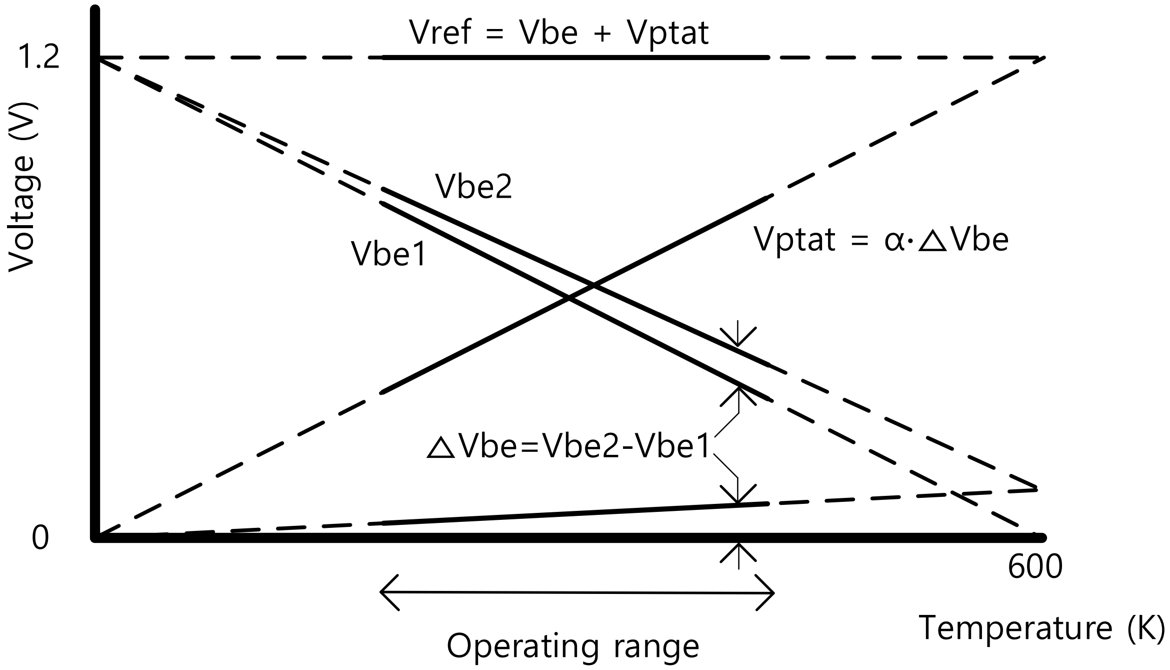

Figure 4.1 Overall temperature measurement graph

$$\mathrm{Vref} = V_{be} + \alpha\Delta\mathrm{Vbe}$$

The ratio α makes the temperature coefficient of bandgap reference 'zero'. It makes PTAT voltage and CTAT voltage opposite slope.

$$\alpha = -\frac{\partial Vbe}{\partial T} \times \frac{q}{kln(pr)}$$

If the emitter area ratio 'r' and bias current ratio 'p' are selected, the ratio α is calculated. If 'pr' ratio is about 3~16, the ratio α will be between 8 and 20.

With reference voltage(Vref) and the amplified PTAT voltage(αΔVbe), the digital temperature number will be represented from ADC. Many types of ADC can be utilized. Sigma-delta is the most frequently used ADC in CMOS smart temperature sensor. ADC output from Vref and Vptat is represented as μ.

$$\mu = \frac{Vptat}{Vref} = \frac{\alpha\Delta\mathrm{Vbe}}{V_{be} + \alpha\Delta\mathrm{Vbe}}$$

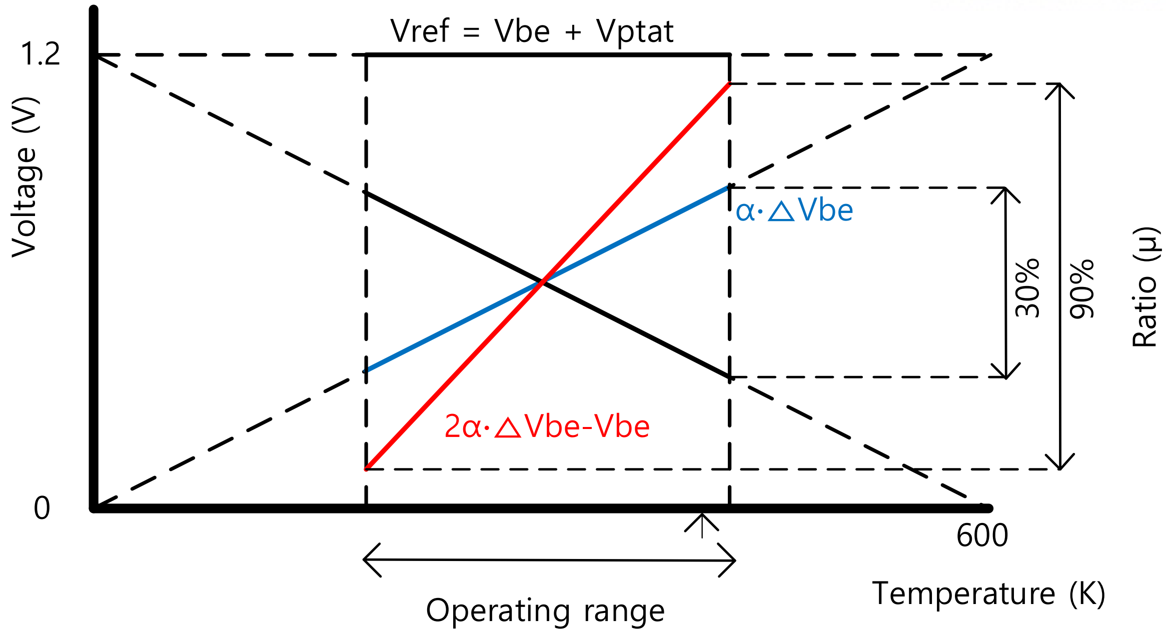

Figure 2.2 Temperature measurement with different slope

The ratio μ increases if temperature increases because Vref is temperature independent and Vptat has positive temperature tendency. μ will have positive temperature coefficient. With two constants A, B temperature information can be measured. A is about 600K(μ increases from 0 to 1), and B is about -273K.

$$\mathrm{Dout} = \mathrm{A} \times \mu + \mathrm{B}$$

Conventional measurement method contains 30% of total range. Because of that, ADC resolution burden will increase. If we change the 'μ′ equation differently, we can widen the operating range. If we modify the equation into

$$\mu = \frac{2\alpha\Delta\mathrm{Vbe} - \mathrm{Vbe}}{V_{be} + \alpha\Delta\mathrm{Vbe}}$$

Range will be widen from 30% to 90%, so we can reduce the burden of ADC resolution. However, this equation can be error source which comes from Vbe. The reason why we use amplified PTAT voltage is that PTAT voltage has better performance than CTAT voltage in linearity. However, the modified equation contains Vbe term. So non-linearity can be included in the slope.

2.2 Temperature measurement without bandgap

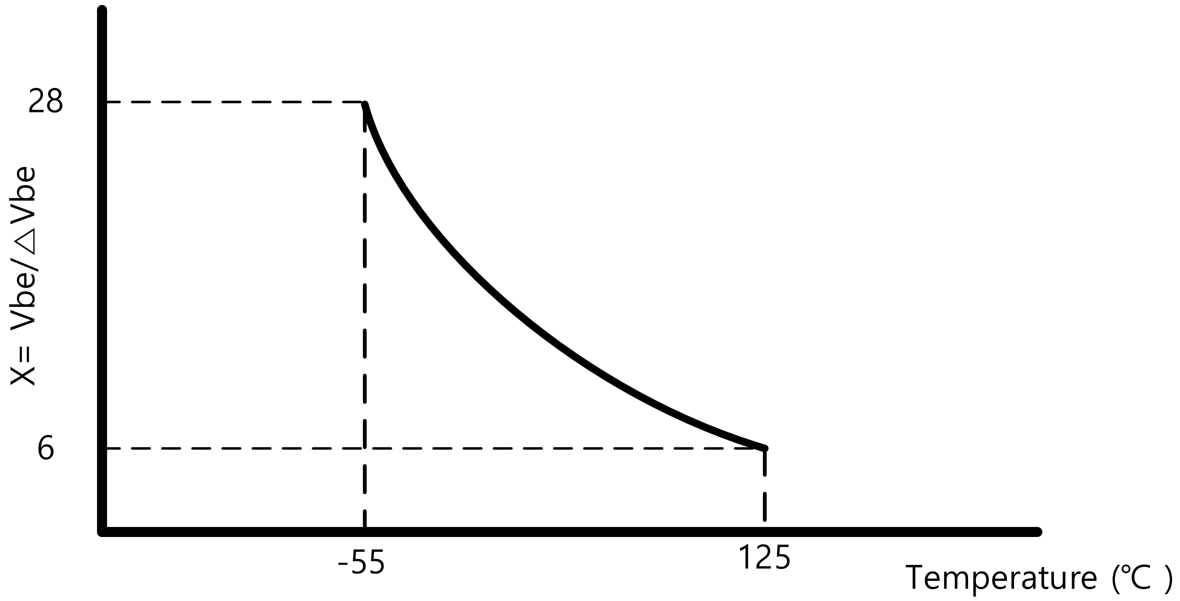

Figure 2.3 X graph with temperature change

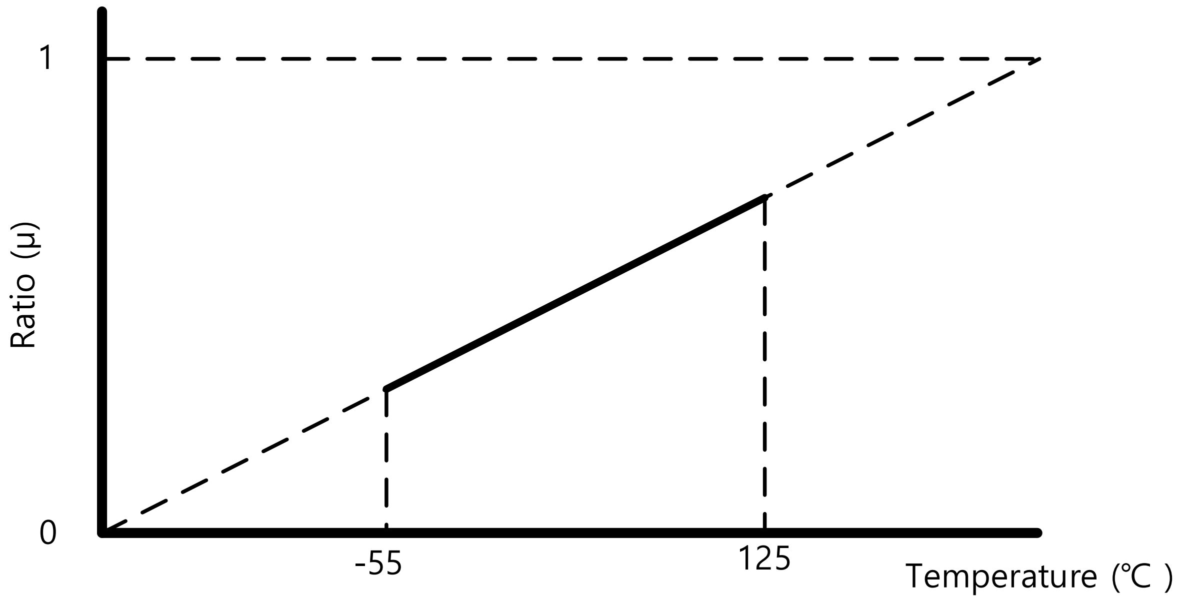

Figure 2.4 Mhu graph with temperature change

Conventional method is the fundamental measurement method. The composed circuit needs a circuit that generate bandgap reference, and amplifying circuit for PTAT voltage. It can be a burden in analog stage. There are efforts to reduce the burden at the analog stage. Adjusting α digitally can be a alternative method. Error caused by incorrect α can be calibrated easily at the back stage. New parameter X is measured.

$$X = \frac{Vbe}{\Delta Vbe}$$

This function is non-linear function of temperature, which varies from 7 to 24 (-40℃~125℃) if the current bias ratio is 5. It is non-linear function so this parameter cannot be converted into temperature rightly. However, μ value can be derived from X.

$$\mu = \frac{\alpha \Delta Vbe}{V_{be} + \alpha \Delta Vbe} = \frac{\alpha}{\alpha + X}$$

Because of this method, amplified PTAT voltage and CTAT voltage don't need to be added in the circuit. Its procedure is shifted from analog to digital. It reduces power consumption, circuit complexity, and total area.

Constant α is immune to process spread because α is implemented at the back stage. We can correct the error by adjusting α at the digital domain. This idea simplifies the circuit burden. Discussion about digitally α correction will be discussed more at the later chapters.

Chapter 3. Proposed circuit design

Before explaining about the proposed circuit design, 3 previous works will be discussed. These papers gave the idea. Temperature does not have to be very accurate. In the state of art, inaccuracy of ± 0.1℃ temperature sensor is shown. Trade-off happens. With that accuracy, we have to give up power and simplicity. For that issue, I tried to make temperature sensor with low power, small area, and moderate accuracy.

At the next section, bias circuit will be discussed. In this section, various error sources will be discussed and the compensation technique will also be explained. After that, the readout circuit will be explained.

3.1 Previous works

3.1.1 CMOS temperature sensor with delta-sigma ADC

Paper's title is 'A CMOS Smart Temperature Sensor With a 3σ Inaccuracy of ± 0.1℃ From -55 ℃ to 125℃'. This paper is published at JSSC 2005. Its bias block is ordinary. However, 2nd order delta-sigma ADC is utilized as readout circuit. Because of that, 2 amplifiers will be added so power and the complexity will increase.

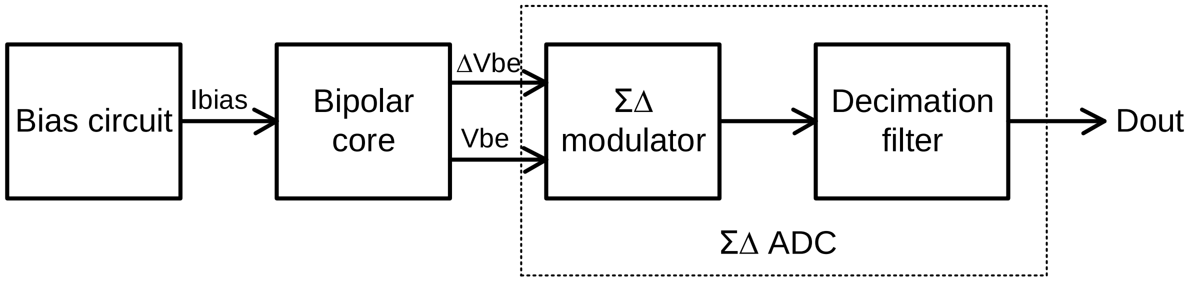

Figure 3.1 Block diagram of temperature sensor

Figure 3.1 represents the block diagram. From bipolar core, PTAT and CTAT voltage is read with delta-sigma ADC. Chip's total area is $4.5mm^2$, and the readout circuit is bigger than bias circuit. This temperature sensor's pros is that it has very high accuracy. However, power consumption and area increases and the complexity of readout stage increases.

3.1.2 CMOS temperature sensor with duty cycle modulated output

Second paper's title is 'A BJT-Based CMOS Temperature Sensor with a $3.6pJ \cdot K^2$-Resolution FOM'. It is published at ISSCC 2014. Its readout circuit is based on relaxation oscillator. Its principle is measuring duty cycle of output pulse. At the integration capacitor, PTAT current is charging and the CTAT current is discharging. Adjusting the amount of current ratio, the duty cycle information will give temperature.

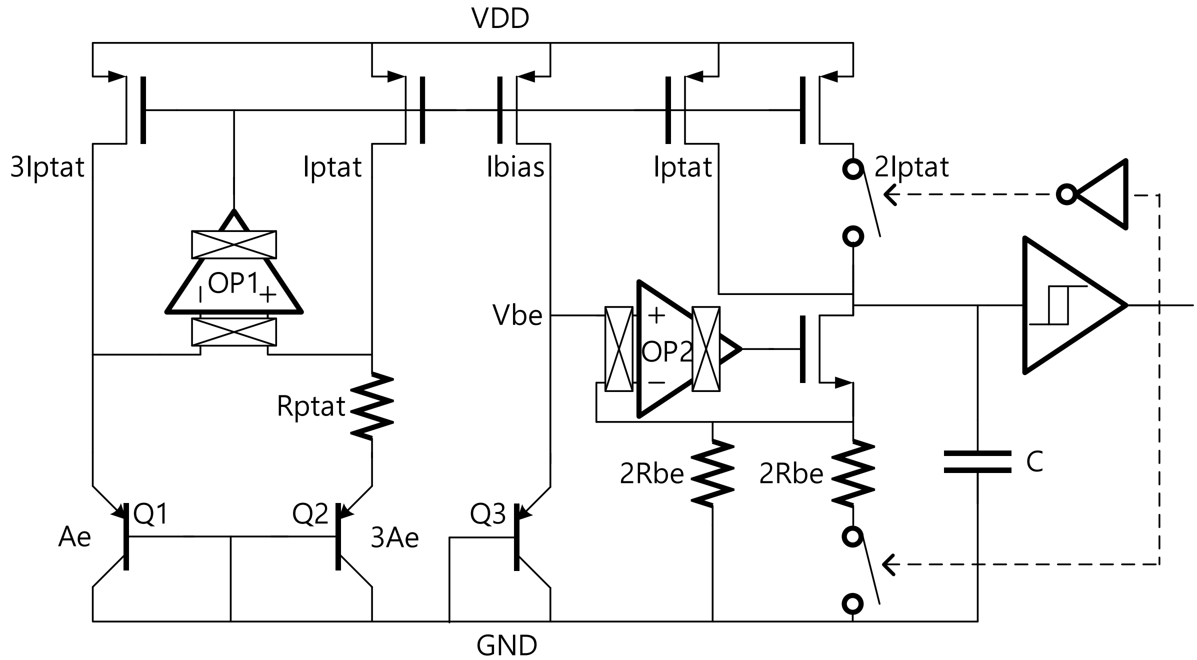

Figure 3.2 Overall schematic of temperature sensor

Figure 3.2 represents the overall schematic of temperature sensor based on relaxation oscillator. As you can see, OP1 is used for biasing PTAT current and OP2 is used for biasing CTAT current. Chopping is utilized to compensate the offset. By using Schmitt trigger for the comparator, the duty will be measured.

This paper's pros is that readout is simpler than previous paper. Output pulse is used as inner clock signal for chopping and Dynamic Element Matching. However, it has cons. Integration voltage is discharged with CTAT current so CTAT current generation circuit is needed. The comparator offset is not cancelled.

3.1.3 RC oscillator with comparator offset cancellation

The last paper's title is 'An RC oscillator with comparator offset cancellation'. It is published at JSSC 2016. It is not temperature sensor paper but relaxation oscillator paper. Its structure is simple. Two capacitor integrates voltage sequentially comparing with resistor reference voltage. During the operation, the first phase adds the offset and the second phase subtracts offset.

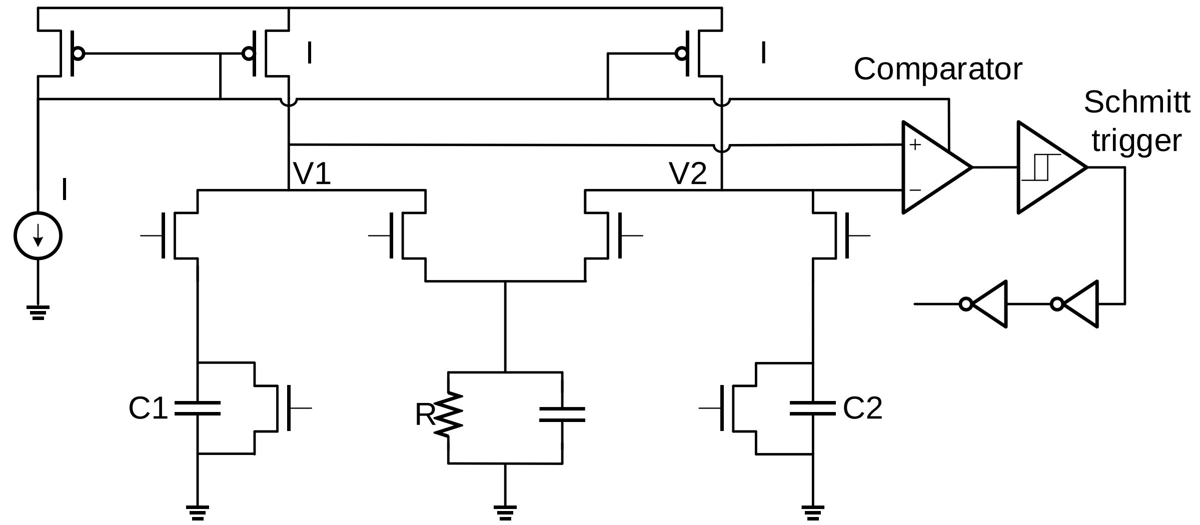

Figure 3.3 Circuit schematic of relaxation oscillator with offset cancellation

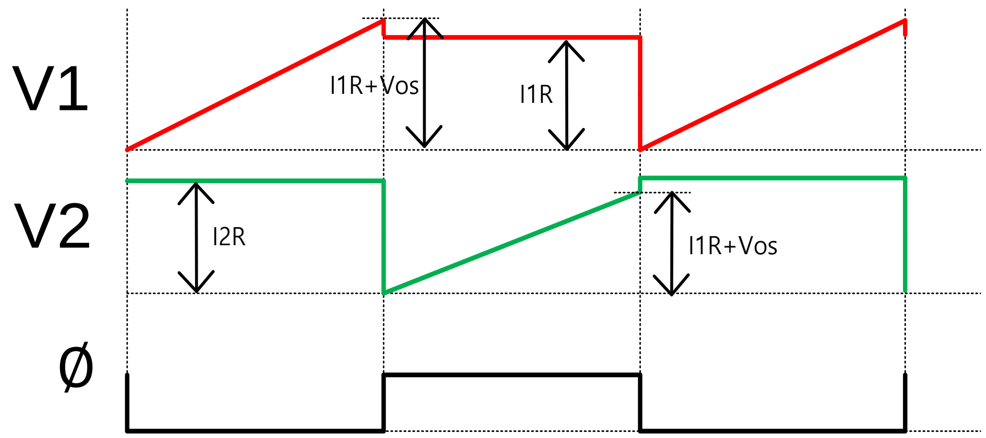

Figure 3.4 Oscillator operation

Figure 3.3 is about circuit schematic and figure 3.4 is about the operation. Output pulse signal is utilized as switch controller. This circuit can cancel offset and the reset time is not needed. Conventional oscillator has only one capacitor so reset time delay can be error source. However, 2 capacitors are integrated so the area will be doubled. Switch can also be error source.

3.2 Biasing circuit

3.2.1 Temperature sensor core type

	Thermistor	MOSFET	BJT
Power	☺	☺	☹
Linearity	☹	☹	☺
Accuracy	☹	☹	☺
Range	☹	☹	☺
Area	☹	☺	☺

Figure 3.5 Temperature sensor core type table

For sensing temperature, electrical information must have temperature dependence. Using this temperature dependence, temperature can be measured. Passive devices like thermistor, MOSFET, BJT contain temperature dependence, so it can be utilized as temperature sensor core.

Figure 3.5 represents the well-known temperature sensor core and its characteristic. Thermistor has good performance in power, but linearity, accuracy, range, and area performance is bad. Resistor area occupation is large and needs many calibration points. It is not proper with accurate temperature sensor.

MOSFET core type temperature sensor is used for low power. Its subthreshold region is operated to measure temperature, so power will be low. However, its accuracy, linearity and range are poor. For accuracy, BJT core type is mostly utilized. Its power performance is not good, but other performances are better than MOSFET and thermistor. For less calibration and accurate sensing, BJT is utilized as temperature sensor core.

3.2.2 How to generate PTAT current and CTAT voltage

To measure the temperature, this temperature sensor requires CTAT voltage and PTAT current. Their values are temperature dependent. CTAT voltage is utilized as reference voltage. Conventional temperature sensor compares bandgap reference with PTAT voltage. Bandgap reference is temperature independent and PTAT voltage is temperature dependent. However, this temperature sensor's reference voltage is changed with temperature change. It sounds strange, but temperature can be measured with this method. Measuring accurate temperature is accomplished with accurate circuit. In the bias circuit, there are many things that can generate errors. First, analyze how bias circuit is formed and see how errors can be made.

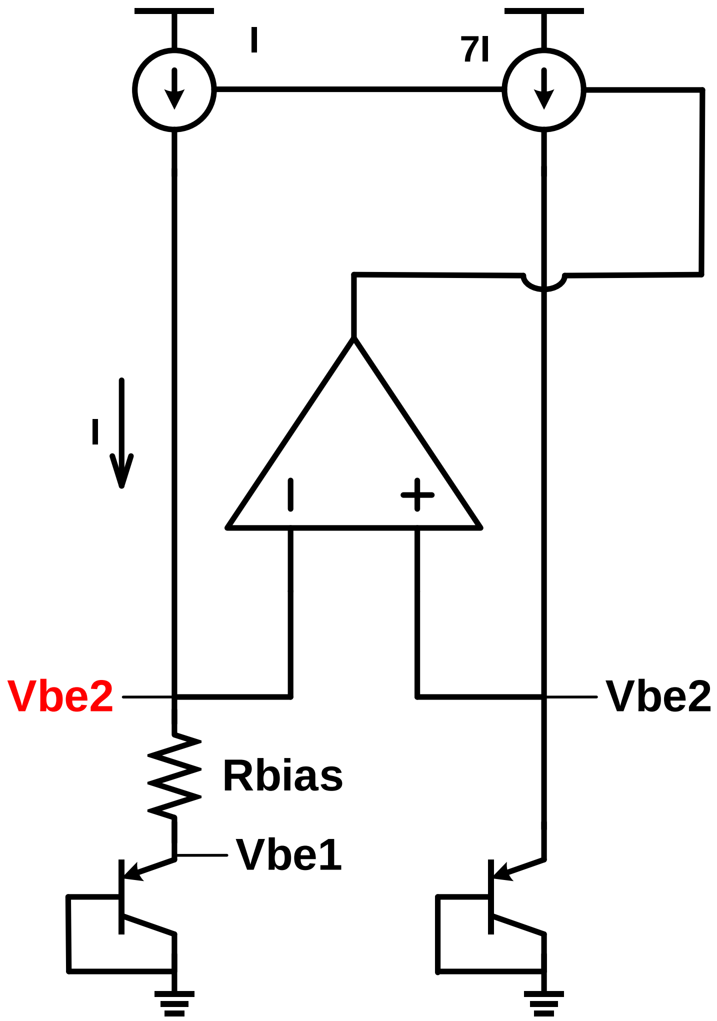

Figure 3.6 Conventional bias circuit of temperature sensor

Figure 3.6 represents the conventional bias circuit. It is composed of PNPs, resistor, amplifier, and current sources. If we bias two pnps with different current ratios, Vbe voltage will be generated. The difference will be utilized as PTAT voltage. There are two ways to generate PTAT voltage. By adjusting two different current ratio or emitter areas of two pnps, ΔVbe slope will be determined.

$$\mathrm{Vbe2} - \mathrm{Vbe1} = \frac{kT}{q}\ln(\mathrm{p})$$

K, q and p are temperature independent constants and T is temperature, so it is linearly temperature dependent. By negative feedback, the negative input of amplifier will be Vbe2. As a result, the voltage on the resistor is $\mathrm{Vbe2} - \mathrm{Vbe1}$. By ohm's law, the PTAT current will be generated.

$$I_{PTAT} = \frac{\mathrm{Vbe2} - \mathrm{Vbe1}}{Rbias}$$

This PTAT current will be used as integration current and CTAT biasing current. We also need one more PNP to generate reference CTAT voltage. CTAT voltage which is generated from PNP with PTAT current shows better performance in linearity. The bias current which has temperature dependence can reduce the curvature of CTAT voltage. As a result, PTAT current is used for integration current in relaxation oscillator and biasing CTAT voltage.

This bias circuit contains many error sources. First, current source error. Current sources can have mismatch, so the mismatch error will give the temperature error. Not only mismatch but also finite output impedance can limit the accuracy.

If we consider the resistor which is utilized for generating current, resistor also can be error source. Resistor has its own temperature coefficient, so current will be affected. Its effect must be compensated.

Amplifier offset can generate wrong PTAT current. Offset can be 1~10mV at the MOSFET. Offset can be added or subtracted so it can change the bias current, and it is temperature dependent, so it can give wrong information.

Finally, PNP's current gain β non-ideality can make error. Current gain is changed with the amount of bias current. We use different current ratios, so its difference makes different current gain.

There are many types of error from bias circuit, and next chapter will describe how these errors can be cancelled or compensated by various techniques.

3.2.3 Various error reduction techniques

	Error	Method
PTAT current	Current mismatch	Dynamic Element Matching
	Output resistance	Cascode current source
	Resistor TC	Zero TC composite resistor
	Offset voltage	Chopping
CTAT voltage	Current gain (pnp)	Rbias compensation (X)
		Current proper biasing (O)
	PTAT spread	α-correction at the back stage
	Non-linearity	PTAT current biasing

Figure 3.7 Various error sources and methods for the compensation

The above figure 3.7 makes up the components for the oscillation and its error source and the methods to compensate or cancel errors. For oscillation, PTAT current and CTAT voltage are required. Errors can be divided into two types. First, current mismatch, finite output impedance, resistor TC, and offset voltage can change the PTAT current. Second, current gain, PTAT spread, and non-ideality of PNP can change the CTAT current. Each solution is mentioned at the next column.

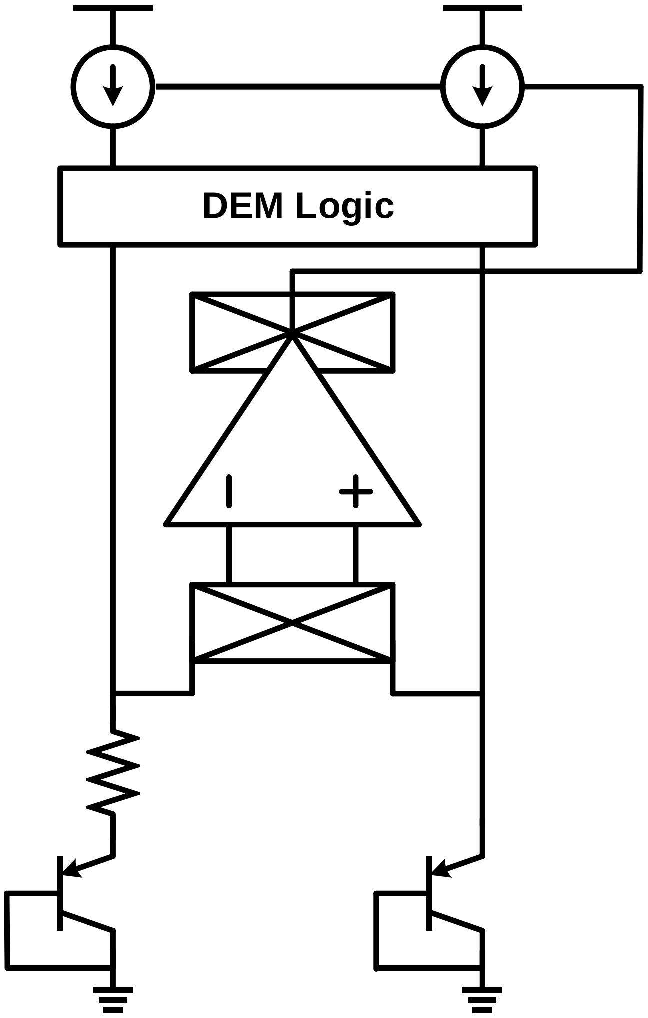

Figure 3.8 Modified bias circuit to reduce errors

Figure 3.8 is the modified bias circuit to reduce errors. Some techniques are not described at the figure. Current sources are cascoded so its impedanace increases. DEM(Dynamic Element Technique) is implemented to be more accurate.

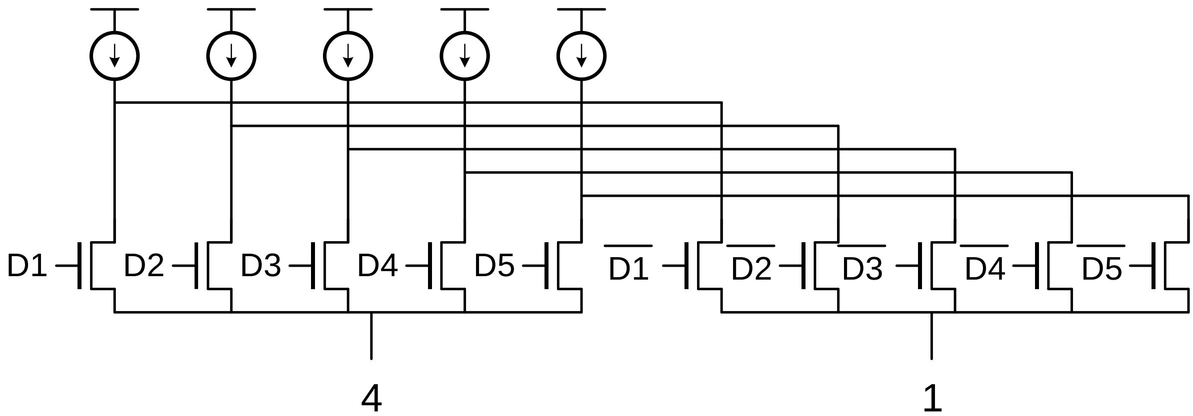

Figure 3.9 Dynamic Element Matching to bias 4:1 current ratio

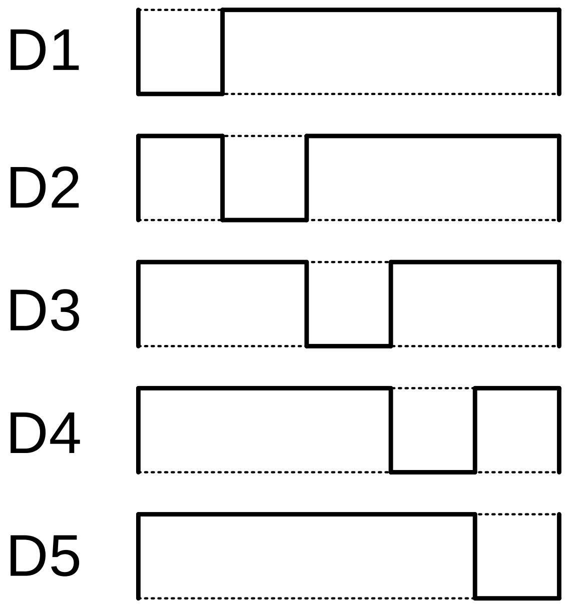

Figure 3.10 Timing diagram for DEM switches

Figure 3.8 is the modified bias circuit to reduce errors. Some techniques are not described at the figure. Current sources are cascoded so its impedanace increases. DEM(Dynamic Element Technique) is implemented to be more accurate. Figure 3.9 and 3.10 describes DEM. For simplicity, figure describes DEM for ratio 4:1. Each path will be changed with discrete output signal. The left path current will be 4I and the right path current will I. Mismatch errors will be compensated with multiple sampling. For 4:1 DEM, 5 timing will be minimum phases. It can be utilized in discrete system. Each current source has mismatch errors, but it will be averaged by 5 combinations. Readout circuit’s output is pulse wave, so DEM can be applied in this schematic.

Chopping is integrated in the bias circuit, so offset will be included and excluded with the phases. As a result, offset will be cancelled. More explanation about offset cancellation will be discussed at next section.

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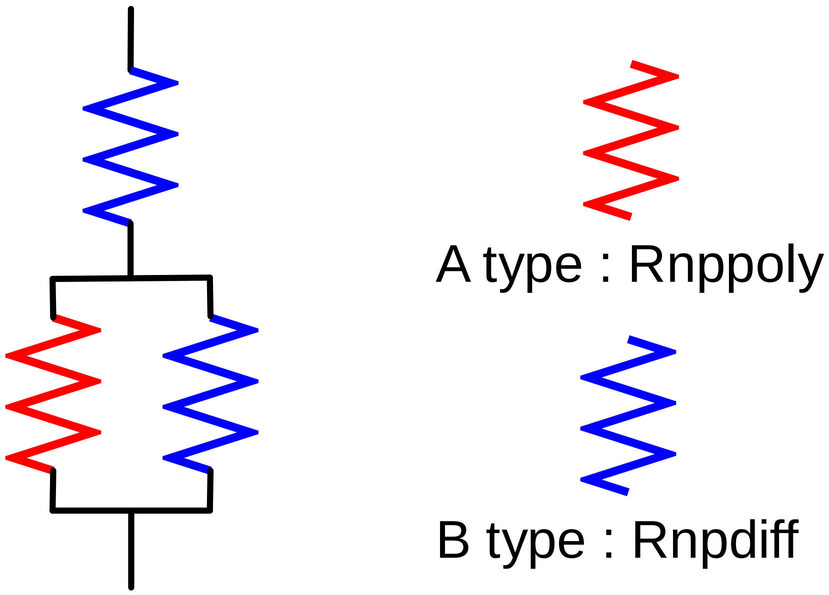

Figure 3.11 composite resistor used for zero TC

Resistor is also modified to composite resistor. Figure 3.10 describes the composite resistor. The series and parallel composite are both used. This connection will reduce the TC variation caused by sheet resistance variation. Two kinds of resistors are used. Rnppoly and Rnpdiff resistor. Current ratio is 7:1 and the resistor at room temperature is 120k at room temperature. As a result, unit bias current at room temperature is 420nA.

Various mentioned techniques are utilized to reduce bias circuit errors. These techniques are also included in the conventional temperature sensor core. By this techniques, more accurate PTAT current will be defined. CTAT voltage biasing with PTAT voltage will have less curvature, so this PTAT current is utilized for biasing CTAT voltage and for integration.

3.3 Readout circuit

3.3.1 Circuit operation

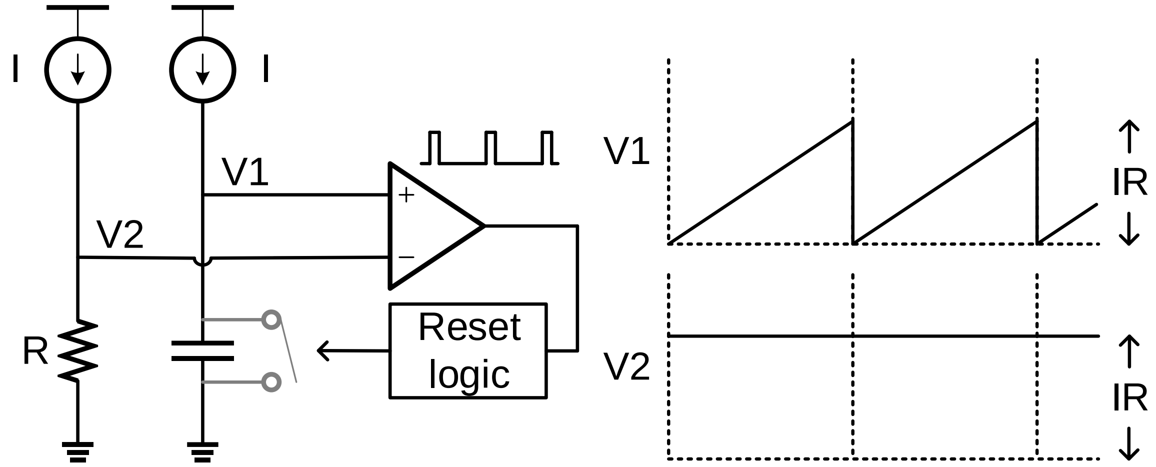

Figure 3.12 Conventional relaxation oscillator and its operation

Conventional temperature sensor's readout circuit is ADC. There are many types of ADC. However, delta-sigma ADC is mostly utilized in temperature sensor. Temperature measurement doesn't need high speed, and delta-sigma ADC's resolution is high. However, it integrates many amplifier so its power consumption will be high. Not only power but also area will increase. My target was to reduce the area and power of the readout circuit and measure the temperature simply. That's why proposed temperature sensor's readout circuit is composed of relaxation oscillator.

Before discussing about readout circuit, we need to know the error sources of the relaxation oscillator. Figure 3.11 illustrates about the conventional relaxation oscillator. One node is connected with the reference voltage and the other node is connected with the capacitor. Current flows through the capacitor so its voltage will increase. When comparator is toggled, the capacitor will be reset its voltage. It repeats this operation so oscillation is performed.

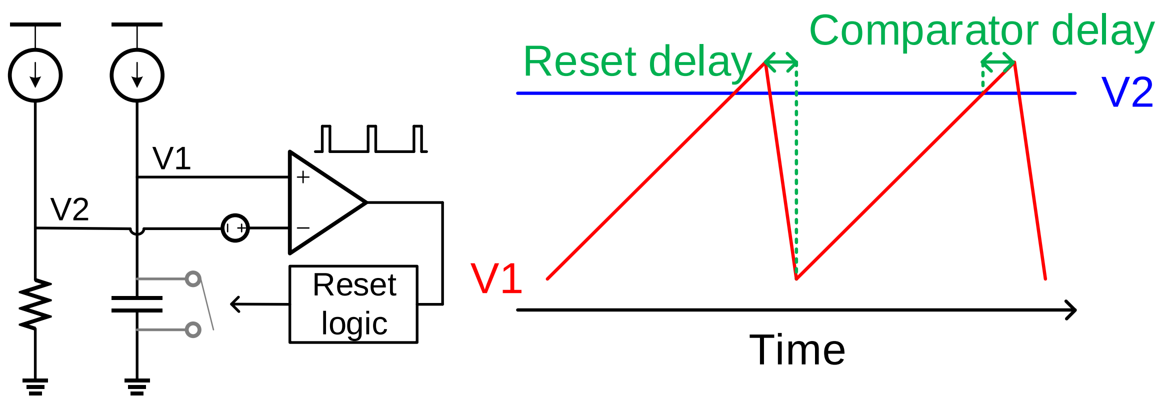

Figure 3.13 Oscillation error by delays

This operation can contain some error sources. Figure 3.12 describes the oscillation error by delays. First, comparator has its own delay, so the integration voltage will slightly higher than the reference voltage. Second, the capacitor reset time will be needed. Its time will be very short, but It can cause error.

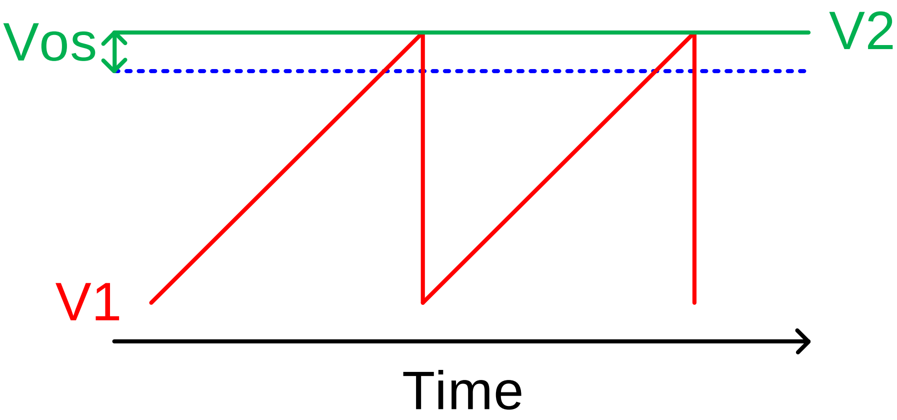

Figure 3.14 Oscillation error by offset

Figure 3.13 is about the offset error. Offset voltage of the comparator will change the reference voltage or integration voltage. The above figure includes the changed reference voltage so the oscillation period will include error. For measuring accurate temperature, mentioned errors must be compensated or cancelled, so readout operation contains some techniques to measure more accurate period.

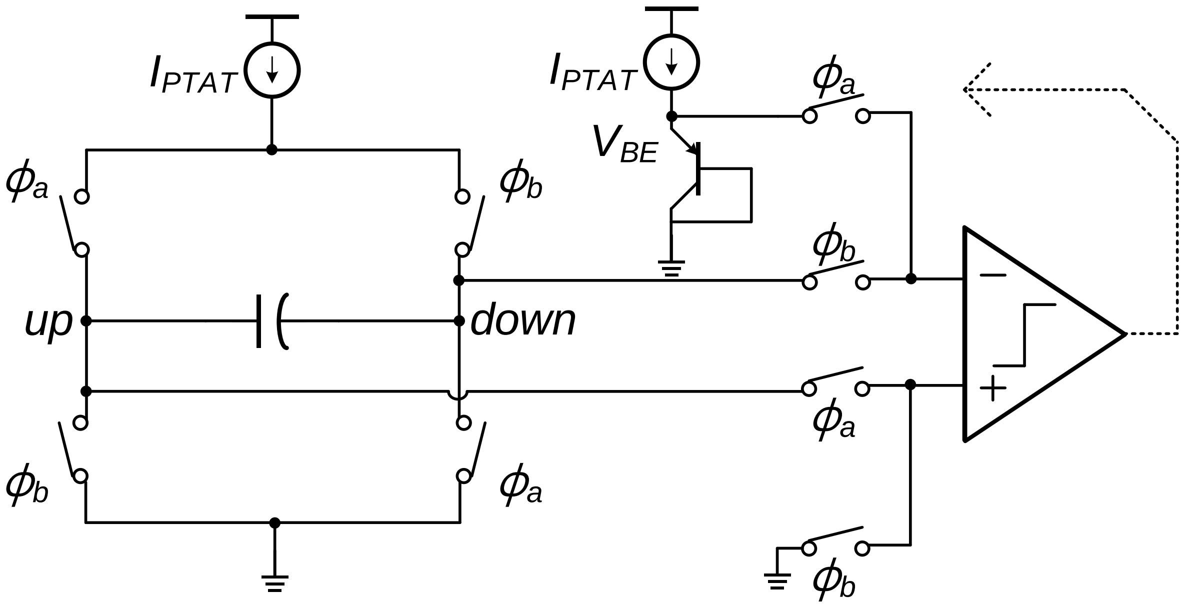

Figure 3.15 Overall readout circuit

Figure 3.14 illustrates the overall readout circuit. First, PTAT current made by bias circuit flows to BJT to generate Vbe voltage. Vbe voltage will be utilized as reference voltage. By switching operation, oscillation will be performed. It has ‘va’ and ‘vb’ signal. They are complementary signals and formed by output pulse of oscillation. When ‘va’ is on and ‘vb’ is off, the negative input of comparator is Vbe and positive input of comparator is ‘up’ node. When ‘va’ is off and ‘vb’ is on, negative input of comparator is ‘down’ node and the positive input of comparator is grounded.

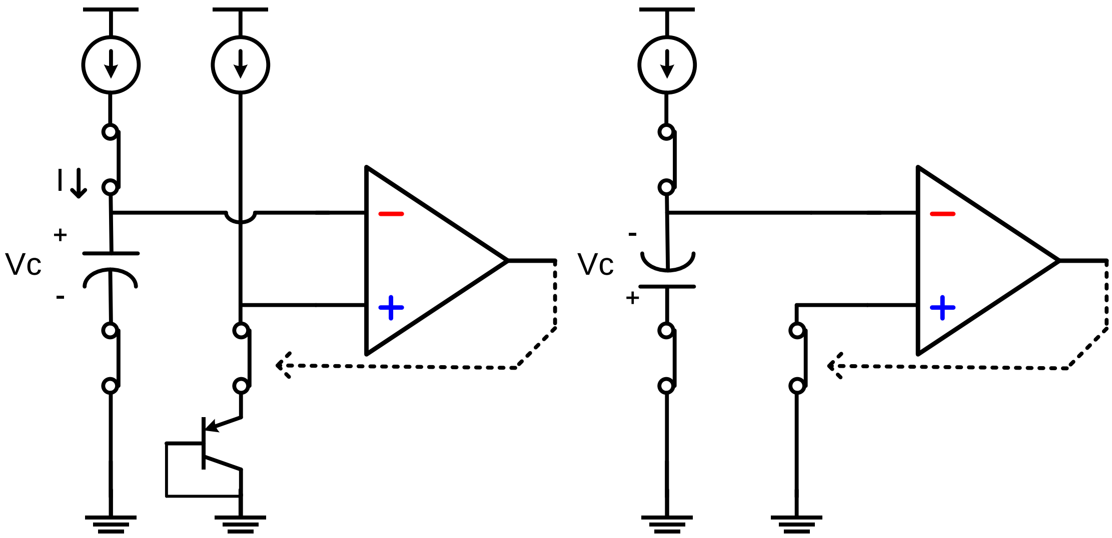

Figure 3.16 Readout operation

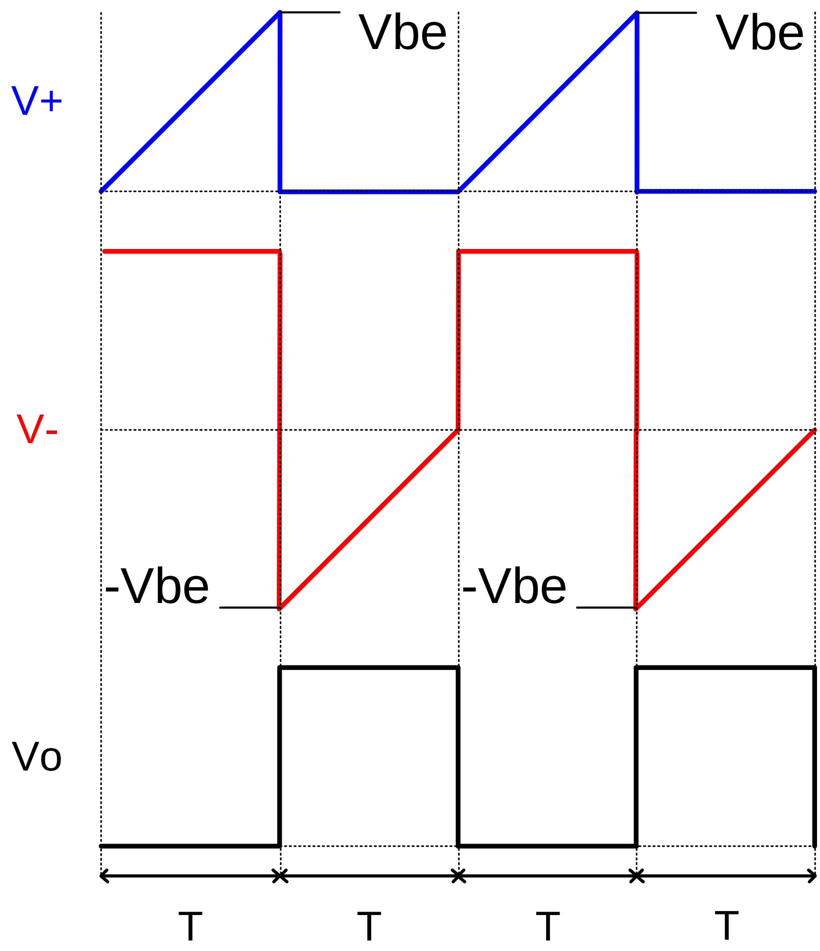

Figure 3.17 Waveform of the comparison nodes

Figure 3.15 is about the two phases of oscillation. At the first phase, 'va' is on and 'vb' is off. Reference voltage will be CTAT voltage and the capacitor is integrated from ground to CTAT voltage. When the comparator toggles, the second phase will be started.

At the second phase, 'va' is off and 'vb' is on. Capacitor flips so the initial voltage will be –Vbe. It will be integrated from –Vbe to ground. As a result, each phase's integration time will be same theoretically. Figure 3.16 describes the waveform of the nodes deeply.

3.3.2 Conversion from period to temperature

At the previous section, the readout circuit operation is explained. The first phase of the integration is from ground to Vbe and the second phase of the integration is from –Vbe to ground. Ideally, it has same time and there is no reason to flip the capacitor. At the next section will explain why capacitor flips and now, the conversion method will be explained.

$$Q = C \times V = I \times t$$

$$V_{+} = \frac{I \times t}{C} \quad \text{(t is proportional to V)}$$

$$V_{-} = V_{BE}$$

Above equations describe the first phase of figure 3.15. Its capacitor is integrated from ground to Vbe. The integration time is proportional to the capacitor voltage if the capacitor size and the amount of current does not change. Negative input of comparator is Vbe and the positive input of comparator is integration node, so the time will be represented as $\frac{I \times t}{C}$.

$$Q = C \times V = I \times t \rightarrow$$

$$V_{-} = -V_{BE} + \frac{I \times t}{C} \quad \text{(t is proportional to V)}$$

$$V_{+} = GND$$

Similarly, the second phase of the operation will follow the above equations. Its integration starts from –Vbe and end at the ground. At chapter 2, temperature measurement without bandgap reference is discussed. With the PTAT voltage and the CTAT voltage ratio, temperature can be measured. In this readout circuit, the integration time includes this term.

$$Q = C \times V = I \times t \rightarrow C \times V_{BE} = \frac{\Delta V_{BE}}{R} \times t$$

$$t = \frac{C \times V_{BE} \times R}{\Delta V_{BE}} \rightarrow \frac{\alpha \Delta V_{BE}}{V_{BE} + \alpha \Delta V_{BE}} = \mu$$

$$\frac{V_{BE}}{\Delta V_{BE}} = X \rightarrow \frac{\alpha}{X + \alpha} = \mu$$

$$\frac{t}{C \times R} = X \rightarrow \frac{\alpha}{\frac{t}{C \times R} + \alpha} = \frac{\boldsymbol{C \times R \times \alpha}}{\boldsymbol{t + C \times R \times \alpha}}$$

If we follow the above equations, temperature is defined as $\frac{C \times V_{BE} \times R}{\Delta V_{BE}}$. Capacitor and resistor values are constant so it will be affected by PTAT and CTAT voltage. X is the parameter which is used for measuring temperature, and X can be represented as time, so the period contains the temperature information.

One more important thing is that we can correct the passive device error. Capacitor and resistor can be varied. If these values change, the measured time will be converted to X wrongly. However, 'Mhu' value is converted from X with α. That means, if we add α at the digital backend, errors can be corrected with optimized α. Implement α term at the digital backend can achieve simplicity of the circuit. Error corrections can be achieved as well as the simplicity.

3.3.3 Offset cancellation with capacitor flipping

Capacitor flipping is done to cancel the offset error. Offset voltage of comparator can give wrong period. If the offset voltage remains constant, we don't have to consider the offset voltage. However, it is changed with the temperature change, so it will be affected differently with temperature change. That's why offset cancellation is necessary for this system.

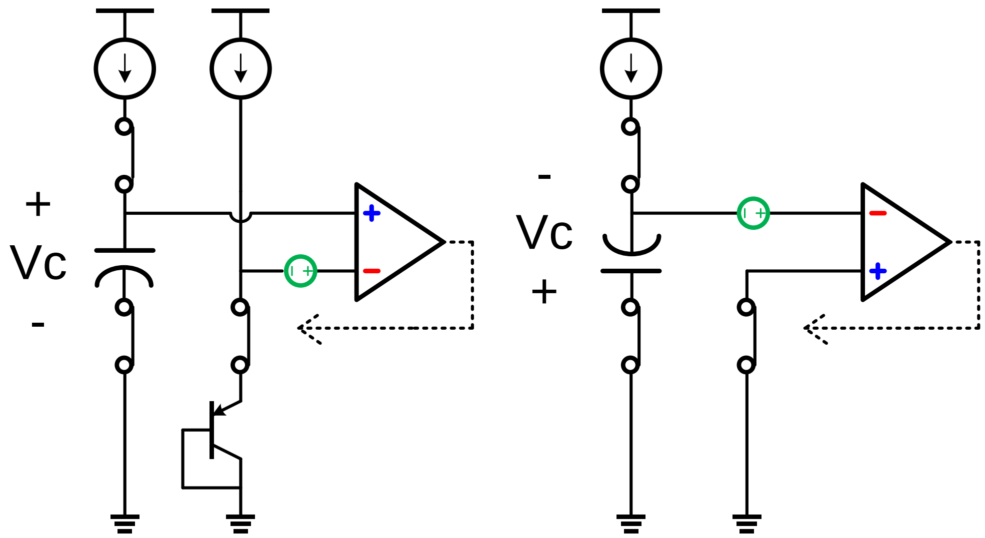

Figure 3.18 Oscillation operation with offset voltage modeling

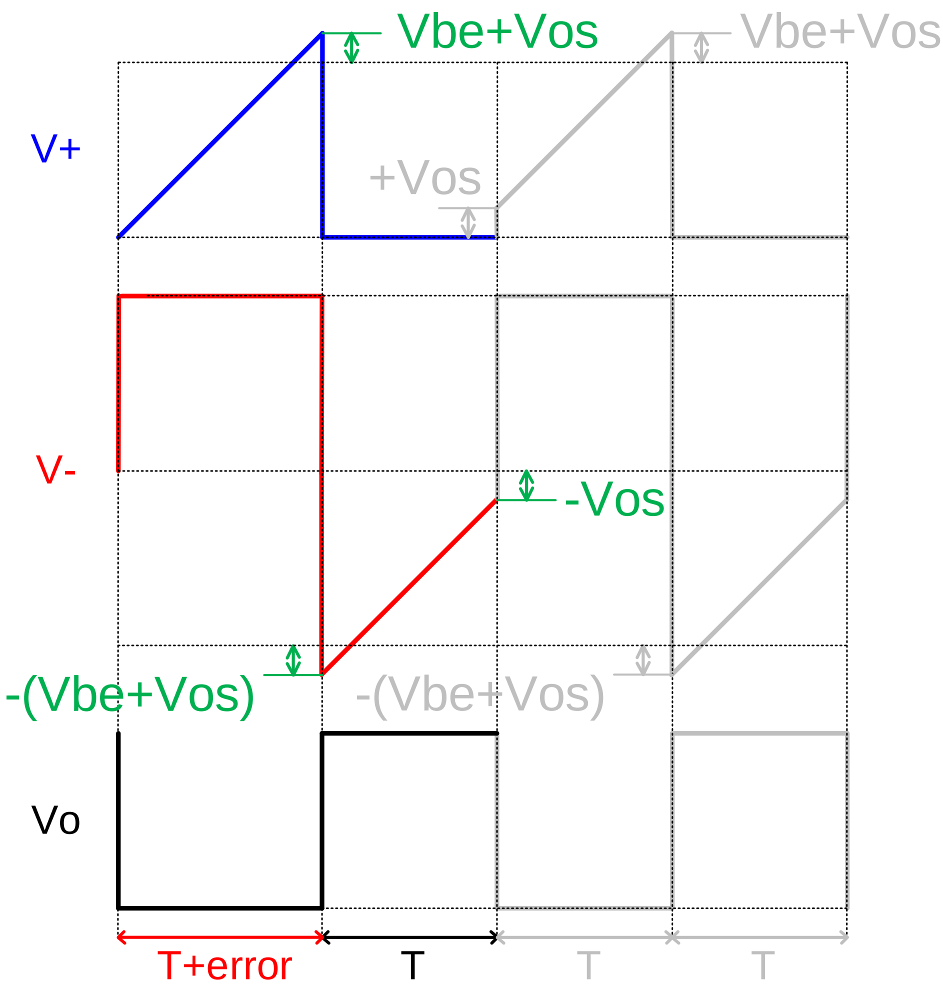

Figure 3.19 Waveform of the comparison nodes with offset voltage modeling

Offset voltage modeling is described at figure 3.17. At the negative input of the comparator, offset voltage is modeled. Figure 3.17 is the figure 3.16's waveform. At the first phase of the first oscillation, the voltage is integrated from ground to Vbe+Vos, so the period will increase. Then, capacitor flips so the integrated voltage is –(Vbe+Vos). From that voltage, it starts integration.

Now, the reference voltage is –Vbe. Then it will perform integration from –(Vbe+Vos) to –Vos. That means the real integration time will be same as the second phase. The remained voltage is –Vos after the second phase. Then, capacitor flips again and starts integration from +Vos to Vbe+Vos again. This operation's integration time is also same with the period of the first phase. As a result, the offset is cancelled with this capacitor flipping.

3.4 Other considerations

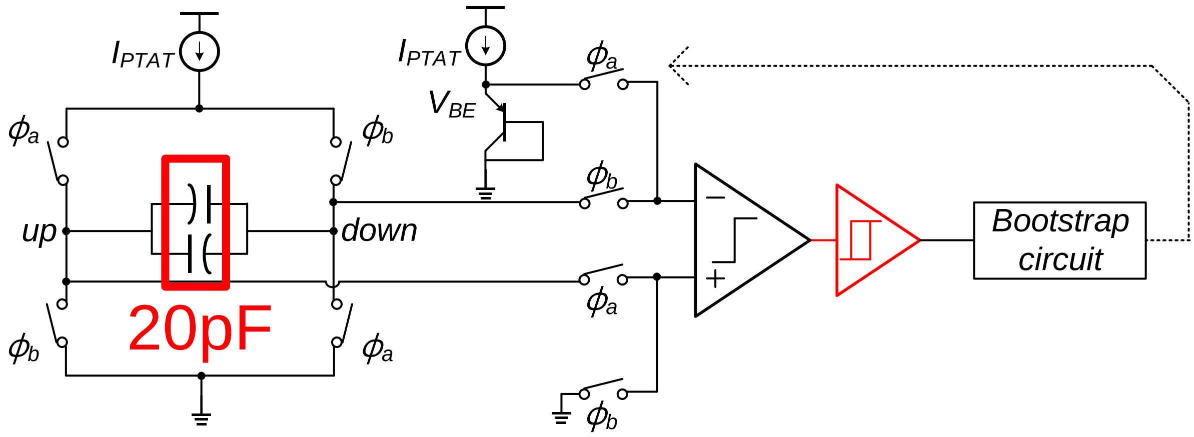

Figure 3.20 Overall readout circuit with some considerations

Previous sections of this chapter explains about the operation of the readout circuit and the conversion method from period of time and how offset cancellation is performed. From this section, the other minor considerations will be discussed.

First, integration capacitor's accuracy is important. It is directly connected with the comparator input, so the charge sharing will make the wrong integration voltage. We cannot fully eliminate the parasitic capacitance by the input MOSFET of the comparator, so we need to increase the size of the capacitor.

There is one more issue with integration capacitor. Capacitor flips with the phase change, so the current flow direction is reversed. Parasitic capacitance shown through top plate and bottom plate needs to be same so careful layout is needed. As figure 3.19, unit capacitor is composed of two capacitors. They are reversing each other so the mismatch of the parasitic capacitance between top plate and the bottom plate will be reduced.

Second, during the simulation the output pulse is destroyed with the glitch. When the temperature is high, delay will be changed. Because of the delay change, the complementary clocks will overlap each other so the problem will be happened. To overcome this issue, Schmitt trigger after comparator is connected. It is inverter based Schmitt trigger so it can catch the glitch.

Finally, the switch signal must be changed from ground to VDD. When the capacitor flips, the integration voltage is –Vbe. Then, the turn off switch will not fully turn off because the Vgs voltage is not zero when the gate voltage is ground. As a result, bootstrapping circuit is needed. It doubles the switching voltage from 'GND~VDD' to '-VDD~+VDD'. It blocks the switch from tuning on by the negative integration voltage.

These issues can give wrong period, so it looks like minor but it must be resolved carefully. Capacitor flipping cancels the offset voltage error and the reset delay. We don't have to reset the capacitor because the voltage is remained. The rest error of the relaxation oscillator is the comparator delay. Actually, proposed circuit does not contain comparator delay cancellation technique. However, we don't have to care about this error if the period is not short. The delay time unit is known as 'pico' seconds. If the oscillation period is 'micro' unit, delay change looks very tiny so we don't have to consider delay. Finally, we can achieve the accurate periods. With this period, accurate temperature can be measured.

Chapter 4. Measurement results

4.1 Design specification

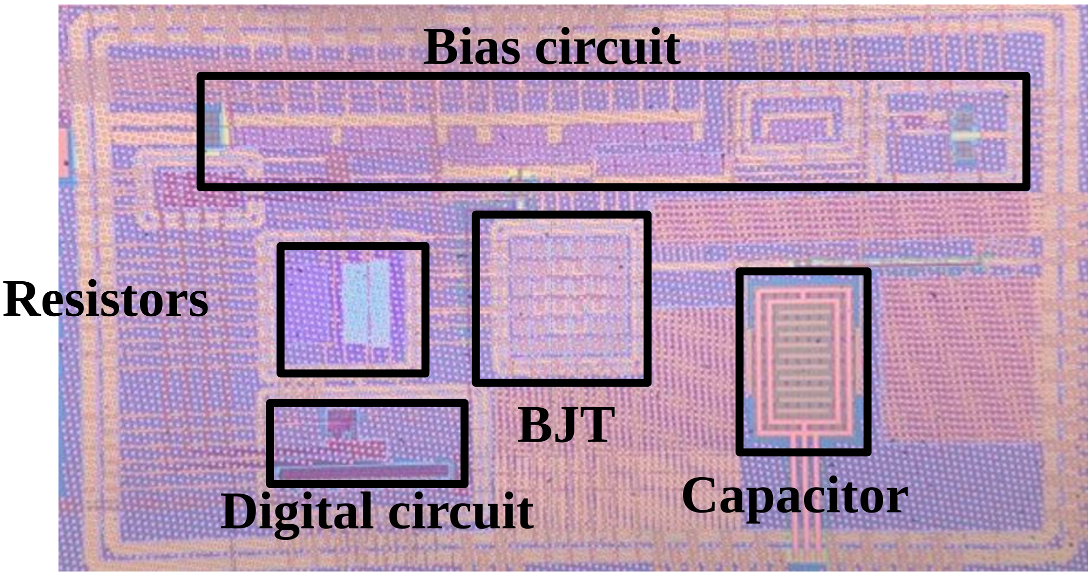

Figure 4.1 Chip micrograph

Proposed sensor specification	
Technology	0.11μm
Chip area	0.05mm^2
Supply voltage	1.6-2.1V
Supply current	18μA
Temperature range	-40~80°C
Inaccuracy	±0.6°C

Figure 4.2 Specification table

4.2 Simulation results

Using Cadence program, temperature sensor chip is completed. It is composed of 3 stages. Bias stage, readout stage, counter stage. Previous tape-out was done about 1 year ago. At that time, only bias stage was completed. At first, I'd like to connect my bias stage with SAR ADC made by our lab member. Its original purpose is for bio sensor. It does differential conversion, so it was hard to connect with bias circuit. It failed and I tried to build my own readout circuit and I did it.

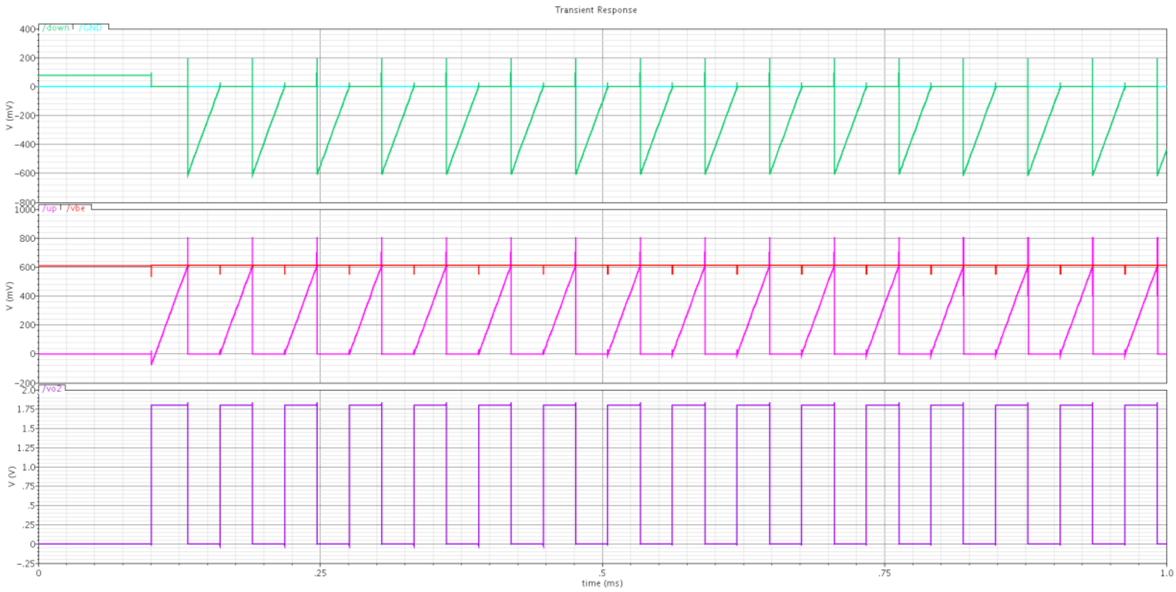

Figure 4.3 Output waveform of the readout operation

Figure 4.1 represents the operation of readout circuit. The top waveform represents negative input node of comparator, middle waveform represents positive input node of comparator, and bottom waveform represents the output pulse of comparator. As I expected, it operated correctly. At the first phase, Vbe voltage is compared with the integration node which increases from ground to Vbe. At the second phase, capacitor is flipping so the initial voltage is –Vbe. It starts integration from –Vbe to ground. With this flipping operation, offset is fully cancelled. Using the counter at the back stage, the pulse is counted during the chosen time. Then, temperature will be given with some mathematical conversions.

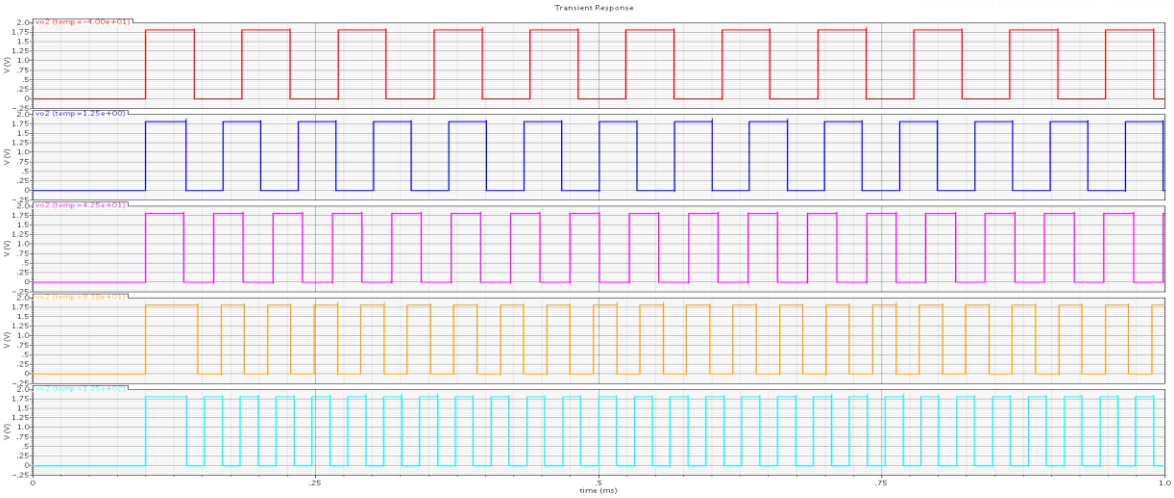

Figure 4.4 Output pulse with temperature change

Figure 5.2 represents the output pulse waveform with temperature change. First target range was $-40\sim125℃$. If the operation is considered, pulse will be shorter when temperature increases. Reference voltage is CTAT voltage and the integration current is PTAT current. As temperature goes up, current will increase and CTAT voltage will decrease. As a result, the output periods will decrease and give us the temperature information. Figure includes 5 waveform. Each temperature is $-40, 12.5, 42.5, 83.75, 125℃$. 5 temperatures are chosen. From $-40℃$ to $125℃$, the operating frequency is about $20\sim60$kHz. It is not much fast speed, so we don't need to consider the error caused by comparator delay.

Delay also can be dependent with temperature. At high VDD, mobility dominates the delay, and at low VDD, threshold variation dominates delay. As a result, Delay is proportional with temperature if VDD is high and inverse-proportional with VDD if VDD is low. However, delay is pico units, and as I mentioned, the output frequency is about 20~60kHz, so comparator can't be a major error source of temperature sensor.

T	t1	t2	t3	t4	t5	t2-t1	t3-t2	t4-t3	t5-t4	Average	mhu	Tmea	error
-40	735.98	778.24	820.73	863	905.49	42.26	42.49	42.27	42.49	42.378	0.4422	-40.506	-0.5065
-35	757.88	799.09	840.09	881.3	922.29	41.21	41	41.21	40.99	41.103	0.4497	-35.261	-0.2608
-30	738.33	778.31	818.09	858.07	897.84	39.98	39.78	39.98	39.77	39.878	0.4572	-30.049	-0.0493
-25	719.55	758.35	796.95	835.75	874.35	38.8	38.6	38.8	38.6	38.7	0.4647	-24.873	0.1266
-20	701.5	739.16	776.63	814.3	851.77	37.66	37.47	37.67	37.47	37.568	0.4721	-19.734	0.2663
-15	757.09	793.66	830.04	866.62	903	36.57	36.38	36.58	36.38	36.478	0.4794	-14.63	0.37
-10	773.8	809.14	844.66	879.99	915.51	35.34	35.52	35.33	35.52	35.428	0.4867	-9.5612	0.4388
-5	789	823.5	857.83	892.33	926.65	34.5	34.33	34.5	34.32	34.413	0.494	-4.5125	0.4875
0	803.11	836.46	869.98	903.33	936.86	33.35	33.52	33.35	33.53	33.438	0.5012	0.4812	0.4812
5	783.44	815.84	848.42	880.82	913.4	32.4	32.58	32.4	32.58	32.49	0.5083	5.4752	0.4752
10	732.78	764.43	795.93	827.58	859.07	31.65	31.5	31.65	31.49	31.573	0.5155	10.45	0.4495
15	715.3	746.07	776.67	807.44	838.05	30.77	30.6	30.77	30.61	30.688	0.5226	15.382	0.3822
20	787.97	817.71	847.61	877.36	907.26	29.74	29.9	29.75	29.9	29.823	0.5297	20.336	0.3364
25	827.15	856.06	885.12	914.03	943.09	28.91	29.06	28.91	29.06	28.985	0.5368	25.264	0.2636
30	835.58	863.82	891.91	920.15	948.25	28.24	28.09	28.24	28.1	28.168	0.5439	30.202	0.202
35	816.07	843.51	870.82	898.26	925.56	27.44	27.31	27.44	27.3	27.373	0.551	35.132	0.1316
40	797.72	824.39	850.92	877.58	904.12	26.67	26.53	26.66	26.54	26.6	0.5581	40.046	0.0463
45	832.18	858.08	883.86	909.77	935.54	25.9	25.78	25.91	25.77	25.84	0.5652	45.006	0.0063
50	864.59	889.76	914.8	939.96	965.01	25.17	25.04	25.16	25.05	25.105	0.5723	49.925	-0.0748
55	870.57	894.9	919.34	943.67	968.11	24.33	24.44	24.33	24.44	24.385	0.5794	54.865	-0.1354
60	804.76	828.39	852.13	875.75	899.49	23.63	23.74	23.62	23.74	23.683	0.5865	59.804	-0.1962
65	811.3	834.35	857.29	880.34	903.28	23.05	22.94	23.05	22.94	22.995	0.5936	64.756	-0.2439
70	839.27	861.65	883.92	906.3	928.57	22.38	22.27	22.38	22.27	22.325	0.6008	69.7	-0.3004
75	841.44	863.06	884.78	906.39	928.11	21.62	21.72	21.61	21.72	21.668	0.6079	74.667	-0.3326
80	861.86	882.84	903.91	924.89	945.97	20.98	21.07	20.98	21.08	21.028	0.615	79.618	-0.3822
85	880.06	900.41	920.86	941.21	961.65	20.35	20.45	20.35	20.44	20.398	0.6222	84.606	-0.3944
90	856.7	876.43	896.27	916	935.83	19.73	19.84	19.73	19.83	19.783	0.6294	89.588	-0.4119
95	872.18	891.32	910.55	929.68	948.91	19.14	19.23	19.13	19.23	19.183	0.6365	94.561	-0.439
100	867.13	885.76	904.31	922.95	941.5	18.63	18.55	18.64	18.55	18.593	0.6437	99.563	-0.4375
105	843.34	861.39	879.37	897.42	915.4	18.05	17.98	18.05	17.98	18.015	0.6509	104.57	-0.4311
110	872.43	889.84	907.33	927.74	942.23	17.41	17.49	20.41	14.49	17.45	0.6581	109.58	-0.4235
115	864.83	881.76	898.62	915.55	932.41	16.93	16.86	16.93	16.86	16.895	0.6654	114.6	-0.3954
120	873.01	889.4	905.71	922.1	938.41	16.39	16.31	16.39	16.31	16.35	0.6726	119.65	-0.3492
125	879.53	895.38	911.16	927.01	942.79	15.85	15.78	15.85	15.78	15.815	0.6799	124.71	-0.2873

Figure 4.5 Digital conversion table

After frequency is measured, period information will be converted to digitized temperature information. Figure 4.3 is a conversion table from period to temperature. At the simulation, measurement with counter is hard so 4 periods are measured. With that 4 period, average period is used. Finally, the last column values represent the temperature error.

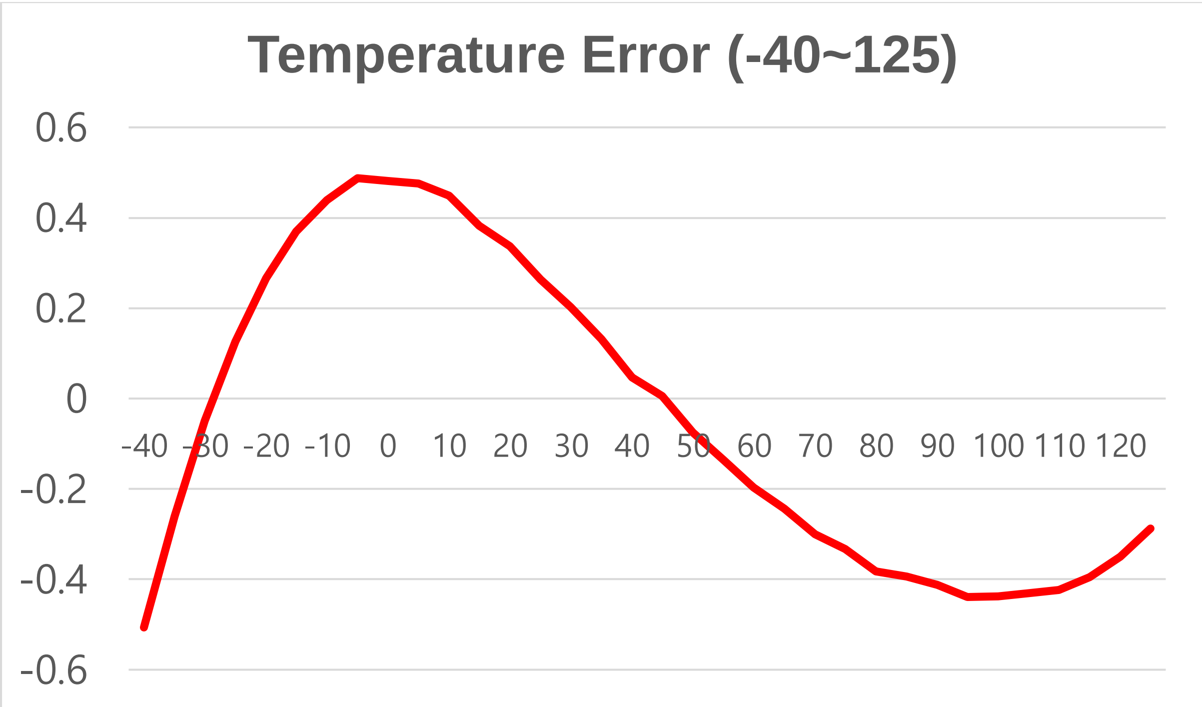

Figure 4.6 Temperature error graph

Figure 4.4 is the temperature error graph which is derived from Figure 4.3 table. Its operation range is $-40\sim125$℃ and the error is about ±0.5℃. This error will be compared with the measurement error later. The curvature is observed in the graph. There can be some reasons, but main two reason is because of the BJT and resistor. BJT has its curvature. With PTAT current biasing, curvature can be compensated but it is not enough. Resistor can cause curvature. Zero TC resistor is integrated, but its second order TC is not considered. This curvature is broadly observed among the BJT based temperature sensor.

4.3 Measurement results with optimizing α

At the previous section, the simulation results and the expected errors and tendency are shown. After tape-out, and measurement is done. The measurement principle without bandgap reference will be shown.

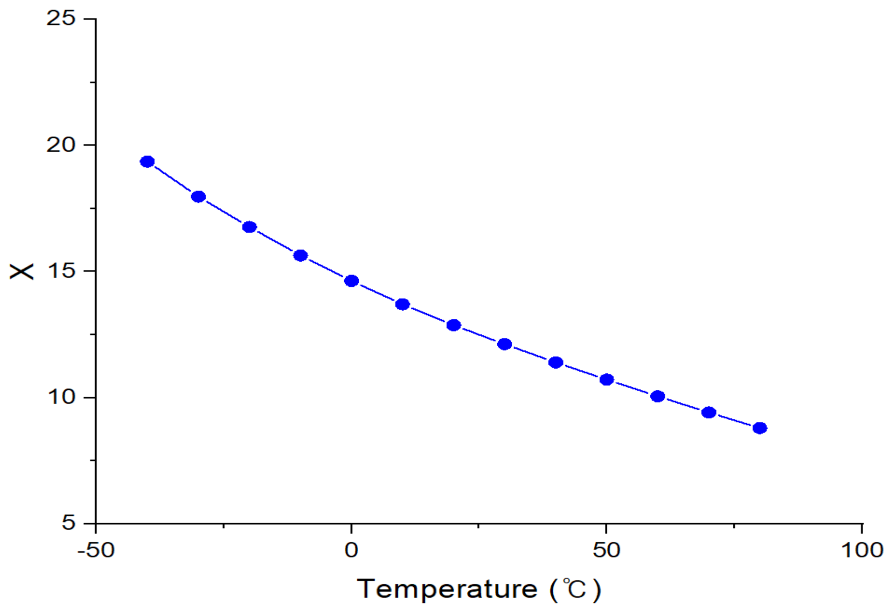

Figure 4.7 X($\frac{Vbe}{\Delta Vbe}$) values with temperature change

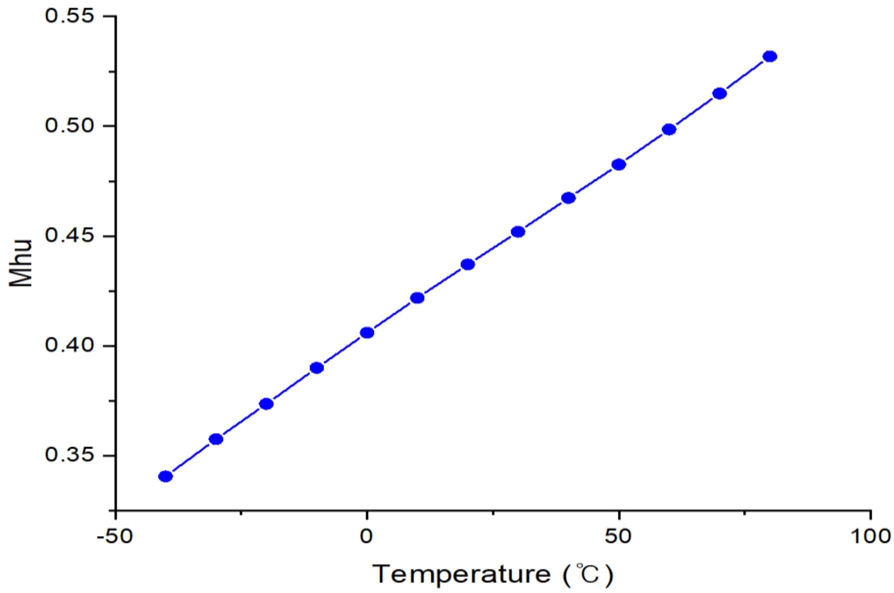

Figure 4.8 Mhu values with temperature change

Figure 4.5 represents the X value with temperature change. At the bias stage, current ratio is 7:1. With that ratio, $\frac{Vbe}{\Delta Vbe}$ ratio will be from 6~19 at $-40\sim125$℃. The X value cannot be changed. However, for linearizing X, α can be a designer's choice. Using α, the linearization equation can be changed so total error will change too. At the simulation, the optimized α was 12.5. The pros of this measurement principle is that the errors can be compensated by adjusting α. For example, Errors can be caused by capacitor spread or sheet resistance variation. Temperature circuit's composite resistor is 120K ohm, and the capacitor is 20pF. If real values are different with expectation, errors can be represented in digitized temperature. However, with α adjustment, this error can be compensated. With α adjustment at the back stage, bias circuit becomes simpler, and the error source can be compensated.

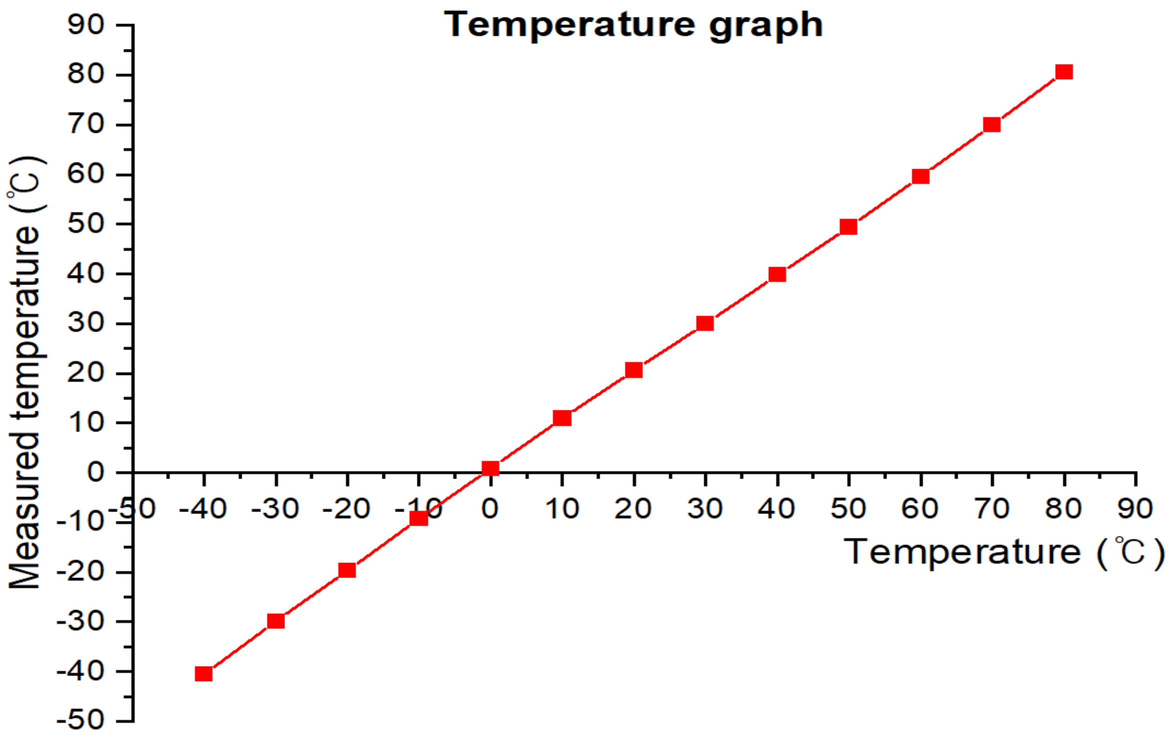

Figure 4.9 Temperature measurement with full range

After α optimization, the overall temperature will be measured as Figure 4.7. Its slope seems like linear from −40~125℃. For checking exact errors, temperature error graph will be shown.

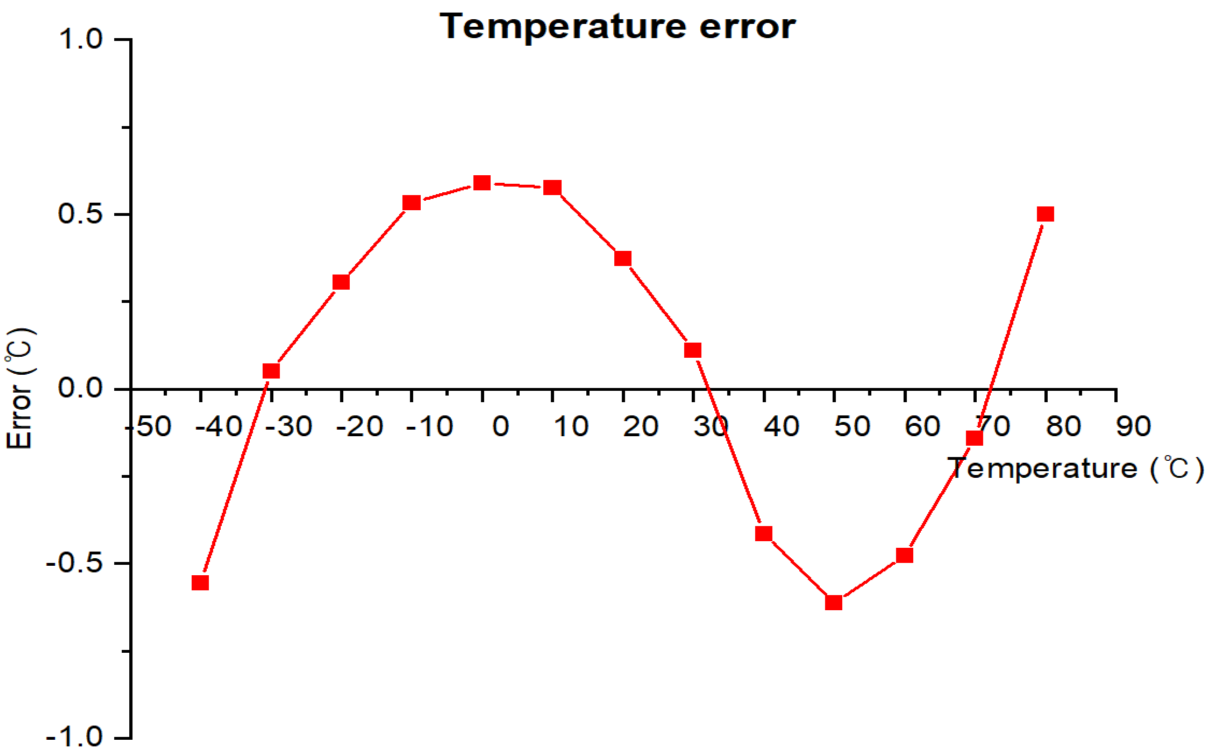

Figure 4.10 Measurement temperature error

Figure 4.8 represents temperature error with full range. At the simulation, total range was $-40\sim125$℃. At high temperature, the readout circuit does not operate completely. Glitch is measured, so the counter cannot measure exact period.

However, the errors from $-40\sim80$℃ is measured well. Its inaccuracy is about ±0.6℃. The optimized α is 9.7. After mhu is calculated, the linearization constant A and B also need to be selected. At this measurement, A is 637 and B is -253.

At the simulation, inaccuracy is about ±0.5℃ and the measurement inaccuracy is about ±0.6℃. The difference is not considerable. However, if we think about this difference, 2 factors can be a cause. First, resistor is not exact zero temperature coefficient resistor. Resistors have second-order TC, and sheet resistance variation can generate error. BJT non-linearity can also be a error source. There is one more factor. In simulation, optimized α is the 2nd digit after decimal point number. However, at the measurement, optimized α is the 1st digit after decimal point number, so error will be worse at the measurement.

Chapter 5. Conclusions and further works

5.1 Comparison table

	This work	[1] 2014 ISSCC	[2] 2005 JSSC	[3] 2017 TCAS2	[4] 2015 ISCAS	[5] 2011 VLSI
Sensing core	BJT	BJT	BJT	MOSFET	MOSFET	Resistor
Readout type	Relaxation oscillator	Relaxation oscillator	Delta-sigma	Delta-sigma	Relaxation oscillator	SAR ADC
Technology	$0.11um$	$0.7um$	$0.5um$	$0.18um$	$0.18um$	$0.18um$
Chip area	$0.05mm^2$	$0.8mm^2$	$2.5mm^2$	$0.089mm^2$	$0.122mm^2$	$0.18mm^2$
Supply voltage	1.6-2.1V	2.9-5.5V	2.7-5.5V	1.8V	1.8	1.2-2V
Supply current	18uA	55uA	130uA	0.46uA	.	20uA
Temperature range	$-40\sim80$℃	$-45\sim130$℃	$-50\sim125$℃	$-20\sim80$℃	$-40\sim120$℃	$0\sim100$℃
Inaccuracy	±0.6℃	±0.15℃	±0.3℃	±1℃	±0.85℃	±0.5℃

Figure 5.1 Comparison table

In comparison table, 5 temperature sensor comparisons are shown. First 2 types are BJT based sensor. First one is ISSCC paper and it is published at 2014. Second one is JSSC paper and it is published at 2005. Their readout is based on relaxation oscillator and delta-sigma respectively. Its accuracy performance is better than mine. However, my initial target was to make power and area efficient temperature sensor.

Next 2 papers are MOSFET based temperature sensor. Their readout is also based on delta sigma and relaxation oscillator. Proposed temperature sensor's sensing core is BJT based so its accuracy performance is better than 2 previous works. In power and area, it shows similar performance. Finally, if we compare it with resistor based temperature sensor, it shows similar accuracy and similar power. However proposed temperature sensor is power efficient temperature sensor.

5.2 Conclusions

With relaxation oscillator based readout circuit, CMOS smart temperature sensor is utilized. Conventional temperature sensor compares the temperature dependent voltage (Amplified PTAT voltage) with temperature independent voltage(Bandgap reference). However, α-implementation in the circuit can increase power consumption and complexity, so that's why comparing CTAT voltage with PTAT voltage is considered. This method can adjust α at the back stage, so it makes circuit simpler. Not only simplicity but also error compensation can be given. With adjusting α, other error sources can be compensated.

For simple readout circuit, relaxation oscillator based readout circuit is utilized. However, it has three main error sources. Comparator offset, comparator delay, and reset time. To overcome this obstacles, I operate the readout circuit with capacitor flipping. With this technique, offset is cancelled except for the first phase of the first oscillation. We don't have to consider comparator delay because the frequency is slow. Conventional relaxation oscillator has only 1 capacitor, so reset time after integration can be error. However, this circuit doesn't have to reset capacitor. We don't have to use 2 capacitors for considering reset time.

After measurement, the total temperature range is $-40\sim80$℃ and the inaccuracy is about ±0.6℃. For the error compensation at the bias circuit, DEM and chopping technique is utilized. DEM is utilized for reducing the current mirror mismatch and chopping is utilized for compensate the offset of comparator at the bias stage. These techniques need clock signals, so it can be a power burden. However, this temperature sensor is relaxation oscillator based so it doesn't need output clock signal. It can be self-clocked.

5.3 Further works

The measurement was done at March so time was too short. Additional measurements are required for trying paper. First, Offset cancellation effect verification is required. I have one more temperature sensor. Its readout structure is same with the relaxation oscillator which is mentioned at the previous chapter. Their bias stage is same so if it shows similar performance, offset cancellation is proved.

Chip variation error measurement is also required. I think chip variation error performance will be good because temperature sensor can be corrected digitally, but the result is needed. VDD variation error measurement is also necessary.

Building system for automation is necessary. From now, I do the measurement by hand-calculation. Using some functions, digitized temperature can be shown automatically.

Chapter 6. References

[1] 48, no. 1, pp. 292-301, Jan. 2013.K. A. A. Makinwa, "Smart Temperature Sensor Survey," [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

[2] K. Souri, M. Kashmiri, and K. Makinwa, "A CMOS temperature sensor with an energy-efficient zoom ADC and an inaccuracy of ±0.25°C (3σ) from -40°C to 125°C," *IEEE ISSCC*

[3] K. Souri, *et al.*, "A CMOS Temperature Sensor with a Voltage Calibrated Inaccuracy of ±0.15°C (±3σ) from -55 °C to 125 °C," *J. Solid-State Circuits*, vol.

[4] A. Heidari, G. Wang, K. A. A. Makinwa, and G. C. M. Meijer, "A BJT based CMOS temperature sensor with a 3.6 pJK2 resolution FOM," in *Dig.Tech. Papers IEEE Int. Solid-State Circuits Conf.*, Feb. 2014, pp. 224–225.

[5] G. Wang, A. Heidari, K. A. A. Makinwa and G. C. M. Meijer, "An Accurate BJT-Based CMOS Temperature Sensor With Duty-Cycle-Modulated Output," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 2, pp. 1572-1580, Feb. 2017, doi: 10.1109/TIE.2016.2614273.

[6] A. Paidimarri, D. Griffith, A. Wang, G. Burra and A. P. Chandrakasan, "An RC Oscillator With Comparator Offset Cancellation," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1866-1877, Aug. 2016, doi: 10.1109/JSSC.2016.2559508.

[7] C. Wu, W. Chan and T. Lin, "A 80kS/s 36µW resistor-based temperature sensor using BGR-free SAR ADC with a unevenly-weighted resistor string in 0.18µm CMOS," *2011 Symposium on VLSI Circuits - Digest of Technical Papers*, Honolulu, HI, 2011, pp. 222-223.