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ULSAN NATIONAL INSTITUTE OF
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Master's Thesis

Indirect Time-of-Flight Sensor with In-pixel Adaptable Background Light Suppression Based on Delta-Sigma Technique

Dahwan Park

Department of Electrical Engineering

Graduate School of UNIST

2020

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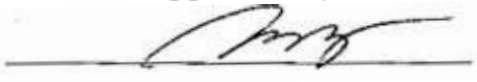
A thesis
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Master of Science

Dahwan Park

06 / 01 / 2020

Approved by



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Indirect Time-of-Flight Sensor with In-pixel Adaptable Background Light Suppression Based on Delta-Sigma Technique

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List of abbreviations

Number	Abbreviation	Word & Phrase
1	CIS	CMOS image sensor
2	IToF	Indirect Time-of-Flight
3	DToF	Direct Time-of-Flight
4	SPAD	Single-photon avalanche diode
5	PPD	Pinned photodiode
6	BL	Background light
7	IR	Infrared radiation
8	APD	Avalanche-diode
9	BLS	Background light suppression
10	SR	Smart reset
11	BR	Bridge
12	FD	Floating diffusion
13	CDS	Correlated double sampling
14	QE	Quantum efficiency
15	CTIA	Capacitive trans-impedance amplifier
16	PSR	Phase shift readout
17	FWD	Forward
18	BWD	Backward
19	CS&H	Current sample and hold
20	ALC	Ambient light cancellation
21	TX	Transfer gate
22	OB	Optical black
23	DDS	Delta double sampling
24	FWC	Full well capacity

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ACKNOWLEDGEMENT

I would like to thank all people that help me to forward my research about semiconductor engineering.

First of all, I really appreciate with my advisor, Prof. Kim. He encouraged me when I was frustrated and always supported me to immerse myself in research. He accepted me as a intern when I was senior student in UNIST. I couldn't decide which field to research before I entered BIAS laboratory. Thanks to my professor, I became interested in image sensors and could immerse myself in research.

Secondly, I would like to appreciate my master's thesis committee members, Prof. Jaehyouk Choi and Prof. Kyuho Lee for giving great lectures for analog and digital circuit. In addition, thanks for taking the time for evaluating my master thesis.

Third, I would like to appreciate my laboratory members who spent the most time together in my master course. I would like to thank Bumjun Kim who teaches basic knowledgement and principle of image sensor. Jihyoung Cha is a head of our laboratory and thanks for helping me to adjust my laboratory life. Minsu Goo is my first junior in the laboratory. I took discussion about hard paper frequently with him. Next, Jubin Kang is my second junior in the laboratory. I tried to take care of him and he helped me. I believe that he can do well in his research because he is sincere. Thanks to Seonghyouk Park who is smart and have been working together recently. Next, Thanks to Suhyun Han who has positive mind. It helped for brightening the atmosphere of the laboratory. Jeeho Park teaches me very much when I was intern. I really appreciate with him. Changyong Shin and Yongjae Park are my colleague. Changyong Shin will graduate with me. I appreciate with him and I wish him well in his career. Yongjae Park is very brilliant colleague and his circuit approach is an inspiration to me.

Finally, I would like to thank my family members who lead me a good way for my life. My father, Sangeun Park is a head of household. Since I was young, he always tried hard to grow me up in a good environment. Thanks to my father, I could set direction of my life. My lovely mother, Eonju Lee always cheered and encouraged me to research. I really appreciate my mother for always encouraging me no matter what happens. My older brother, Jihwan Park is abroad now for studying English. I appreciate my brother for encouraging me by voice talk when I was frustrated. Lastly, I really appreciate all of the people around for encouraging me.

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Abstract

Entering the era of the fourth industrial revolution (4IR), interest about camera is growing rapidly. The demand for detecting range has been increased by consumer of electronics applications such as gesture recognition like kinect gaming and robotic vision. The depth sensing technology can be classified into 2 types. One is sensing with optical sources and the other is sensing without optical sources. The most popular approaches include radar and time-of-flight (TOF) sensing systems.

In the non-optical sensing category, the well-known radar range-finding system utilizes the radio waves to measure the range. Radar is the abbreviation of radio detection and ranging. Literally, this system uses radio wave for detecting the range and it consists of receiving part and transmitting part which produces electromagnetic waves. However, this systems is weak on spatial resolution. Because large array size receiver is hard to be materialized.

Time-of-flight (ToF) principle is measuring distance based on time difference between emitted light wave and reflected light wave. ToF is classified 2 types; direct-ToF (dToF) and indirect-ToF (iToF). The direct-ToF is measurement of the time delay between emitted light and reflected light, while indirect-ToF is measurement of the phase delay of a periodic waveform. In direct ToF system, single-photon avalanche diode (SPAD) is the most commonly used sensing device because of high sensitivity and fast responsivity.

In this research, the proposed sensor is implemented to iToF structure with depth calculation using phase shift. It has 4 advantages compared to previous ΔΣ based background light suppression i-ToF. As modulation frequency increases, switching noise becomes more dominant. Therefore, to reduce unnecessary switching noise, smart adaptable ΔΣ operation is proposed. Process variation is one of the factors causing depth error. To compensate process variation, in-pixel automatic chopping controller is proposed. Additionally, to increase background suppression capability, all pixel include individual integrator for global ΔΣ operation in pixel and pinned photodiode is implemented for high electron transfer speed. This chip is fabricated with a 0.11um DBH CIS process.

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Chapter 1. Introduction

1.1 Range detection methods overview

There are 2 types of range detection methods. First is non-injection type such as stereo vision. Second is optical injection type such as triangulation, interferometry and time-of-flight. The basic principles of non-injection 3 techniques for range detection are summarized in this chapter.

1.1.1 Triangulation

The triangulation is range detection technique which determines the coordinates and distances of any single point through a trigonometric function using the properties of the triangle. The distance of the object can be determined by measuring angles. This is shown in figure 1.1. Triangulation systems are useful for various applications because its distance range is very discursive, but it needs a large triangulation base. Therefore, it is not easy to set a system without restrictions.

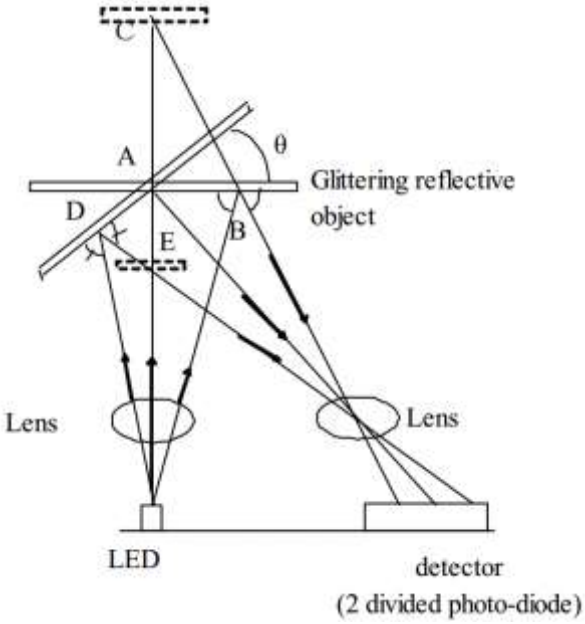

Figure 1.1 Triangulation diagram

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1.1.2 Interferometry

Figure 1.2 The Michaelson Interferometer system Interferometry is a method of interpreting short-length photovoltaic field measurements or line spectrum using two light interference. In figure 1.2, coherent light source emits light to a mirror and reflected light pass interferometer and reflected again to a reference mirror and comes in detector. This technique can be considered as a time-of-flight principle. Because measuring runtime difference is same between interferometry and time-of-flight. However, this systems have two drawbacks. First thing is that complexity of this system is very high and second thing is that maximum detect range is limited.

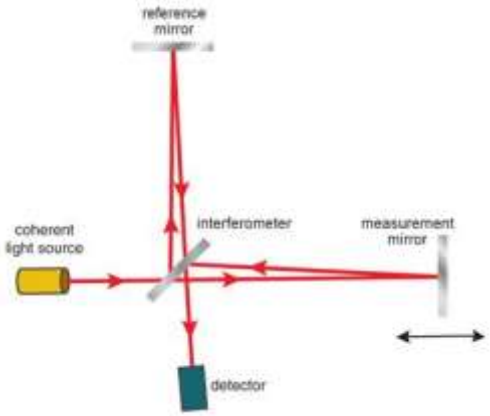

Figure 1.2 The Michaelson Interferometer system

1.1.3 Time-of-Flight

Time-of-Flight is a range detecting system by measuring round trip time of emitted light. Advantages of this technique are simplicity, efficient distance algorithm and speed. If signal is sampled only one time, it is impossible to distinguish the intensity of light due to various reasons such as phase motion, reflectivity due to color or surface characteristics of the object, and background. The depth information of the target is wrong according to the phase of the signal. Figure 1.3 shows ToF system diagram.

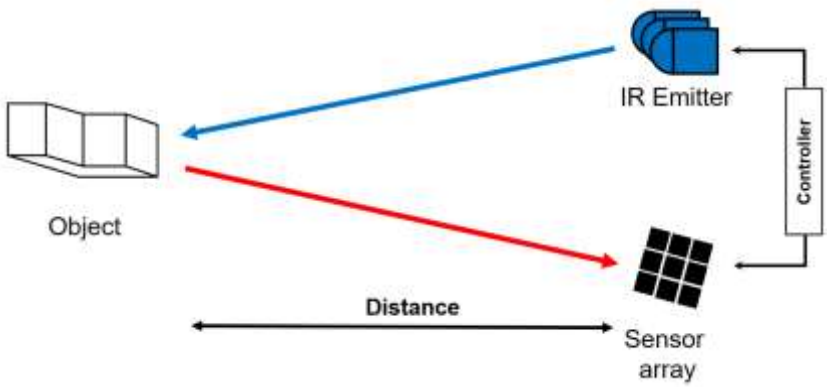

Figure 1.3 Time-of-Flight system diagram; IR emitter and photodetector

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1.2 Range detection error by Background light

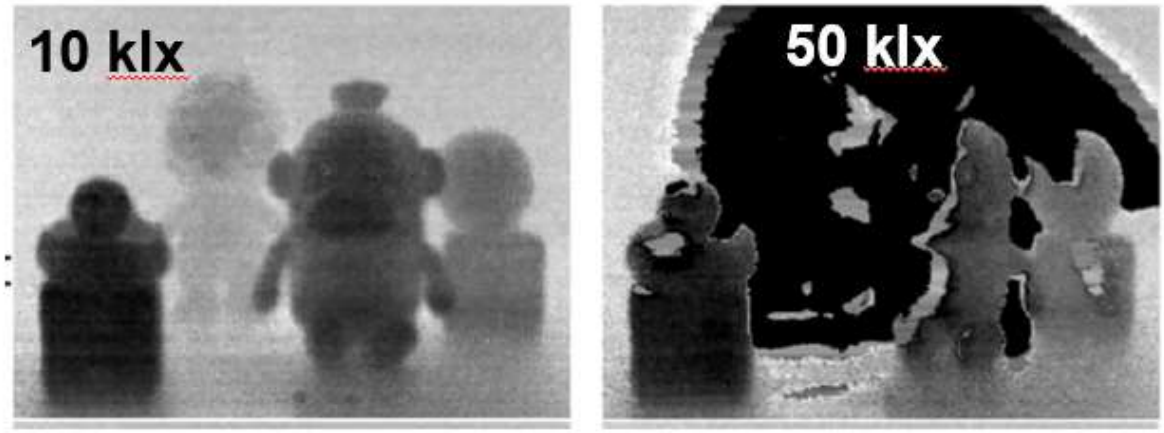

Figure 1.4 Distorted depth image in outdoor by background light

As interest in cameras increases more and more, smart phone are equipped with not only 2D camera but also 3D camera. 3D depth camera in smart phone should provide precise detection of depth independent of ambient light. In figure 1.4, right image is distorted depth image in outdoor by background light.

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Chapter 2. Time-of-Flight 3D Imaging

2.1 Principles of Time-of-Flight 3D Imaging

2.1.1 Classification of Time-of-Flight

There are 2 types of distance detection methods in Time-of-Flight. One is direct-ToF (dToF) and the other is indirect-ToF (iToF). The Time-of-Flight 3D imaging is roughly composed of 2 components, optical emitter, and photonic detectors. Both dToF and iToF systems use diodes (photonic detectors) for light signal to transfer electric signal. However, diode operation region is different between dToF and iToF. In figure 2.1, normal photodiode, avalanche-diode (APD), single-photon avalanche diode (SPAD) operate in reverse bias, but gain is different according to breakdown voltage.

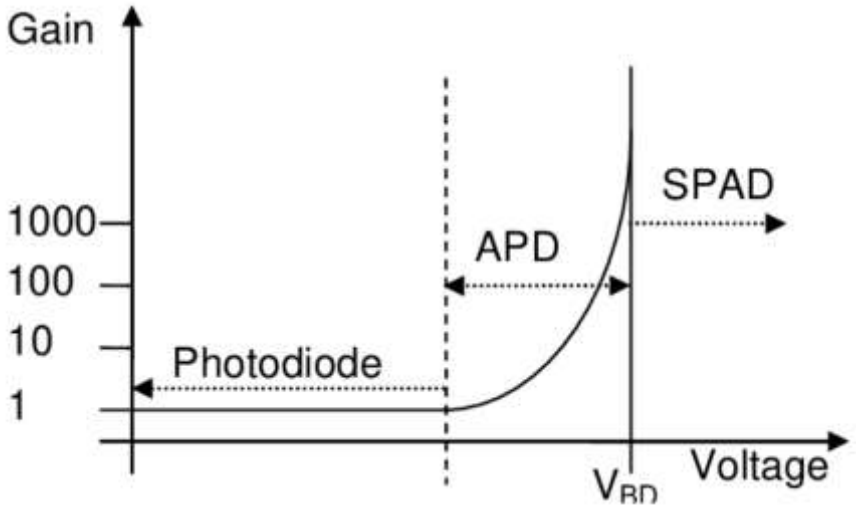

Figure 2.1 Photodiode gain variation in accordance with breakdown voltage

The direct-ToF is measurement of the time delay between emitted light and reflected light.

In direct ToF system, single-photon avalanche diode (SPAD) is the most commonly used sensing device because it can generates large current when a low light signal comes into photodiode. Therefore, it has high sensitivity and can detect long distance of over 20m. However, it has fatal drawback on spatial resolution. SPAD requires guard-ring to suppress unintended avalanche current around diode and needs deep N-well for isolating from circuit in pixel. [1] - [4].

On the other hands, indirect-ToF is measurement of the phase delay of a periodic waveform. Sensor array read out phase difference between modulated emitted signal and light signal which is reflected on object.

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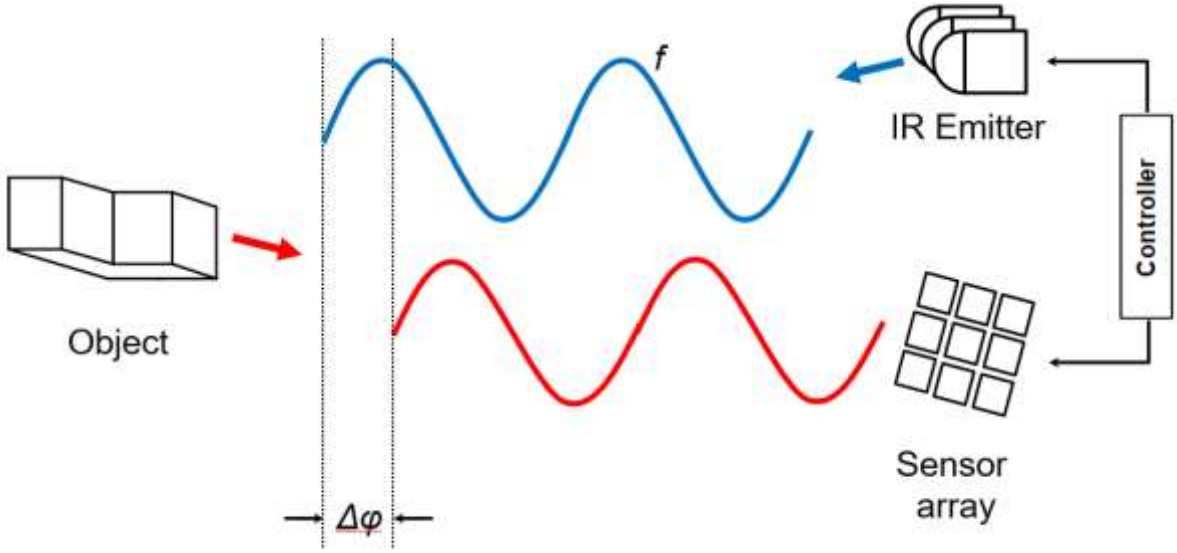

Figure 2.2 Basic principle of indirect Time-of-Flight 3D imaging system.

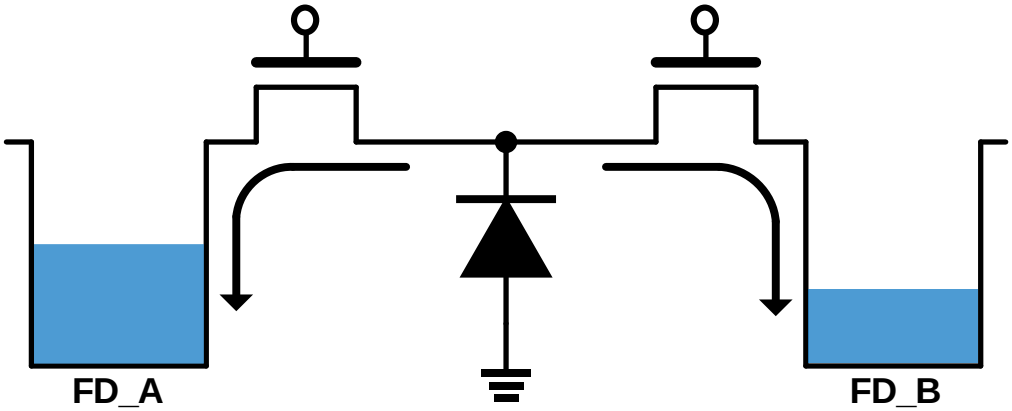

Figure 2.3 Demodulation operation of sensor

Figure 2.2 shows the principle of indirect Time-of-Flight. IR emitter emits modulated light to object and sensor receives phase-shifted light reflected to object. Figure 2.3 shows that received light signal is demodulated to in-phase signal and out-phase signal by switching operation and calculated as range data. To get 2 different phase information, sensor and emitter is synched in the indirect-ToF system.

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2.1.2 Distance detection by phase difference between emitted and reflected light

Emitted light is reflected from the target object. Reflected light amplitude is smaller than emitted light because light amplitude is inversely proportional to distance squared. Demodulation of reflected light can be calculated by correlation function between emitted light and reflected light. We assume reflected signal s(t) = 1+ a · $\cos(\omega t - \varphi)$ and correlation signal g(t) = cos(ωt).

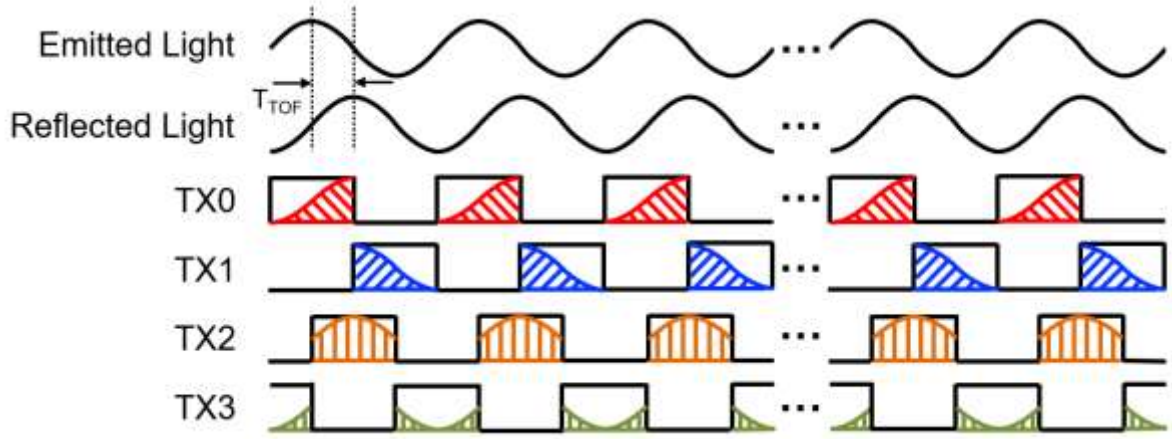

Figure 2.4 Phase measurement of Time-of-Flight 3D imaging system.

$$c(\tau) = \varphi(\tau) = [1 + a \cdot \cos(\omega t - \varphi)] \otimes [\cos(\omega t)]$$
$$= \lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} [1 + a \cdot \cos(\omega t - \varphi)] \cdot [\cos(\omega t + \tau)] dt$$
$$= \frac{a}{2} \cdot \cos(\omega t + \varphi)$$

Additionally, we add a constant indicating offset B by background light and choose 4 phase information ($0°, 90°, 180°, 270°$). Considering above condition, 4 phase data are shown below.

$$C(0°) = c(0°) = \frac{a}{2} \cdot \cos(\varphi) + B$$
$$C(90°) = c(90°) = -\frac{a}{2} \cdot \sin(\varphi) + B$$
$$C(180°) = c(180°) = -\frac{a}{2} \cdot \cos(\varphi) + B$$
$$C(270°) = c(270°) = \frac{a}{2} \cdot sin(\varphi) + B$$

With this 4 phase signal, we can calculate phase shift φ and distance from phase shift [5]

$$\varphi = \arctan\left(\frac{c(270°) - c(180°)}{c(90°) - c(0°)}\right)$$
$$D(\text{distance}) = \frac{c}{4\pi f} \arctan\left(\frac{c(270°) - c(180°)}{c(90°) - c(0°)}\right)$$

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2.2 Correlation between background light and depth image

Depth calculation by 4 phase measurement is appropriate on both case with background light and without background light. Because background light signal is DC signal and in-phase background amount is same with out-phase background amount, so it is removed when subtracted.

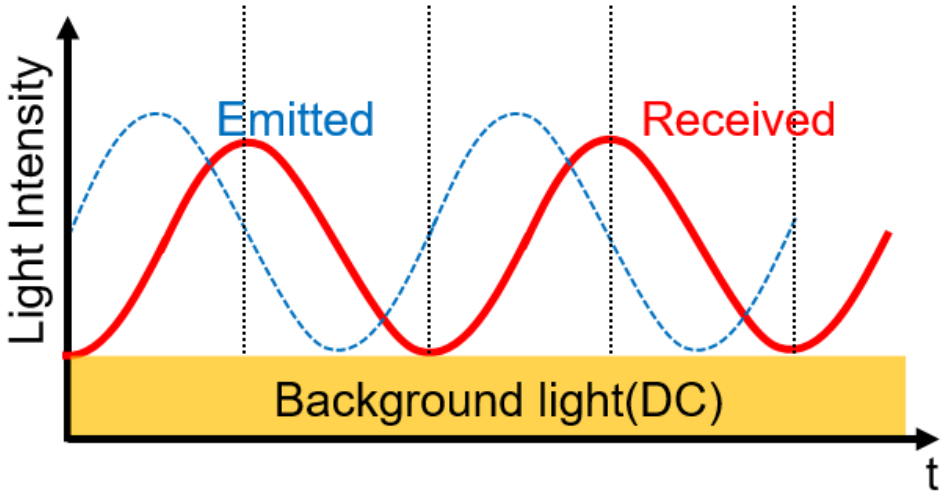

Figure 2.5 Emitted light and reflected light intensity when background light exists

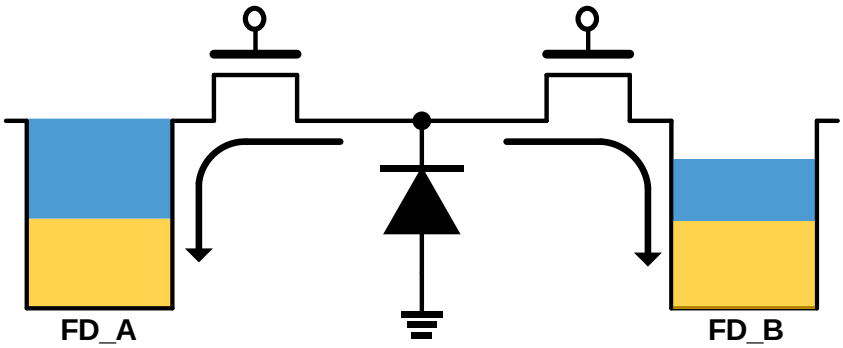

Figure 2.6 Signal distortion by background light in saturation case

However, depth error occurs when background light (BL) is strong. In figure 2.6, during integration time, if storage node (FD) is saturated early by high BL, signal is distorted by BL. To solve this problem, subtract in-phase signal and out-phase signal frequently when strong background light before storage node is saturated.

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2.3 Conceptual ideas of background light suppression

There are many factors causing background light. It could be sunlight in outdoor and could be fluorescent lamp. In case of high background light, if the signal is saturated by background light, sensor can't measure phase difference. In this case, it will be noise element and it will cause depth error. Therefore, Suppressing background light is mainly caused subject in ToF sensor. Figure 2.7 introduces 4 types of suppressing background light signal. Background light is DC signal, so BL added on out-phase signal is same with BL added on in-phase signal. Because in-phase pulse width and out-phase pulse width is same.

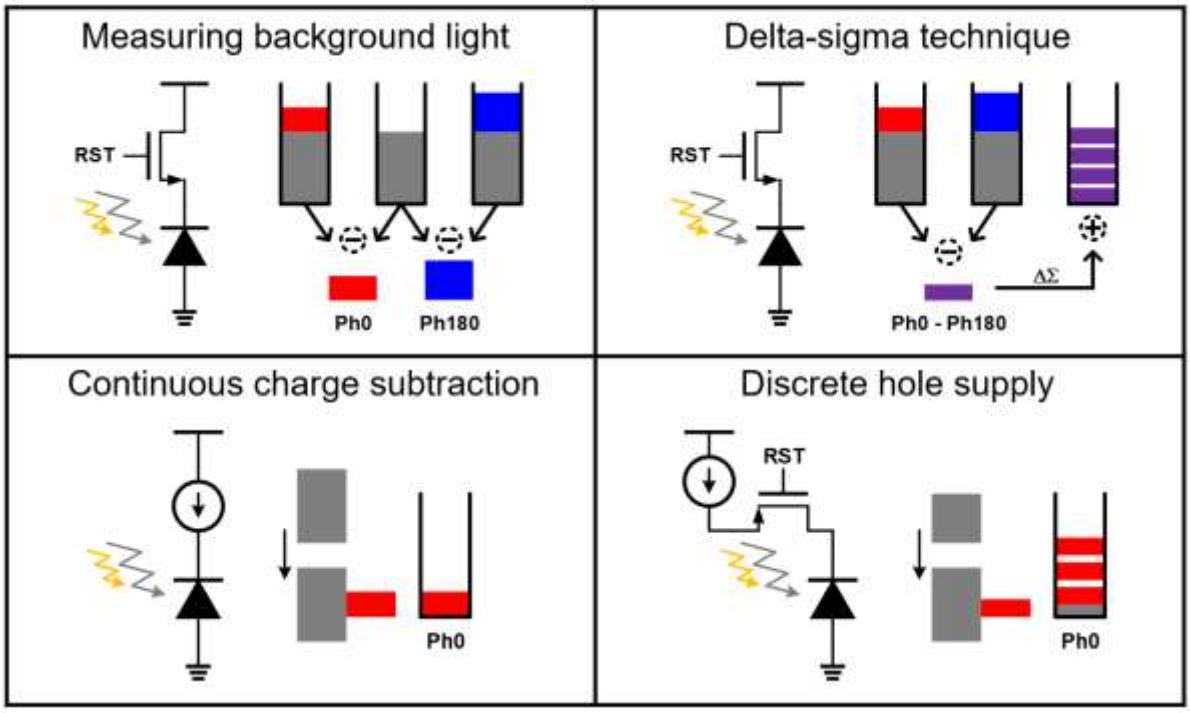

Figure 2.7 Conceptual 4 types of background light suppression

First method is measuring background light and subtracting same value to in-phase signal and out-phase signal. Second method is delta-sigma technique that subtracts in-phase value to out-phase value. There are 4 types of implementing delta integrator; Flipping photodiode, Flipping capacitor, Flipping CDS operation and cross-coupled capacitor. Third method is continuous charge subtraction. It is sampling photocurrent by background light and then only accumulates additional photocurrent except continuously flowing current by BL. Fourth method is randomly supplying discrete hole.

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Chapter 3.

Previous BLS techniques in iToF depth sensor

3.1 Measuring background light and subtraction scheme

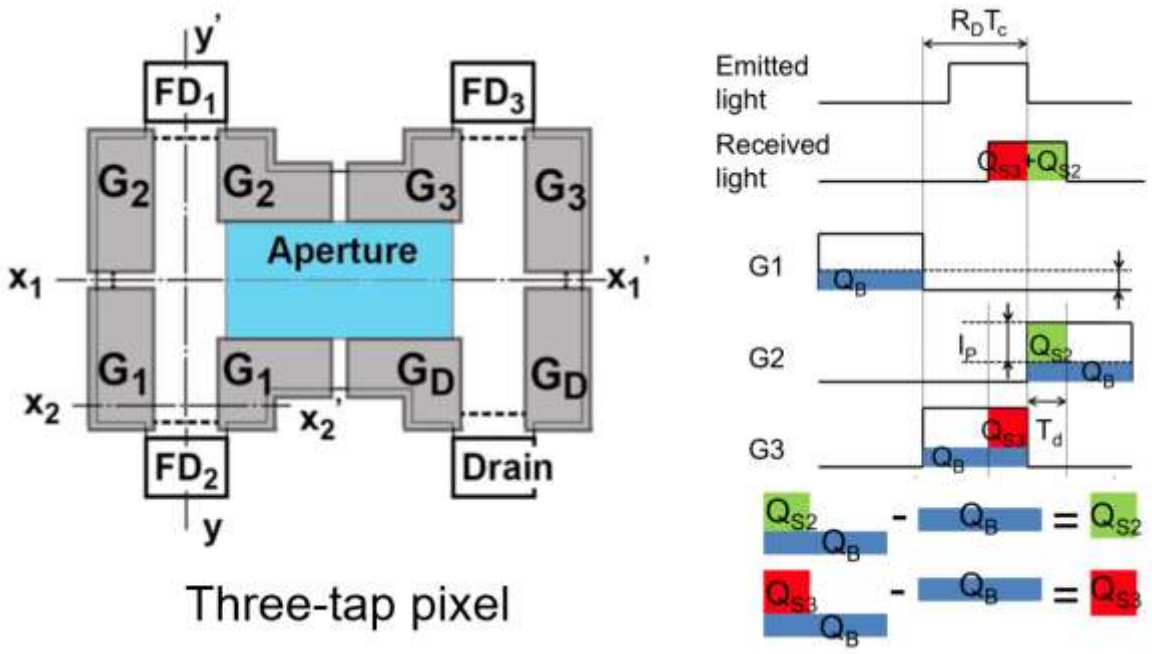

Figure 3.1 Three-tap pixel structure

Figure 3.1 is three-tap pixel structure, two-tap is used for accumulating in-phase and out-phase signal and other 1-tap is used for accumulating only background light. By subtracting the output of G1 from G2, G3, the background light can be canceled. The equation for estimating the range in each pixel is given by :

$$L = \frac{cT_0}{2} \cdot \frac{S_2 - S_1}{S_2 + S_3 - 2S_1}$$

where c is the speed of light, and S_1, S_2 and S_3 are outputs of G_1, G_2, and G_3, respectively [6].

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3.2 Delta-Sigma background light suppression scheme

3.2.1 Flipping photodiode

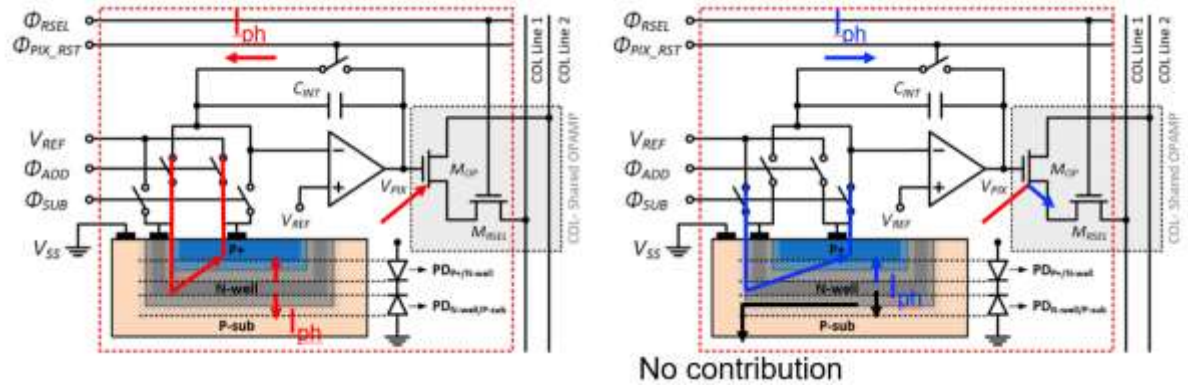

Figure 3.2 In-pixel flipping photodiode pixel structure

Figure 3.2 is in-pixel flipping photodiode pixel structure. Among the 3 types of PD (P+/N-well/P-sub, N-well/P-sub, and N+/P-sub, N-well/P-sub diode has the highest quantum efficiency (QE) and sensitivity. Each pixel has in-pixel capacitive trans-impedance amplifier (CTIA) for transferring current to voltage.

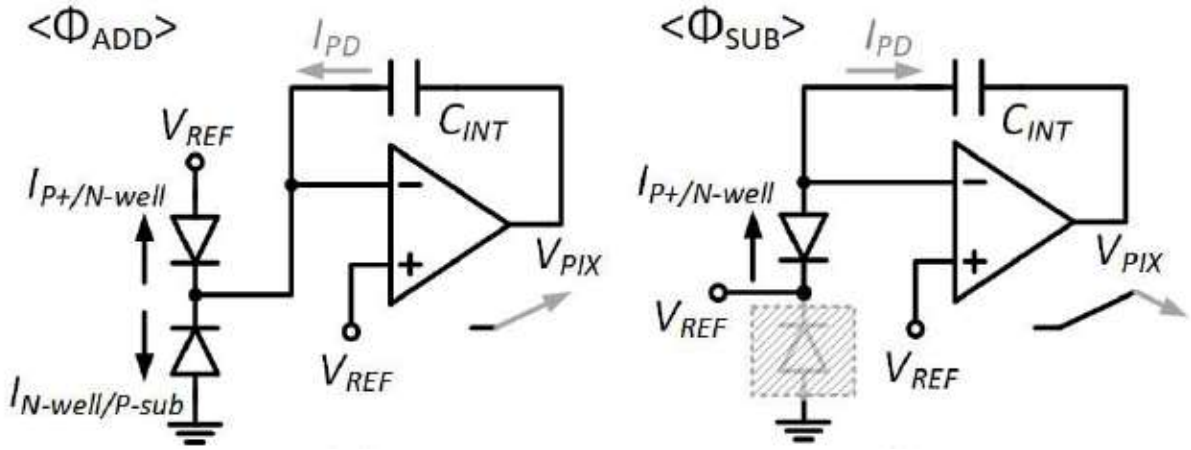

Figure 3.3 Pixel operation when add phase and subtraction phase

Figure 3.3 shows connection between photodiode and CTIA when add phase and subtraction phase. When add phase, both P+/N-well diode and N-well/P-sub diode generate photocurrent according to signal and background light. Conceptually, CTIA output voltage will increase $\Delta V_{PIX,0}$ except parasitic diode photocurrent.

$$\Delta V_{PIX,0} = \frac{1}{C_{INT}} \left(I_{P+/N-well}^{<LED>} \cdot t_0 + I_{P+/N-well}^{<BGL>} \cdot \frac{1}{2} T_{mod} \right)$$

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When subtraction phase, only P+/N-well diode generates photocurrent.

$$\Delta V_{PIX,180} = \frac{1}{C_{INT}}\left(I_{P+/N-well}^{<LED>} \cdot t_{180} + I_{P+/N-well}^{<BGL>} \cdot \frac{1}{2} T_{mod}\right)$$

After M cycles of integration, voltage difference by accumulated signal can be expressed like below.

$$\Delta V_{PIX} = M \cdot \left(\Delta V_{PIX,0} - \Delta V_{PIX,180}\right) = M \cdot \left[\frac{I_{P+/N-well}^{<LED>}}{C_{INT}} \cdot (t_0 - t_{180})\right]$$

However, parasitic diode's photocurrent will cause depth error, so phase-shift readout (PSR) technique is proposed. Nevertheless, for sampling electron generated by light to integration capacitor, switching operation may cause charge injection, so it is not suitable on high frequency operation [7].

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3.2.2 Flipping input capacitor

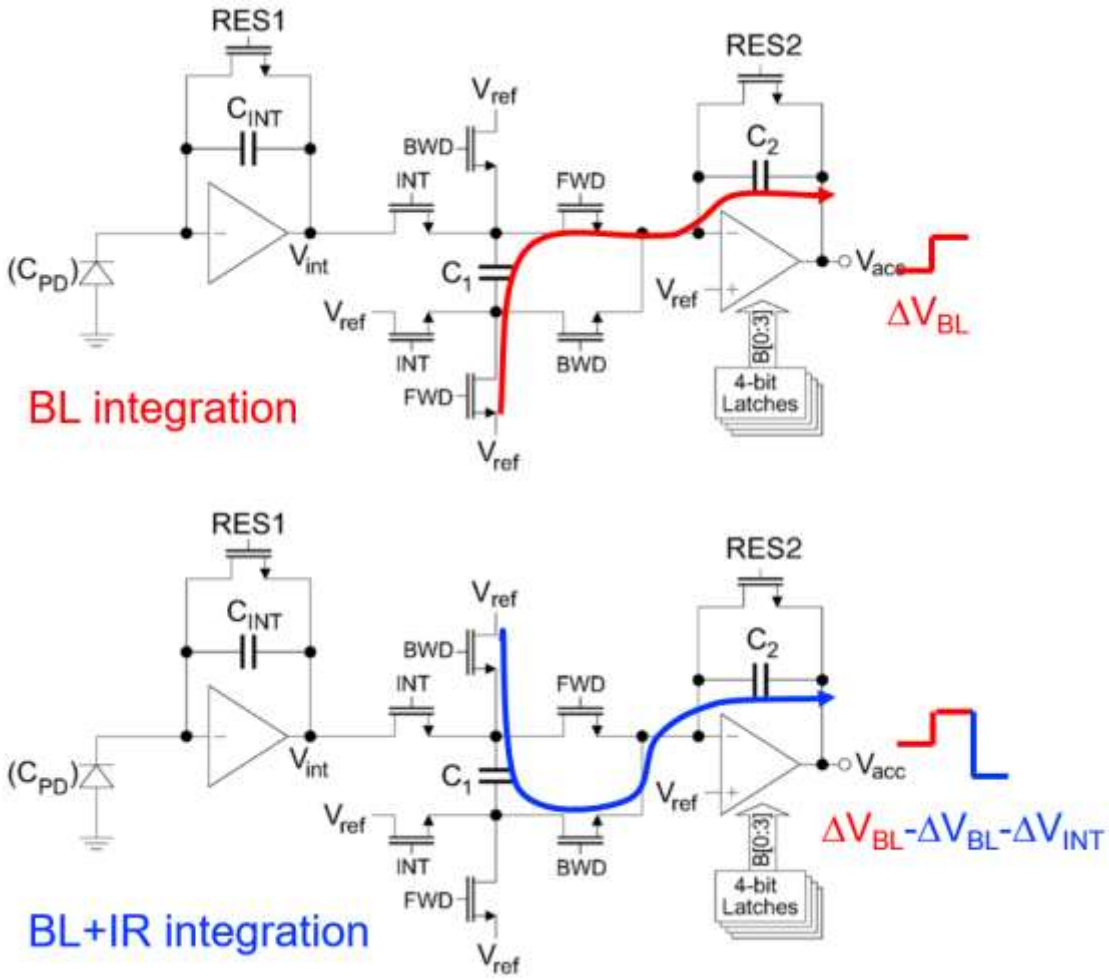

Figure 3.4 Pixel structure of flipping input capacitor with in-pixel CDS

Figure 3.4 shows pixel structure of background cancelling by flipping input capacitor using in-pixel correlated double sampling. At initial phase, only background is integrated on C_{INT} capacitor. Then, by turning on FWD switch, charge for BL signal is integrated on C_2 capacitor. At next phase, IR signal added background signal are integrated on C_{INT} capacitor. Then, by turning on BWD switch, charge for BL+IR signal is integrated, but its sign is negative. Because input capacitor's two nodes are flipped. This scheme is also not suitable for high frequency operation similar to flipping photodiode scheme because of photodiode structure [8].

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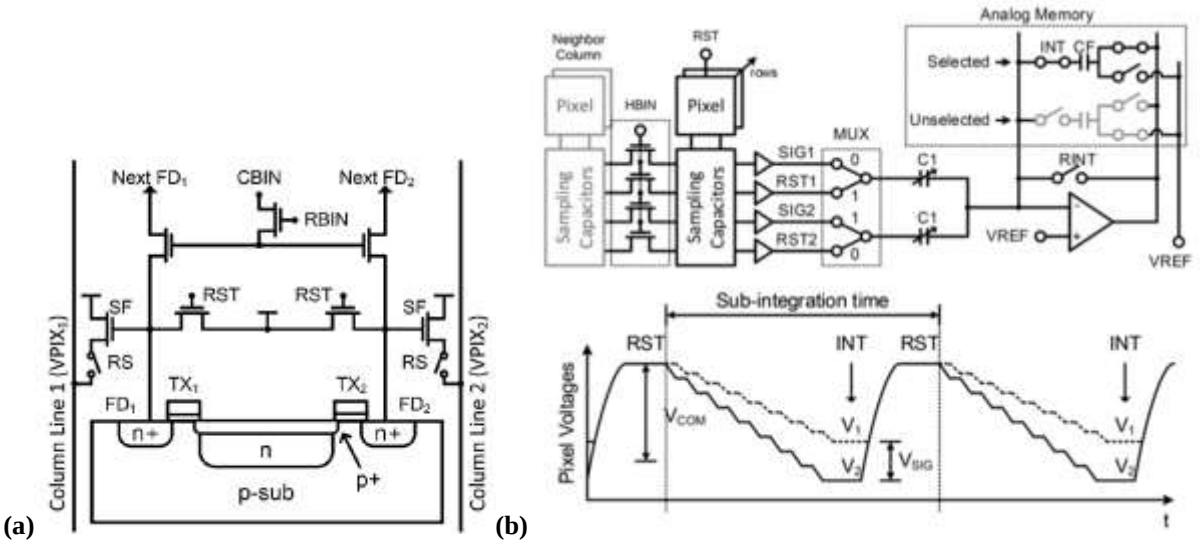
3.2.3 Flipping CDS operation



(a) **(b)**

Figure 3.5 (a) Pixel structure of column-parallel background cancelling scheme
(b) Architecture of flipping column-parallel CDS operation

Figure 3.5 (a) shows unit pixel structure which has 2 transfer gates, FD nodes, source followers, reset transistors, and row select switches. In-phase signal is read out on column line 1 and out-phase signal is read out on column line 2 and then it is connected to mux connected to column-parallel CDS input capacitors. Figure 3.5 (b) shows architecture of flipping column-parallel CDS operation. At first phase(mux value is zero), SIG1 and RST2 is connected to input capacitor's left node and then RST1 and SIG2 is serially connected as mux value is high. In this case, charge for voltage difference at input capacitor left node is sampled at C_2 capacitor.

$$\Delta V_{CF} = \frac{C1}{CF}[(RST1 - SIG1) - (RST2 - SIG2)]$$

Output voltage is voltage difference between in-phase signal + BL and out-phase signal + BL. Therefore, signal difference except only background signal is acquired. Because background signal is DC value [9].

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3.3 Continuous charge subtraction scheme

3.3.1 Sampling photocurrent by background

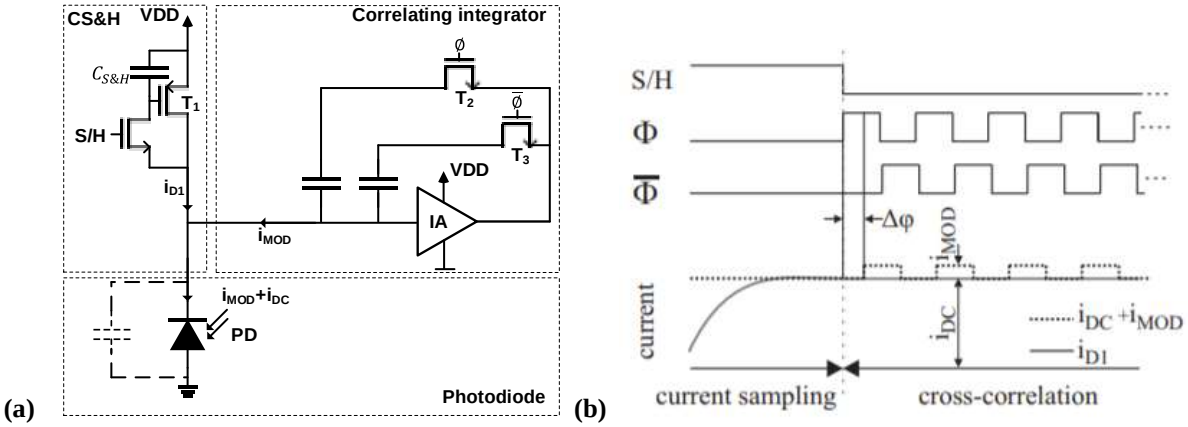

Figure 3.6 (a) Pixel structure of sampling photocurrent by background light
(b) Operation principle of CS&H

Figure 3.6 (a) shows current sample and hold (CS&H) circuit for BL suppression. $C_{S\&H}$ samples photocurrent by BL and then accumulates additional photocurrent by emitted light. In Figure 3.6 (b), $C_{S\&H}$ senses DC current by setting S/H to high state and gate-source voltage of T_1 is defined. After S/H transistor turns off, gate-source voltage remains preserved by $C_{S\&H}$, so it facilitates BL suppression [10].

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3.3.2 Flipping feedback capacitor to delta accumulation

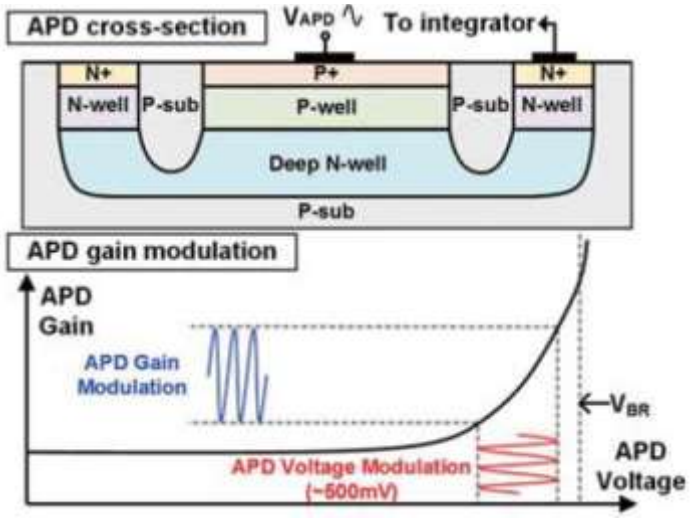

Figure 3.7 APD cross-section and its operation principle

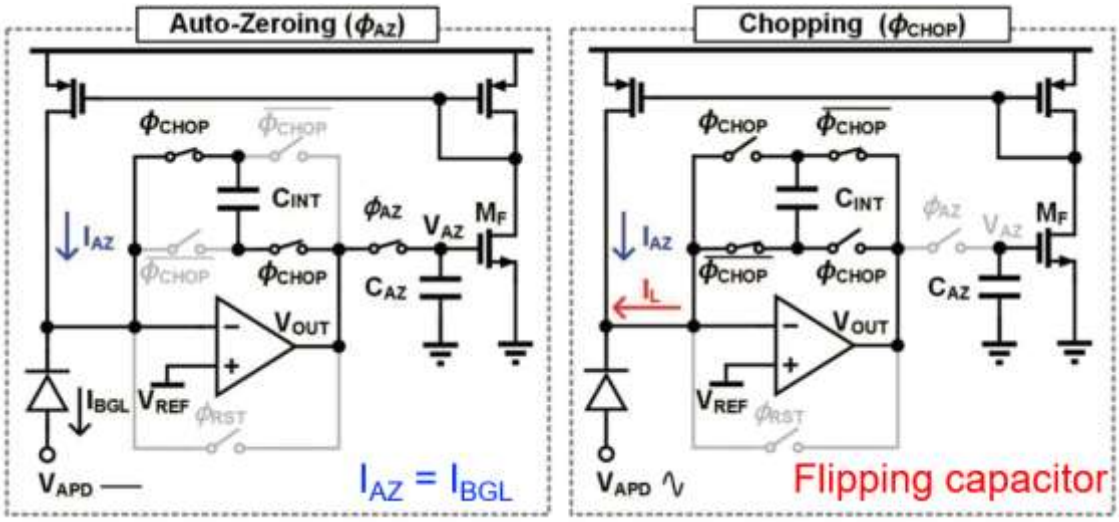

Figure 3.8 Pixel schematic with in-pixel BLS and chopping

In figure 3.7, a low noise APD is implemented with a p-well/DNW junction and it has better sensitivity, but it needs additional p-sub guard-ring to avoid early breakdown, so its pixel pitch is a quite large by photodiode structure. There are coarse and fine scheme for BL suppression. Coarse is flipping integration capacitor and fine is sampling only BL and nulling photocurrent by BL. In figure 3.8, at initial state, photocurrent by only BL is generated and then it is copied by current mirror. This nulling current is present during chopping phase by C_{AZ}. Through these techniques, it can suppress up to 200klx sunlight [11].

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3.4 Discrete hole supply scheme

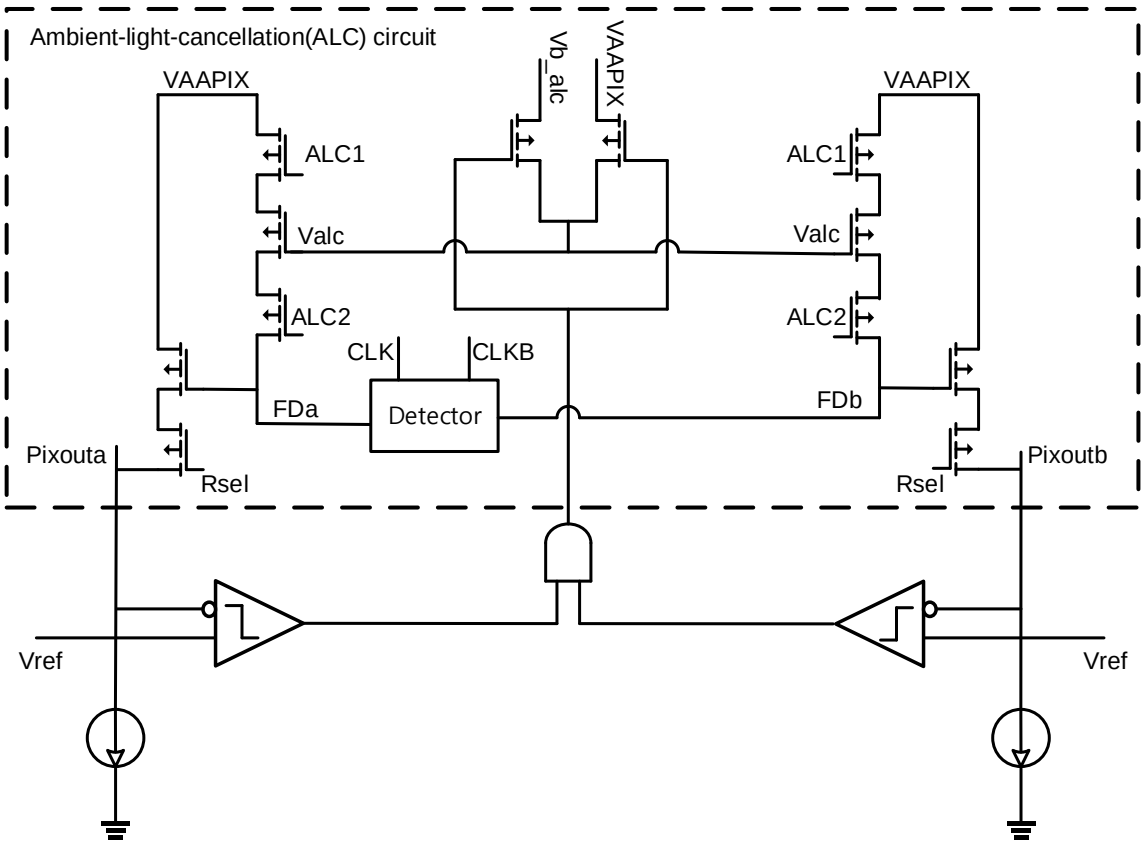

Figure 3.9 Ambient-light-cancellation TOF pixel with three-transistor discrete-time charge sources

In figure 3.9, three-transistor discrete-time charge sources (ALC1, Valc, ALC2) are implemented for ambient light cancellation. When these transistors are activated, ALC circuit injects the same number of holes into each FD. The electrons in FD node recombine with discrete hole packet and it helps saturation of FD node and prevents depth error by ambient light. Each hole source consists of PMOS transistors and middle transistor acts like a MOS capacitor. It stores hole and transfers to FD. This scheme can be implemented on small size pixel, but it has limited subtraction efficiency (up to 40klx) [12].

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Chapter 4.

Proposed i-ToF sensor with in-pixel Adaptable BL Suppression Based on ΔΣ

4.1 Solution of previous work problem

4.1.1 Adaptable ΔΣ by monitoring FD node

In previous work, flipping photodiode scheme has some problems. First is that switching noise is very large. For flipping photodiode, a few switches need and it requires switch operation at every in-phase and out-phase integration. In case of low light signal, this scheme has unnecessary switching noise. Proposed solution of large switching noise is removing unnecessary switch operation by smart adaptable ΔΣ when light signal is not high.

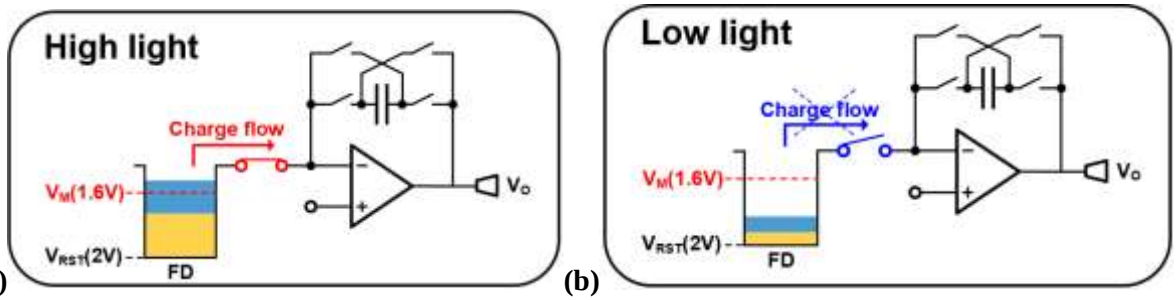

Figure 4.1 (a) Smart adaptable ΔΣ ON
(b) Smart adaptable ΔΣ OFF

At integration phase, generated electron is demodulated to in-phase signal and out-phase signal. After integration time, comparator monitors FD node voltage and determines ΔΣ operation will be ON or OFF. Figure 4.1 (a) shows case of high light and figure 4.1 (b) shows case of low light. In low light case, ΔΣ operation is skipped and electrons for background and light are accumulated continually.

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4.1.2 Automatic TX chopping interlocking adaptable ΔΣ

In previous work of flipping photodiode, second problem is mismatches. There is some factors causing mismatches. One is photodiode mismatches. P+/N-well photodiode and N-well/P-sub photodiode has different sensitivity and it causes different photocurrent. In add phase, additionally, both P+/N-well PD and N-well/P-sub PD make photocurrent, but in subtract phase, only P+/N-well PD makes photocurrent. It may cause depth error. Another is TX strength variation by process variation. If TX strength is different, charges generated on PD transfer to FD capacitors differently about in-phase case and out-phase case. To resolve these problems, automatic TX chopping technique is proposed.

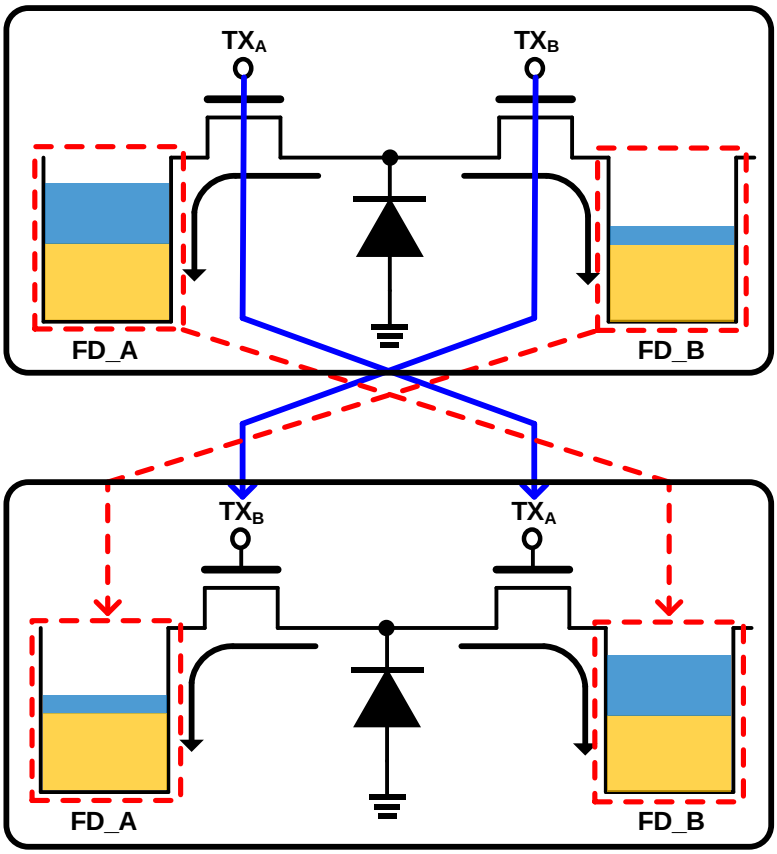

Figure 4.2 TX chopping mechanism by flipping control signal

After ΔΣ operation, T flip flop for TX chopping controls that TX signals are flipped and accumulates in-phase signal on FD B node and out-phase signal on FD A node. Through this technique, TX strength variation and floating diffusion mismatch problem could be compensated.

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4.1.3 Pinned-PD for accelerating charge transfer

Third problem is only possible for low frequency operation due to conventional photodiode structure characteristic. An expression for the standard deviation of the phase measurement of indirect ToF is known as [13]:

$$\sigma_R = \frac{c}{4\pi f_{mod}\sqrt{2}} \cdot \frac{\sqrt{A_{sig} + Background}}{c_{demod} A_{sig}}$$

where A_{sig} is intensity of signal and f_{mod} is modulation frequency and c_{demod} is demodulation contrast. From this equation, we can know σ_R will decrease as modulation frequency goes up. To operate high modulation frequency up to 50MHz, pinned-photodiode with doping gradient is proposed.

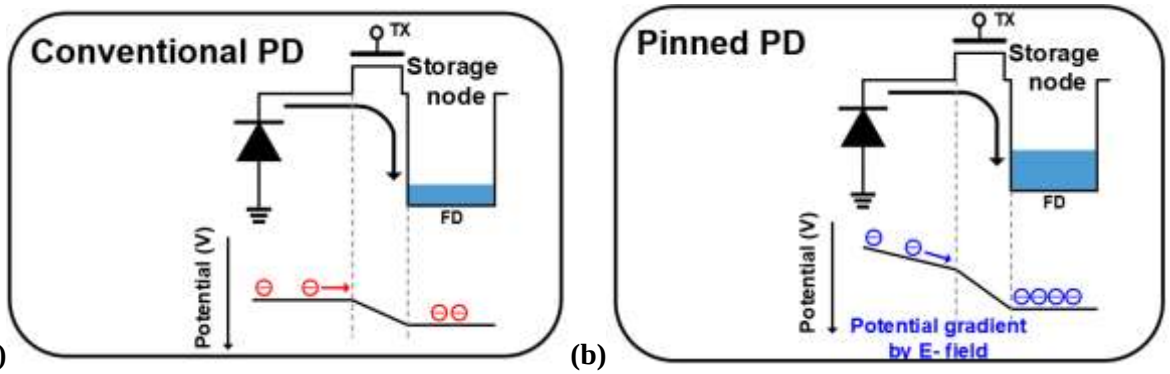

Figure 4.3 (a) Conventional photodiode potential diagram
(b) Pinned-photodiode potential diagram

In figure 4.3 (a), conventional PD has flat electric-field from PD to FD node, so as frequency increases, electrons generated on PD could not fully transfer to FD node for given time. Figure 4.3(b) shows accelerated charge transfer. By gradient doping concentration on photodiode region, sloped electric-field from PD to FD node is generated and it helps for electrons to fully transfer to FD node [14].

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4.1.4 In-pixel integrator for global ΔΣ operation

Fourth problem is BL suppression capability decrease through row-by-row ΔΣ. In ΔΣ BLS by column-level subtraction scheme, integrator is shared in each column. Through sharing integrator, pixel pitch could decrease because there is no integrator in pixel, so it is effective in terms of pixel resolution. However, it can't implement ΔΣ operation globally because there is only 1 integrator in column line. Therefore, ΔΣ time is much longer than global ΔΣ operation and it can't implement many sub-integration.

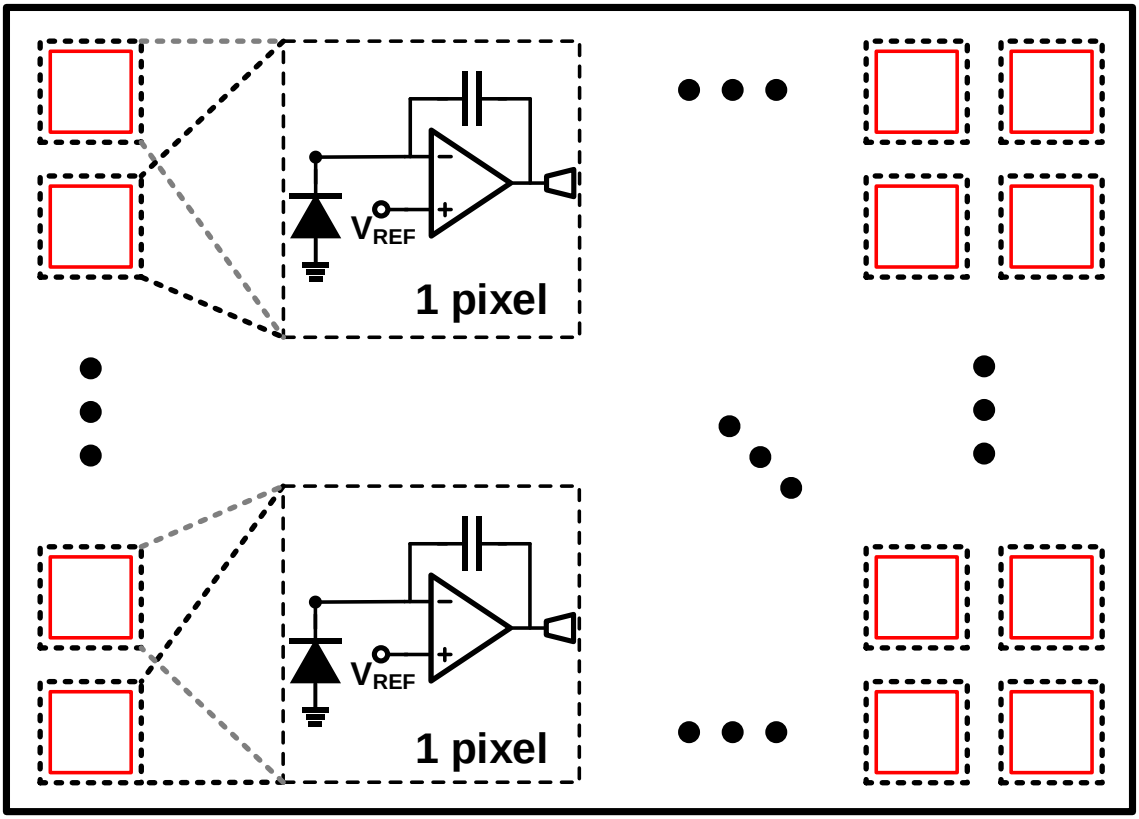

Figure 4.4 Structure with integrator in-pixel level for global ΔΣ

Figure 4.4 shows pixel structure with integrator in pixel for global ΔΣ. In this case, ΔΣ time is very short, so it can implement much times of ΔΣ compared to column-level ΔΣ. In strong background case, global ΔΣ operation will be effective.

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4.2 Proposed Sensor Design

4.2.1 Proposed overall architecture

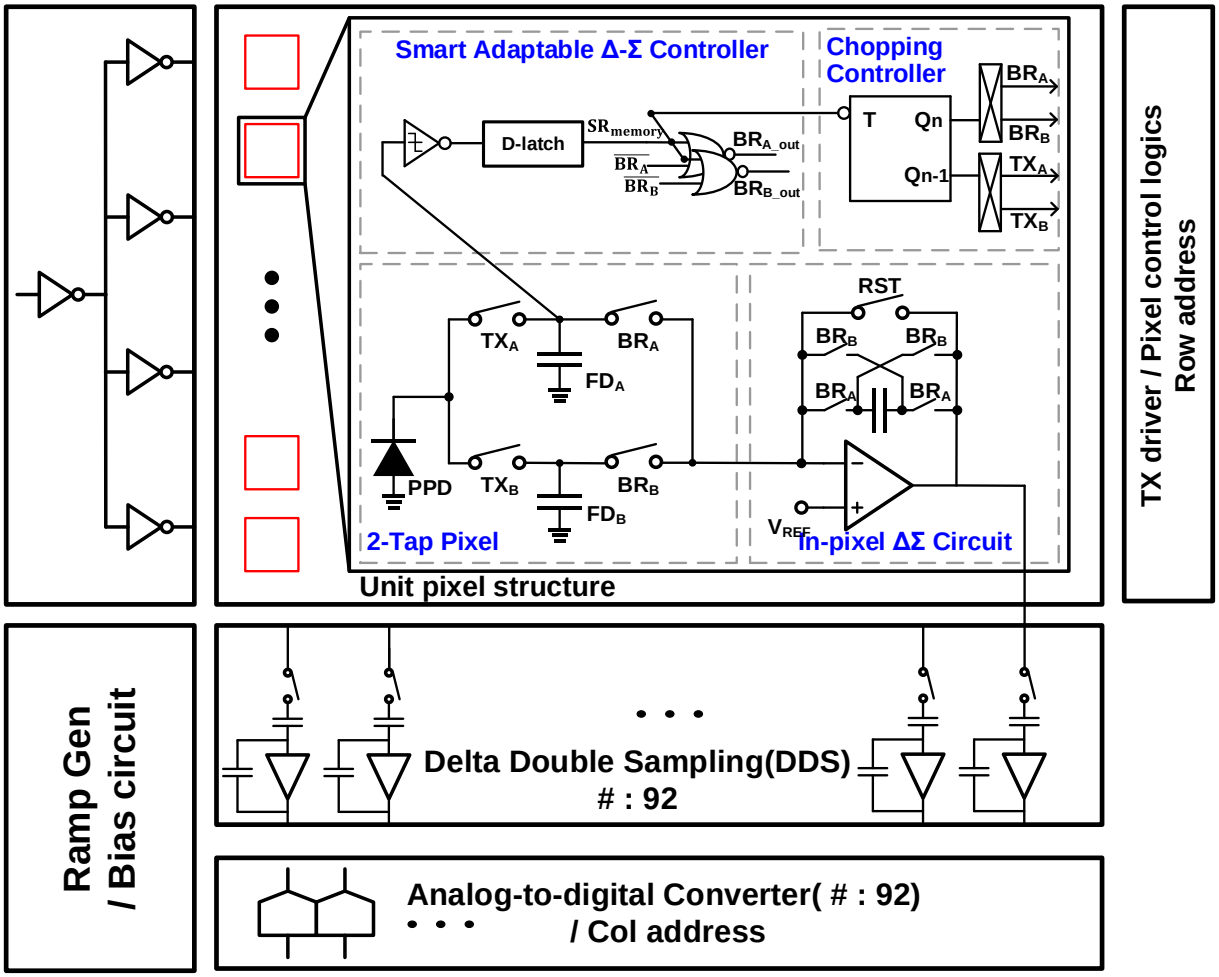

Figure 4.5 Overall architecture of proposed sensor

Figure 4.5 shows full architecture of proposed BLS sensor. It consists of a pixel array, two row drivers, decoders and TX clock trees, and a column-parallel delta double sampler (DDS) with an address decoder. Each pixel includes pinned photodiodes, amplifier, 3 memories for smart reset and TX chopping, 100fF MIM capacitor. Single-slope ADC has 10 bits resolution. Pixel pitch is 28.8um and pixel array is 92 x 72 with optical black (OB) dummy pixel. A pixel on the edge is not surrounded by pixels everywhere, so it may cause mismatch compared to other pixels. This is first reason we add OB pixel on the edge. Second reason is for calibrating signal by dark current in no light signal case. Effective pixel array is 80 x 60 without OB pixel. All pixel has individual amplifier in pixel for switched-capacitor Integrator. In addition, it has active reset scheme for reducing KTC noise and smart reset for reducing

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unnecessary switching noise. For background light cancelling, integration time is divided by a few sub-integrations. By monitoring FD node voltage through inverter-based comparator, it determines whether turning delta-sigma operation on or off between FD A node (In-phase) and FD B node (Out-phase). On sub-integration time, FD node reset is automatically implemented by transferring FD node charge to integration capacitor.

4.2.2 In-Pixel Background Light Suppression (BLS) structure

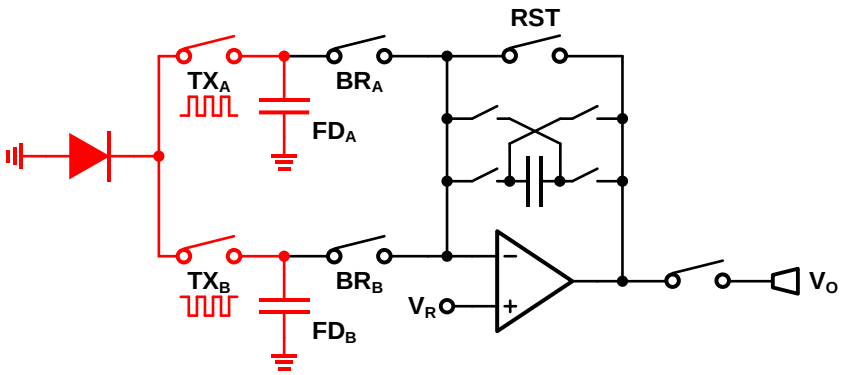
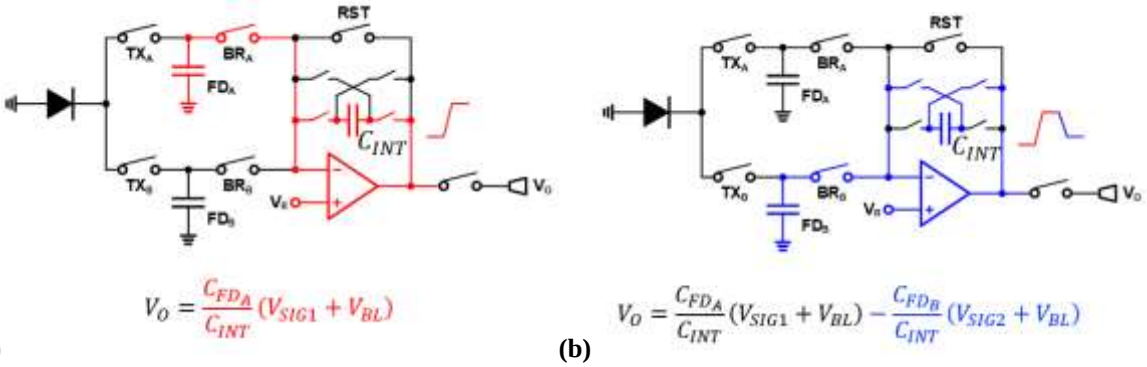


Figure 4.6 Operation on integration phase

Figure 4.6 shows TX operation on integration phase. Through TX operation, electrons on PD is transferred to two nodes corresponding to TX signal. Usually, signal for 0 degree and 90 degree is collected on FD A node and signal for 180 degree and 270 degree is collected on FD B node.



(a) **(b)**

Figure 4.7 (a) In-phase operation on background light suppression (BL) phase
(b) Out-phase operation on background light suppression (BL) phase

In BLS phase, by turning on BR A switch, charges on FD A node transfers to integration capacitor and capacitor ratio × voltage corresponding to signal 1 and background light is added to reference voltage. At next, by turning on BR B switch, integration capacitor is flipped and charges on FD B node transfers to integration capacitor. In this case, however, voltage for signal 2 and background light is subtracted because capacitor is flipped. Through delta-sigma of FD node, we can get difference signal between in-phase signal and out-phase signal except background light

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4.2.3 Smart reset technique for low charge-injection

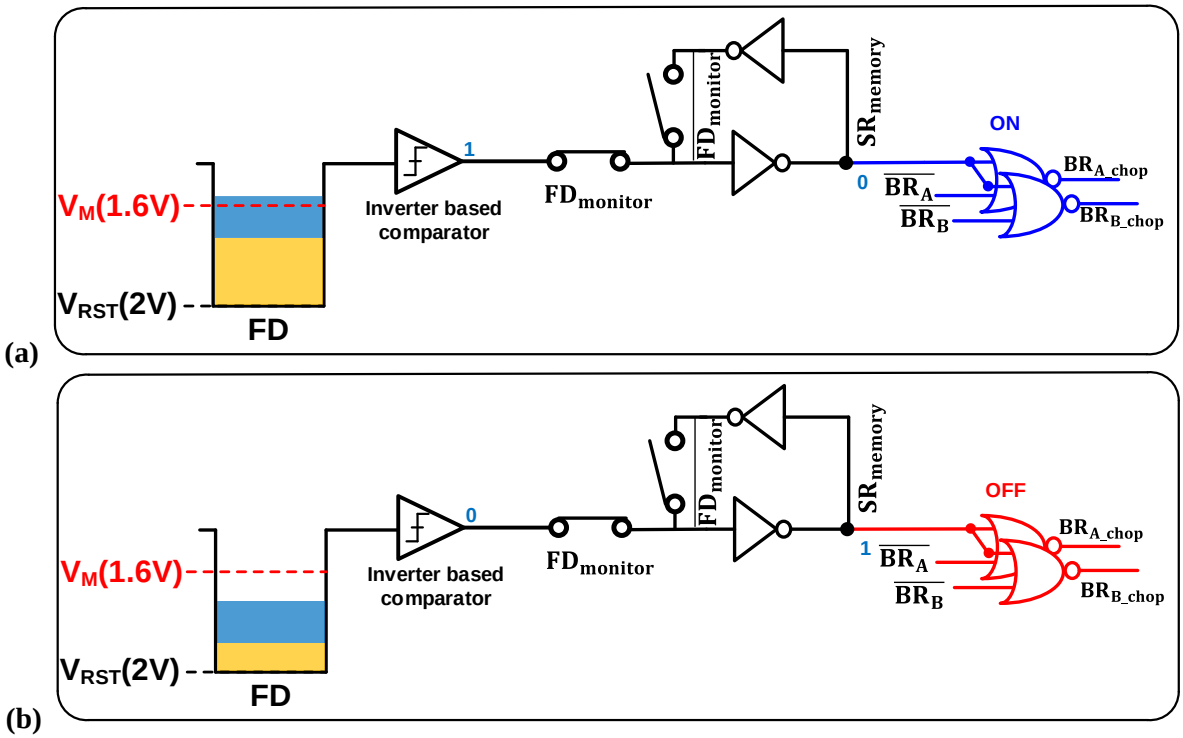

Figure 4.8 (a) ΔΣ controller ON state when light signal is high
(b) ΔΣ controller OFF state when light signal is low

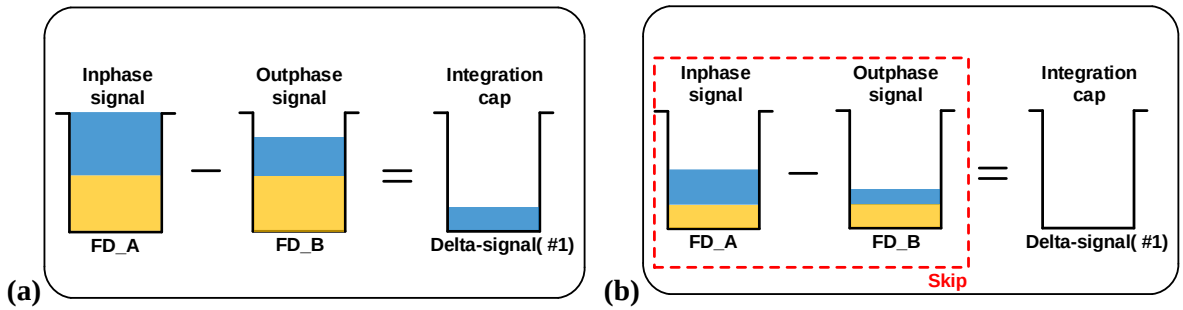

Figure 4.9 (a) ΔΣ operation is ON
(b) ΔΣ operation is OFF

Smart adaptable ΔΣ controller scheme is proposed for reducing unnecessary switching noise when background light is not dominant. In strong background light (BL) case, signal will be distorted by BGL. In figure 4.8, inverter-based comparator monitors light condition and inverter-latch memory stores this data for delta-sigma phase. If FD voltage is under 1.6V (High light), inverter output is high and it determines delta-sigma and FD node reset. If FD voltage is over 1.6V (Low light), inverter output is low and it skips delta-sigma operation and collects light signal continuously. At next phase, comparator monitors FD node again and if FD voltage is under 1.6V, it determines delta-sigma operation. Figure 4.9 (a) shows that ΔΣ operation is on when light signal is high and (b) shows that ΔΣ operation is off when light signal is low.

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4.2.4 TX gate signal chopping in pixel-level for reducing mismatch

There are some mismatch factors in pixel. First is TX strength variation between FD A node and FD B node. Second is full-well-capacity (FWC) variation between two FD nodes. Mismatch of FWC cause different gain and it may cause depth error. To compensate these mismatches by process variation, TX gate signal chopping in pixel-level is proposed.

Figure 4.10 is memory based on T flip-flop for chopping. BR chopping time is next to TX chopping time, so this is why 2 memories for chopping are needed. Figure 4.11 is operation of chopping logic in strong background light case.

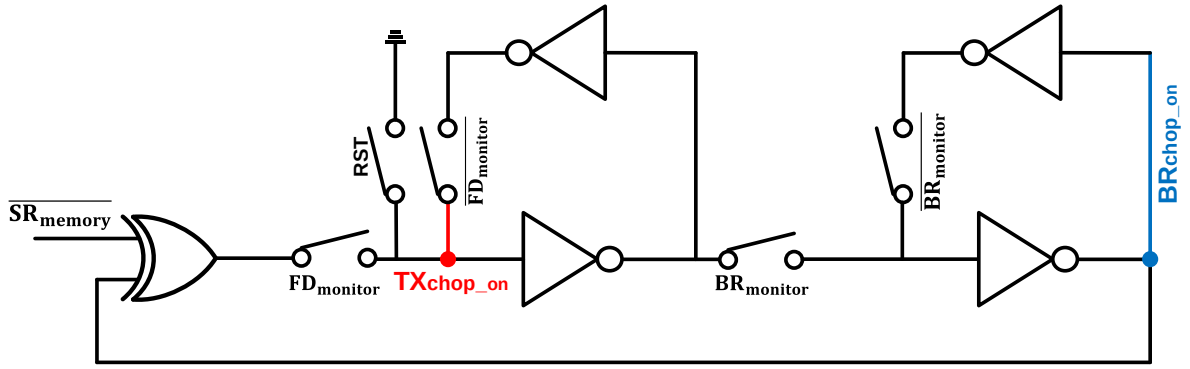

Figure 4.10 Memory based on T flip-flop for TX and BR chopping

	Sub int #1	ΔΣ#1	Sub int #2	ΔΣ#2	Sub int #3	ΔΣ#3	Sub int #4	ΔΣ#4
FD value	>1.6V	>1.6V	<1.6V	<1.6V	>1.6V	>1.6V	<1.6V	<1.6V
Smart reset		OFF		ON		OFF		ON
TX chopping	OFF	OFF	OFF	ON	ON	ON	ON	OFF
TX signal	TX		TX		$\overline{TX}$		$\overline{TX}$	
BR chopping	OFF	OFF	OFF	OFF	OFF	ON	ON	ON

Figure 4.11 Case of strong background light

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4.2.5 Overall operation

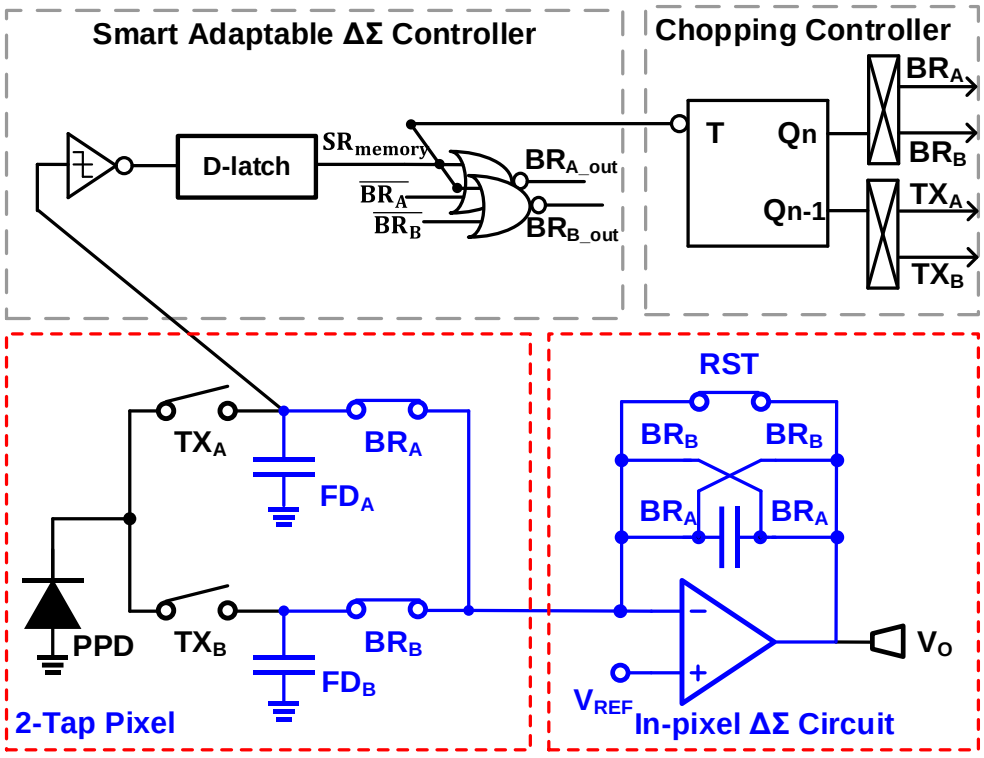

Figure 4.12 Unit pixel schematic with smart adaptable ΔΣ and chopping controller

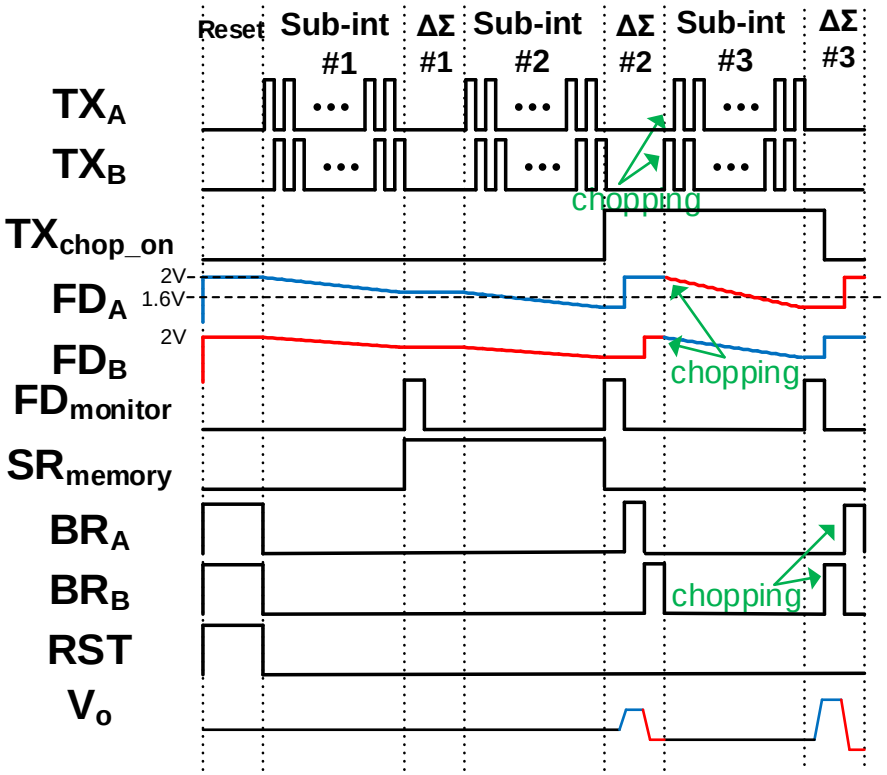

Figure 4.13 Overall timing diagram of proposed sensor

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Figure 4.12 shows overall structure of unit pixel. It consists of 4 blocks; 2-tap pixel based on pinned-photodiode, integrator with 5 switches and 1 MIM capacitor for ΔΣ operation, smart adaptable ΔΣ controller for determining ΔΣ ON/OFF and chopping controller for TX and BR switching operation chopping. Operation is divided by three phase briefly; reset phase, sub-integration phase and ΔΣ phase. First phase is reset phase. Storage node FD is reset to V_{REF} by negative feedback of amplifier. At sub-integration phase, electron generated on photodiode is demodulated by TX operation. FD A stores in-phase signal and FD B stores out-phase signal. After sub-integration, smart adaptable ΔΣ controller determines ΔΣ operation. Inverter based comparator monitors FD node voltage. If it is over 1.6V, ΔΣ operation turns OFF. On the other hand, if it is under 1.6V, ΔΣ operation turns ON. Because FD node voltage means signal intensity added background light. If ΔΣ turns ON, chopping controller controls TX chopping signal ON. After ΔΣ operation, in-phase signal is stored on FD B and out-phase signal is stored on FD A. Because TX signal is flipped by TX chopping controller. In this case, ΔΣ operation also should be flipped in sync with TX signal. After 2nd sub-integration phase, ΔΣ operation is flipped by BR chopping memory. Therefore, charges of in-phase signal on FD B transfers to integration capacitor firstly and charges of FD A transfers to flipped integration capacitor. At next sub-integration phase, TX chopping signal is inverted again, so in-phase signal is stored on FD A and out-phase signal is stored on FD B node. Through these techniques, it can reduce unnecessary switching noise or charge injection when light signal is not high and it can compensate storage node mismatch and TX strength mismatch problem by process variation.

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Chapter 5. Measurement result

5.1 Measurement system setup

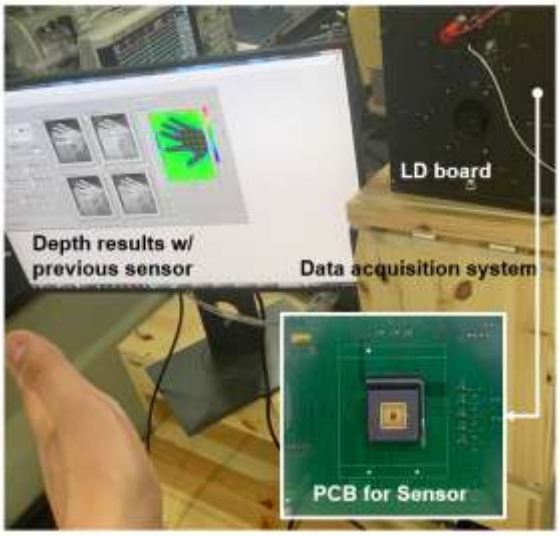

Figure 5.1 Measurement system setup of sensor board

In figure 5.1, it shows system of sensor measurement. Control signal is generated by FPGA and inserted to chip. Row decoder and column decoder signal controlled by FPGA makes address and CDS output is read out row by row.

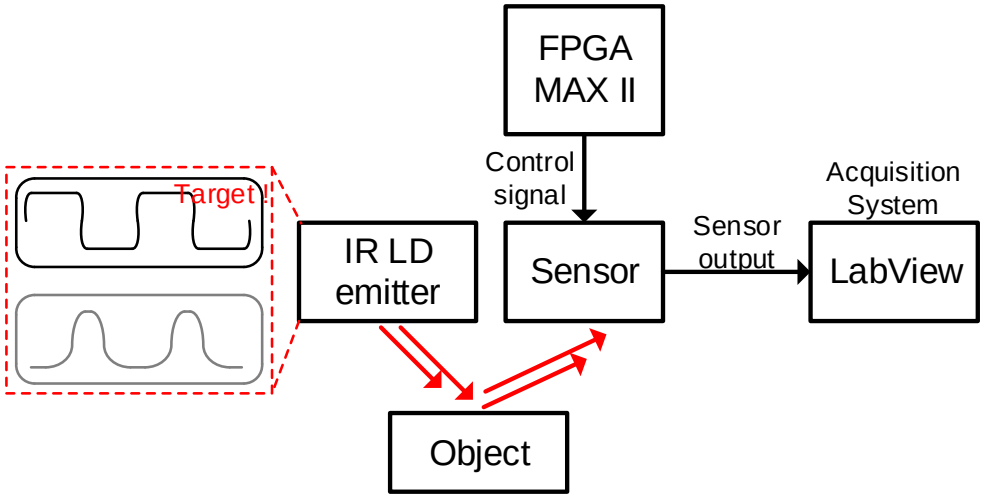

Figure 5.2 Block diagram of overall system

In figure 5.2, LED emitter pulse has long rising and falling time and it means that our depth calculation is not correspond in this case. Additionally, emitter's large distortion in waveform also causes depth error. Therefore, we need IR LD emitter which has short rising and falling time and operates on high modulation frequency.

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5.2 Light source and optical emitter design

5.2.1 Light source - LED

2 types of light source are used in ToF optical emitter. First, LED is abbreviation of light emitting diode. LED is photonic-semiconductor that transfers electric energy to light energy. In figure 5.3, LED basically consists of p-type semiconductor and n-type semiconductor (P-N junction). When forward voltage is biased on diode, electron on n-type semiconductor moves to p-type semiconductor and then it combines with holes. In this case, light is emitted by forward current.

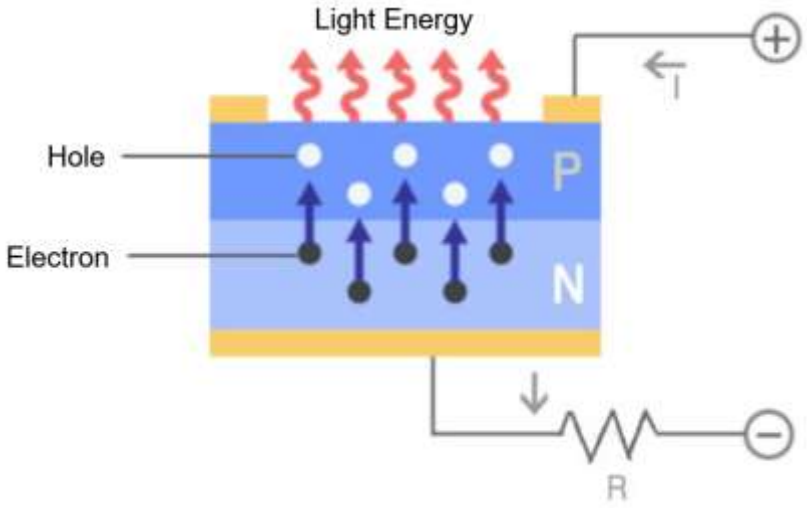

Figure 5.3 Structure of LED

5.2.2 Light source – LD

LD is abbreviation of light amplification by stimulated emission of radiation. In figure 5.4, literally, to get a stimulated emission, it needs 2 mirrors for resonance cavity and it plays the role of light amplification. The most difference between LD and LED is coherence. LD can emit completely same phase and wavelength light pulse, so coherence is very high. Therefore, LD's wavelength spectrum is uniform, while LED is broad.

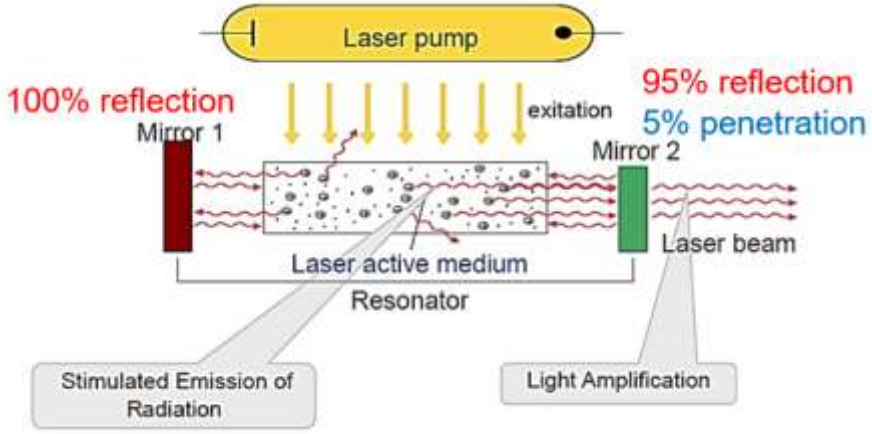

Figure 5.4 Structure of LD

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5.2.3 Light source device comparison

Figure 5.5 is comparison between LED device (OSRAM SFH4259S) and LD device (Lumentum 22045498)

	LED(SFH4259S_OSRAM)	Laser(22045498_Lumentum)
Output power	Linearly proportional to drive current	Proportional to current above threshold
Power intensity	55mW	2.4W ☺
Divergence	50°	Approximately 20° ☹
Rising time	12ns	1ns ☺
Fall time	12ns	2ns ☺
Wavelength	860nm	855nm

Figure 5.5 Comparison of LED and LD

LD power intensity is approximately 44 times stronger than LED's. Because LD's power is exponentially proportional to current above threshold current. Figure 5.5 is comparison between LED device (OSRAM SFH4259S) and LD device (Lumentum 22045498)

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5.2.4 Switching topology

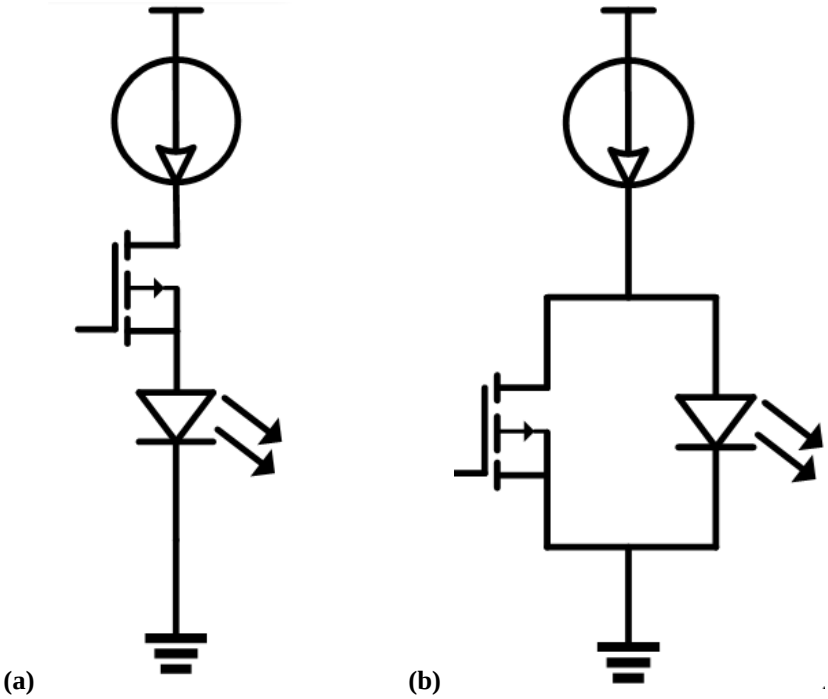

Figure 5.6 (a) Series switching circuit
(b) Shunt switching circuit

Figure 5.6 shows two types of switching circuit. In series switching circuit, it has voltage source and emitter and switch in series. By controlling gate voltage, it turns on and off the switch at modulation frequencies. In this case, it has disadvantage of having switch drain node impedance going to infinite when switch turns off. The only advantage to use this topology is that inductor is not necessary. In shunt switching topology, it has current source and emitter and switch in parallel. This is same to Norton's equivalent of series switching circuit. In this topology, the advantage is that there is no infinite impedance node. Therefore, in high frequency operation, this switching topology is recommended. However, it is not suitable for very low power illumination circuits. Because most discrete switching power MOSFETs in market have relatively high output capacitance. Small current from current source could not drive the MOSFET output capacitance at high frequencies. Nevertheless, it has many advantages compared to series switching topology. Its output power is relatively stable against frequency, temperature and electrical to optical conversion efficiency is higher.

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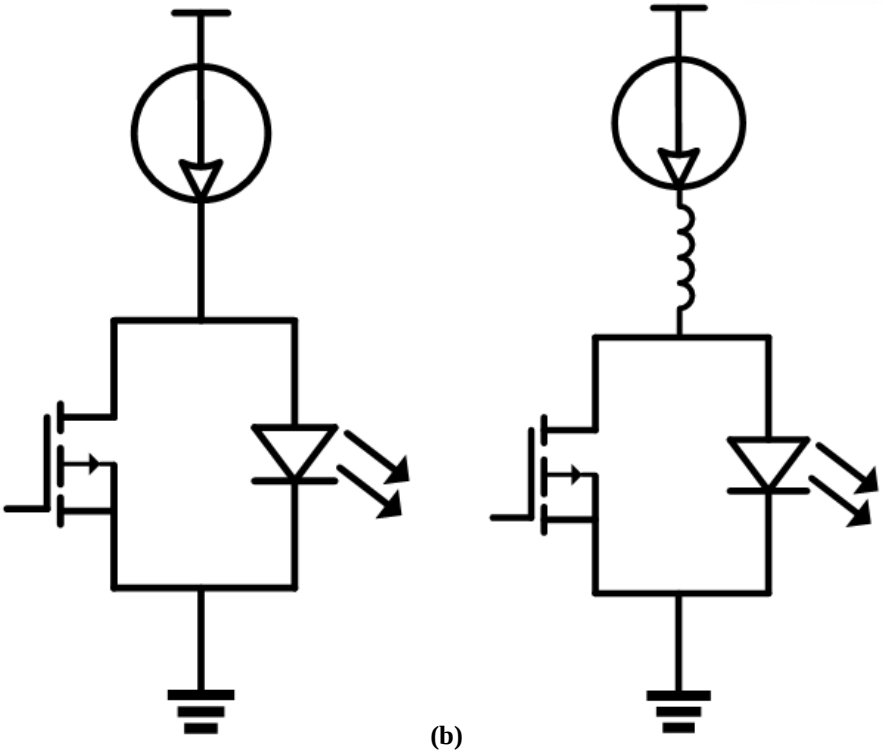

(a) **(b)**

Figure 5.7 (a) Shunt switching circuit without high frequency inductor
(b) Shunt switching circuit with high frequency inductor

However, practical current sources cannot provide high impedance as frequencies goes up. It is very hard to get high impedance current sources at voltage rise edge rates of optical emitter circuits. In figure 5.7, Adding inductor in series with current sources compensates current source's impedance. Impedance of inductor increases with frequency (ωL). On high frequency, inductor impedance increases the overall output impedance of current source.

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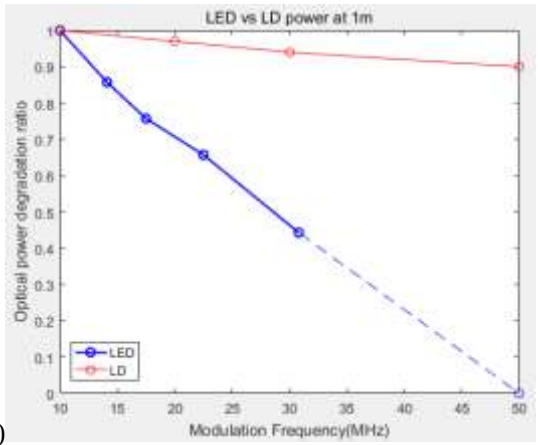
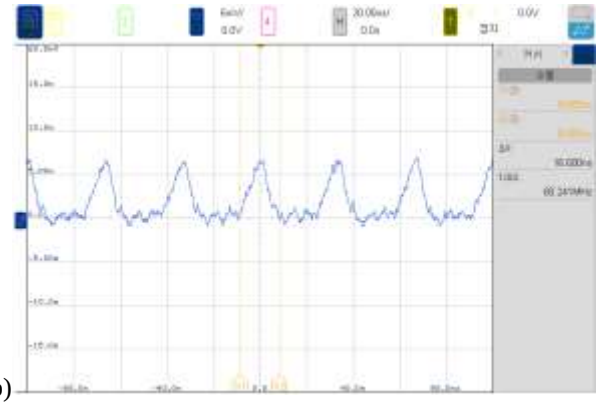
5.2.5 LD board measurement



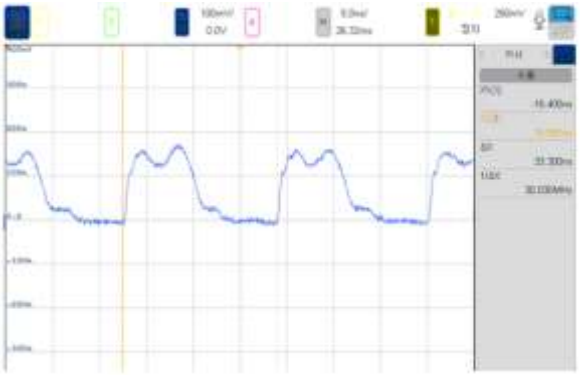
(a)



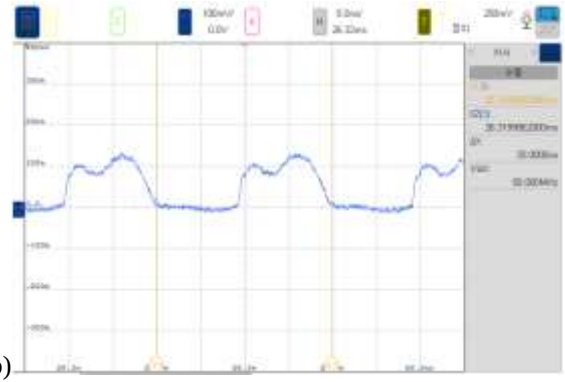
(b)

Figure 5.8 (a) Optical power degradation ratio graph as frequency changes
(b) LED pulse waveform through photodetector on 30MHz

Figure 5.8 (a) shows optical power degradation ratio between LED and LD. As frequency goes up, pulse width decreases. In figure 5.8 (b), it seems like triangle wave not pulse wave. Because it's rising and falling time is quite long. This is why its optical power decreases as frequency increases.



(a)



(b)

Figure 5.9 (a) Pulse waveform through photodetector on 30MHz
(b) Pulse waveform through photodetector on 50MHz

However, Figure 5.9 shows LD waveform through photodetector. It's falling and rising time is much shorter than LED, so its waveform is much closer to pulse waveform. Additionally, optical power degradation is under 10% from 10MHz to 50MHz.

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5.3 Chip measurement

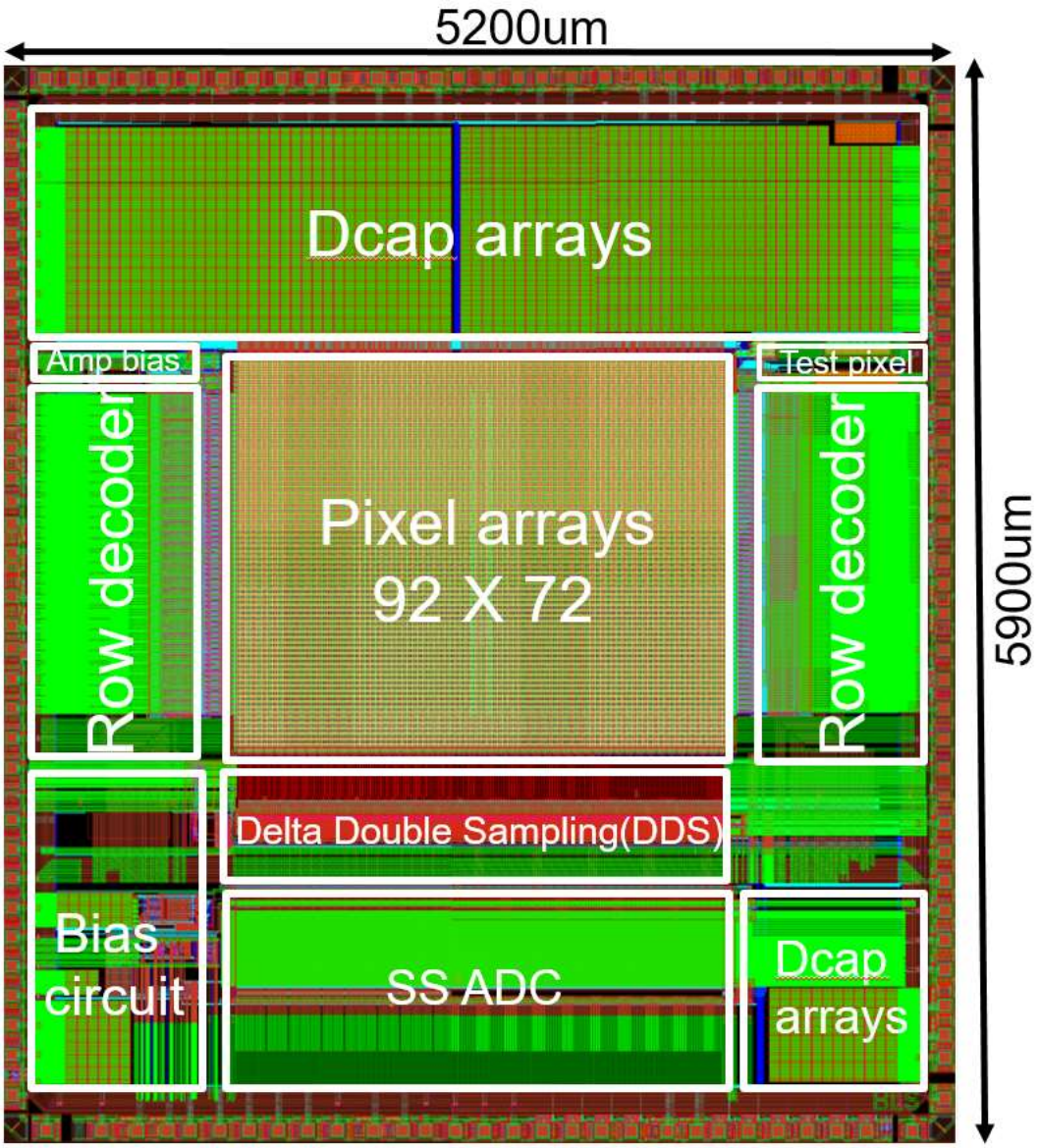

Figure 5.10 5200um x 5900um in-pixel background light suppression i-ToF system layout

Figure 5.10 shows overall layout of smart adaptable ΔΣ with BL suppression. Pixel array is 92 x 72 with optical dummy and pixel pitch is 28.8um. Pixel array and unit pixel layout is shown below.

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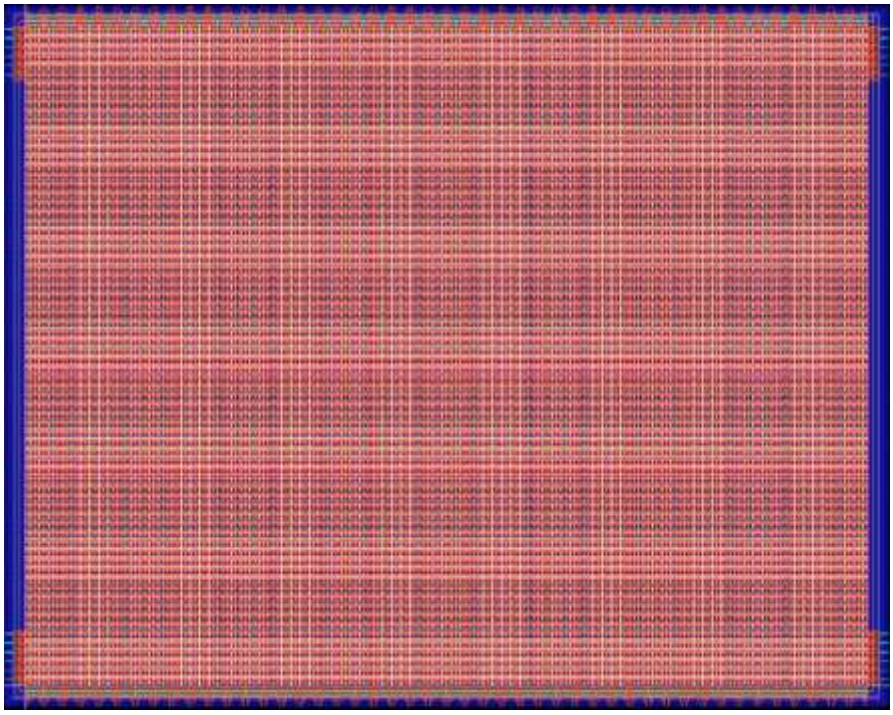

Figure 5.11 92x72 pixel array layout

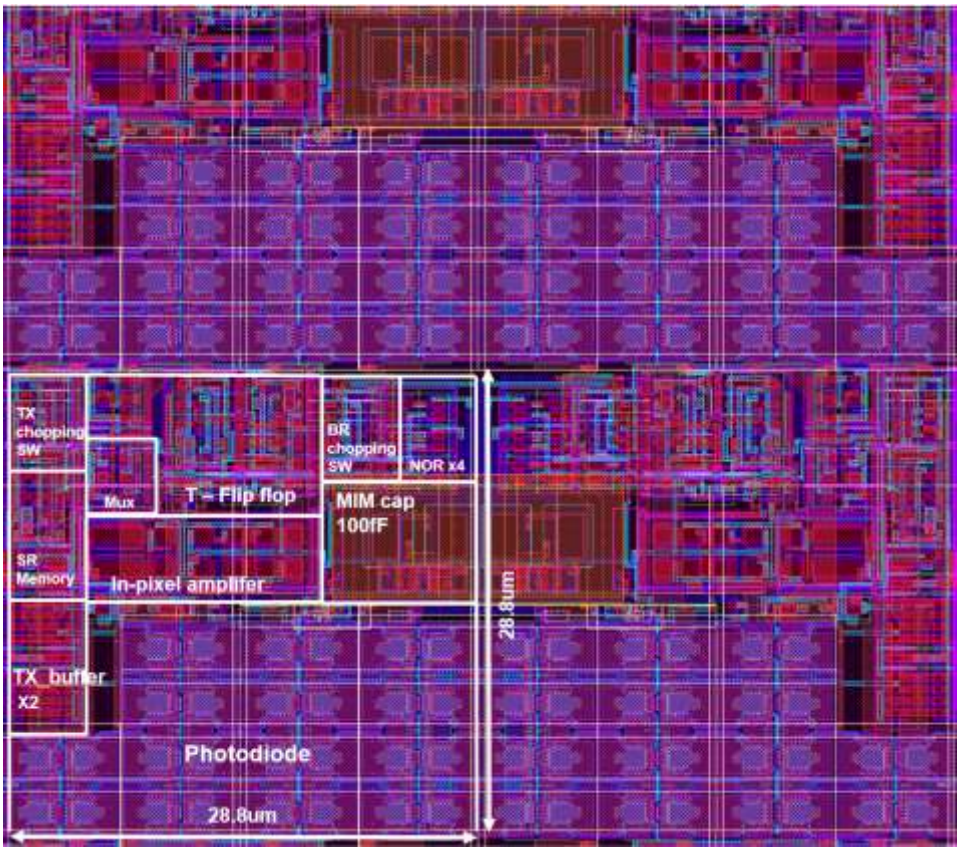

Figure 5.12 2x2 pixels layout

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A. Smart adaptable ΔΣ simulation result

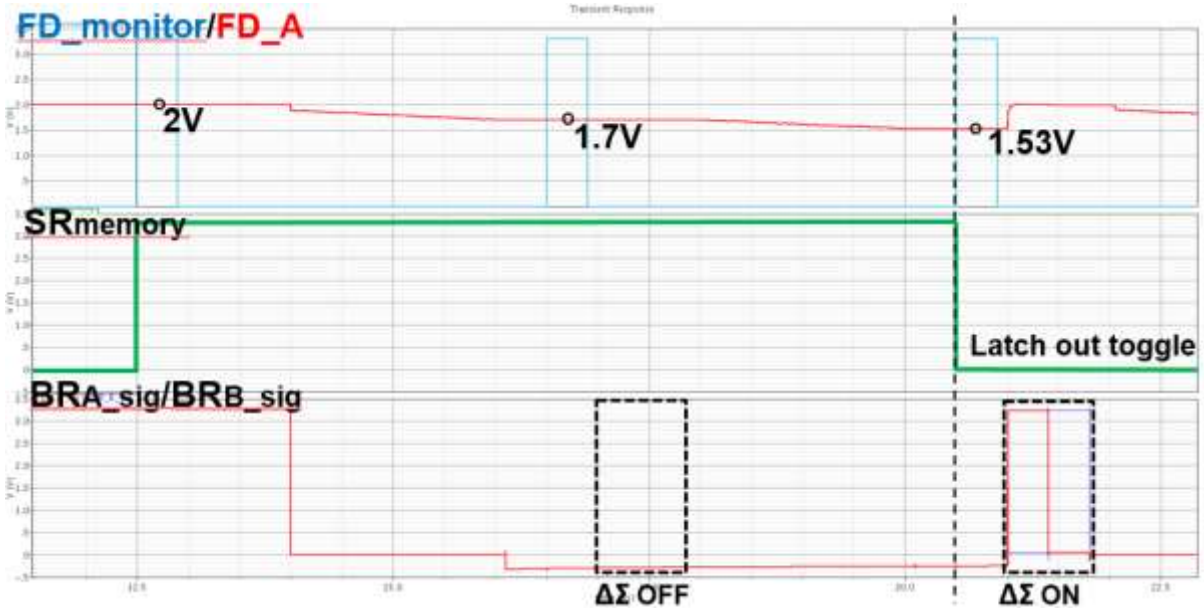

Figure 5.13 Simulation result of smart adaptable ΔΣ ON/OFF operation

At first, storage node (FD) is reset to 2V by negative feedback. For integration time, FD voltage decreases as generated electrons are transferred by modulated TX operation. At ΔΣ phase, inverter-based comparator monitors FD node (1.7V). It is over 1.6V, so ΔΣ operation is OFF. After 2nd integration, comparator monitors FD node (1.53V) again. SR_{memory} value is toggled to zero because it is under inverter switching point. In this phase, ΔΣ operation is ON.

B. Automatic TX chopping simulation result

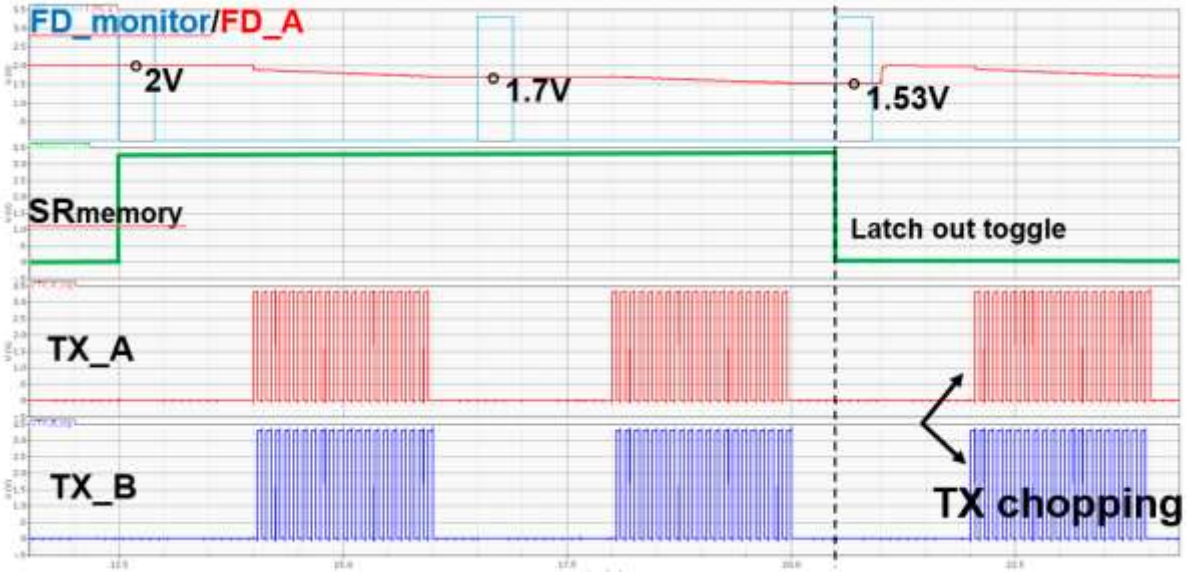

Figure 5.14 Simulation result of automatic TX chopping operation

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TX chopping is interlocked with smart adaptable ΔΣ operation. If FD value is under inverter switching point, ΔΣ operation turns ON and TX signal for next integration is flipped. Figure 5.14 shows TX A signal and TX B signal are flipped as latch out is toggled.

C. ΔΣ operation simulation result for 3 cases

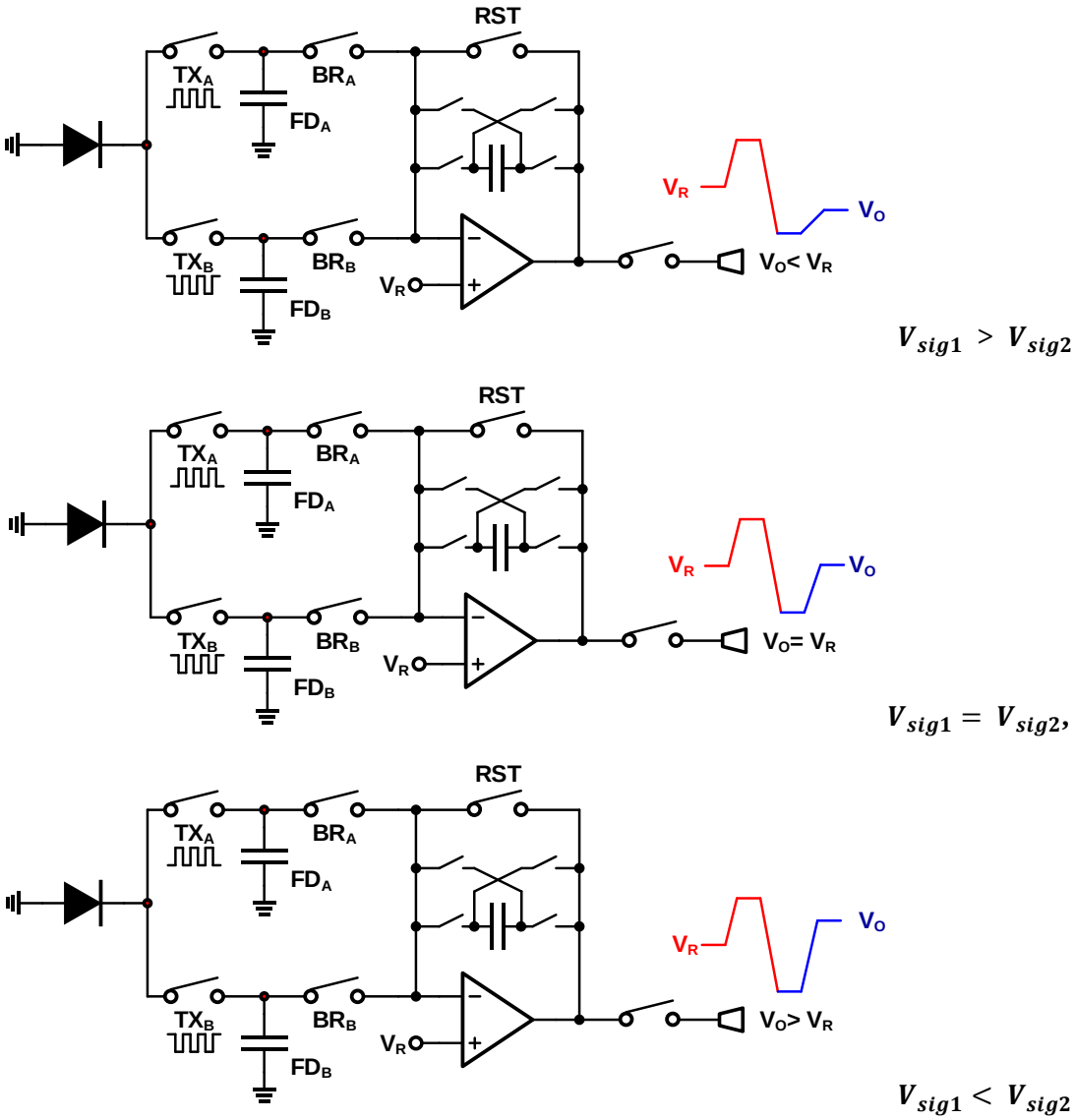

Figure 5.15 Pixel output change for 3 cases of different signal intensity

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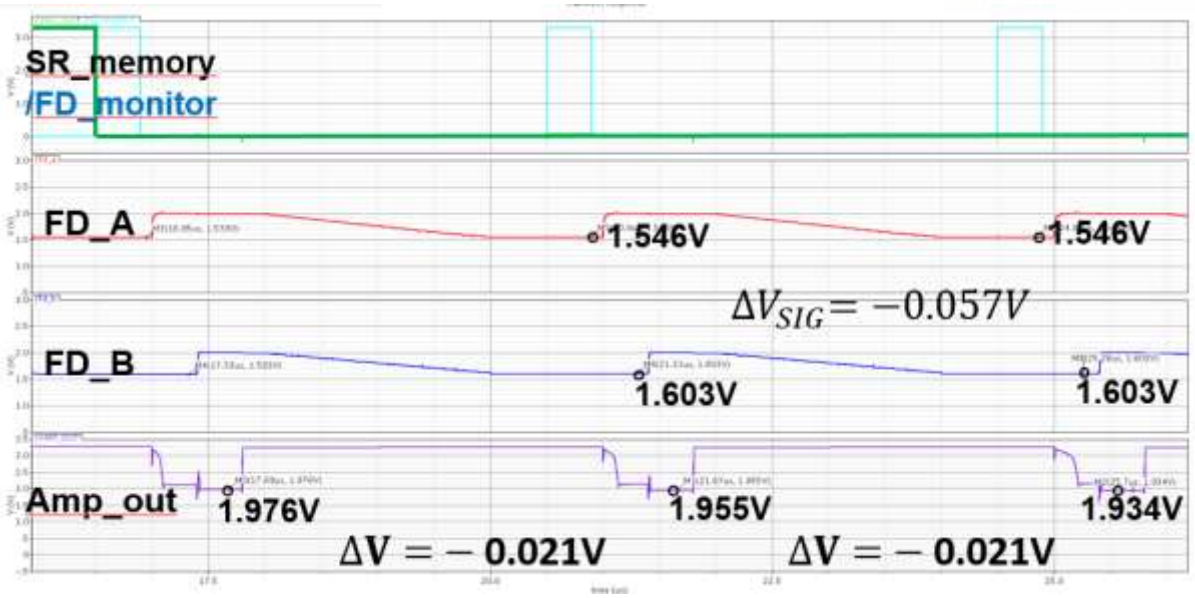

Figure 5.16 Pixel operation simulation result for $V_{sig1} > V_{sig2}$

Figure 5.16 shows simulation result of 1 case that in-phase signal intensity is larger than out-phase signal intensity. Difference between in-phase signal and out-phase signal is approximately -0.057V and closed-loop gain is approximately 0.4. At first, storage node is reset to V_{ref}(2V). After ΔΣ operation, pixel output voltage decreases as much as 0.021V ($\Delta V_{sig} \times$ gain).

Figure 5.17 Pixel operation simulation result for $V_{sig1} = V_{sig2}$

Figure 5.17 shows that in-phase signal intensity is same with out-phase signal intensity. Difference between in-phase signal and out-phase signal is approximately 0V and closed-loop gain is approximately 0.4. At first, storage node is reset to V_{ref}(2V). After ΔΣ operation, pixel output voltage is continuously 1.998V because voltage increment by in-phase signal is same with decrement by out-phase signal.

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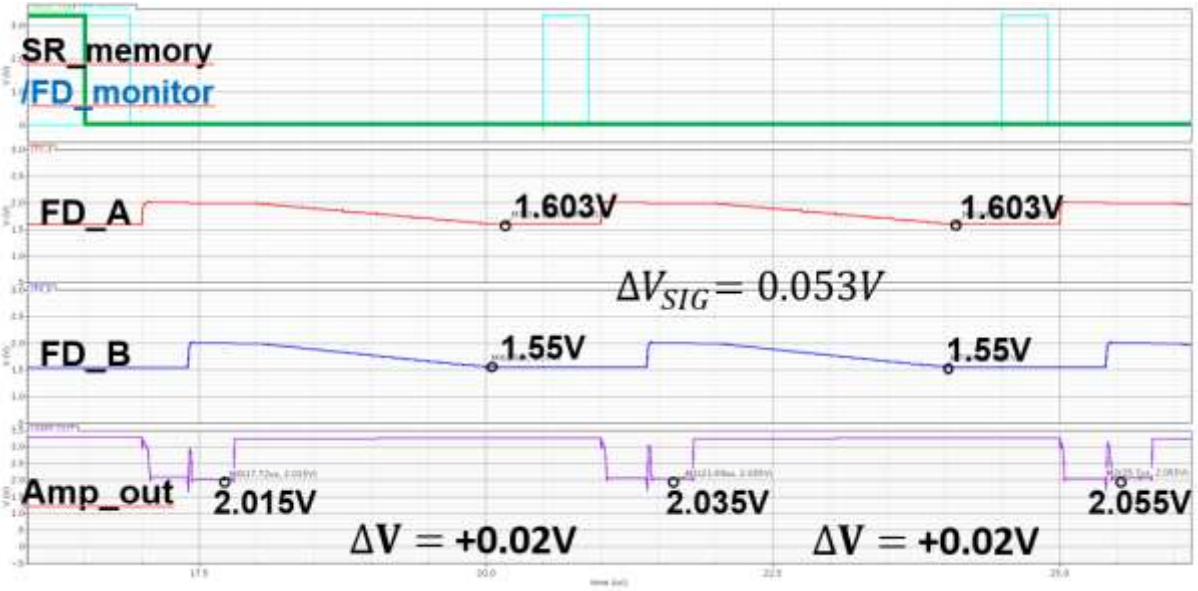

Figure 5.18 Pixel operation simulation result for $\boldsymbol{V_{sig1} < V_{sig2}}$

Figure 5.18 shows that in-phase signal intensity is smaller than out-phase signal intensity. Difference between in-phase signal and out-phase signal is approximately 0.053V and closed-loop gain is approximately 0.4. At first, storage node is reset to V_{ref}(2V). After ΔΣ operation, pixel output voltage increases as much as 0.02V ($\Delta V_{sig} \times$ gain).

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5.3 Conclusion

In this research, 92× 72 i-ToF with smart adaptable background light suppression based on ΔΣ techniques are proposed. Overall architecture consist of a pixel array, two row drivers and decoders for row addressing, TX clock trees, and a column-parallel delta double sampler (DDS) with an column address decoder and 10-bits single-slope ADC. Full chip size is 5900um × 5200um. Briefly, 4 techniques are proposed to develop previous work problem. At first, for reducing unnecessary switching noise when light is low, comparator monitoring storage node determines ΔΣ operation at every sub-integration. At second, for compensation of mismatch problem by process variation, automatic chopping in pixel-level is proposed. At third, for high depth precision, trident PPD with accelerated electric field by doping gradient was implemented. Lastly, for high frame-rate and high background suppression capability, all pixel include individual integrator in pixel and implement ΔΣ operation at the same time.

To compensate power consumption, power-gating controls amplifier bias. Turning off the in-pixel amplifier array on integration time is helpful for power saving because integration time is dominant than readout time and reset time.

Finally, this chip is fabricated with a 0.11um DBH CIS process.

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