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Master's Thesis

A 30 x 32 SPAD-Based Scanless LiDAR Sensor with In-Pixel Histogram Array

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2018

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submitted to the Graduate School of UNIST
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requirements for the degree of
Master of Science

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06. 14. 2018

Approved by

Advisor

Seong-Jin Kim

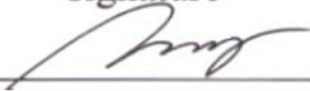
A 30 x 32 SPAD-Based Scanless LiDAR Sensor with In-Pixel Histogram Array

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Abstract

Recently, low cost image sensors have been rapidly developed and applied to various applications. Particularly, the interest in self-driving technology that can drive without a driver beyond the common sense that such applications just help the driver to drive gets attention. Many sensors are required to accurately detect the surrounding situation, and in particular, a LiDAR sensor capable of quickly and accurately measuring mid-range detection is essential to prevent immediate accidents. However, the current LiDAR sensors are expensive due to technical problems with process and rotation issue. It is urgent to introduce a low-cost 3D LiDAR sensor to solve this problem. A single photon avalanche diode (SPAD) is a sensitive device that can generate a signal in response to a single photon and measure a long distance. However, since the SNR of the SPAD is low, histogram which solves the problem through numerous measurements is required. Unfortunately, pixel array cannot be designed due to a memory of histogram, and then SPAD-based LiDAR sensors are currently used as a line sensor. Line sensors using scanning method result in low frame rate, high structural cost for rotation, and low durability issues.

This thesis is based on a new concept using a binary search, a successive approximation registrar (SAR) histogram technique, which eliminates the histogram memory and then designs a low-cost solid-state SPAD-based LiDAR sensor with small size in-pixel histogram. And in order to solve the problem of increasing measurement by eliminating memory, the problem was solved by exponential counting by measuring spatiotemporal correlation using multi-SPADs.

A 30 x 32 in-pixel histogram array and associated circuitry have been designed in a 0.11 μm DBH CMOS process. The sensor has dynamic range of 96m and 0.75m precision for coarse resolution sensor with conventional p-well guard ring (GR) SPAD and advanced virtual guard-ring for high spec dark count rate (DCR) photon detection probability (PDP), 7%, at infrared (IR) -wave. The in-pixel histogram occupies 165 μm x 115 μm area by eliminating memory for histogram.

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TABLE 1. Comparison of performance with State-of-Art Papers

List of Abbreviations

ADAS	Advanced Driver Assistance Systems
APD	Avalanche Photo Diode
BGL	Background Light
DCR	Dark Count Rate
DLL	Delay-Locked Loop
EUDC	Exponential UP-DOWN Counter
GR	Guard-Ring
LD	Laser Diode
LED	Light Emitting Diode
LiDAR	Light Detection and Ranging
SPAD	Single Photon Avalanche Diode
PDP	Photon Detection Probability
SAR	Successive Approximation Register
TCSPC	Time-Correlated Single-Photon Counting
TDC	Time-to-Digital Converter
TH	Threshold
ToF	Time of Flight
PLL	Phase-Locked Loop

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I . Introduction

With the development of Hyper-connected society, the image sensor market is getting bigger. In recent years, low cost 3D image sensors have attracted considerable attention and are being developed for many applications. Typically, self-driving systems that do not require driver manipulation using 3D mapping are actively researched. Advanced driver assistance systems (ADASs) have been studied that include forward collision warnings, emergency braking, traffic sign recognition, cross traffic alerting and parking assistance functions to help users with safety and convenience before self-driving. To realize this function, ADAS systems have used mm-wave radar sensors with passive stereo-vision cameras. However, in order for the driver to reliably drive the self-driving system, the sensor is required to quickly and accurately determine the urgency of a long distance in fig 1. For this purpose, light detection and ranging (LiDAR) sensors which is one type of time-of flight(ToF) are rapidly being studied. The LiDAR sensor measures time difference between the light emitted time from a light source, such as light-emitting diodes (LEDs) or a laser diode(LD) to the detected time of the sensor. However, since the light travels a long distance, there is a serious attenuation and there is very little light entering the sensor. There is a problem that when the background light which is one of noise is strong, the reflected signal is not easy to distinguish from noise. Furthermore, the LiDAR sensor uses invisible infrared (IR)-wave, which is generally used for avoiding to confuse the people, and is less reactive. Therefore, it is difficult to use the silicon process due to low reactivity on IR light.

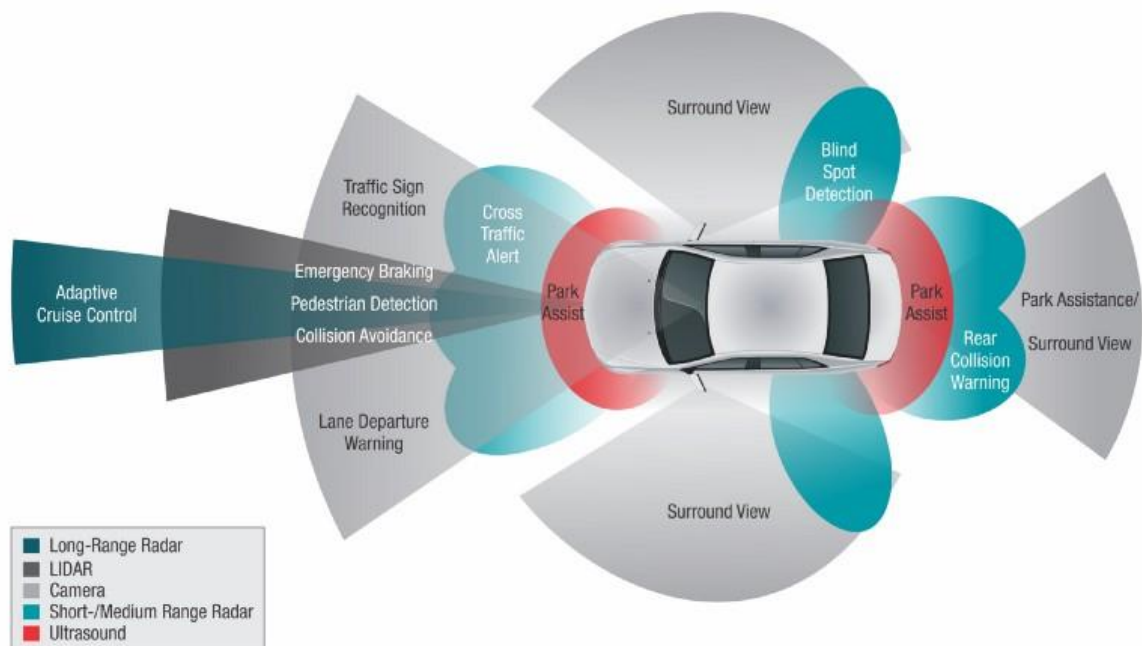


Fig 1. Required sensors for realizing self-driving system

In these days, conventional LiDAR sensors are very expensive due to process issue [2]. Also, in general LiDAR sensor, because of the column sharing structure with scanning method due to the size issue, it was made as a scanning line sensor [2-5, 16]. The scanning sensor has a fatal disadvantage that it has to rotate. There is a structural difficulty in matching the motor and the sensor for rotation, a factor of raising the price, and also there is a problem of durability because it has to rotate physically.

In this paper, a scanless single photon avalanche diode (SPAD) based LiDAR array sensor system is introduced using a key device, SPAD, to measure the attenuated light from a long distance. This is a sensitive device that can react to one photon by using geiger mode with infinite gain while adding excess bias to the breakdown voltage that is applied in general avalanche photodiode(APD) [6]. The sensor can distinguish between background light and signal light by using multi-SPADs to trigger time-correlated single-photon counting (TCSPC) using spatiotemporal correlation for better response. However, due to the incompleteness of the SPAD, it has a low SNR. To solve this problem, a SPAD is aligned to a TDC to solve the SNR problem by measuring a lot of the values for Histogram. The problem is that the memory for histogram is too large [7] and can not be used as an array. Therefore, it is used as a line sensor through column sharing [3,4].

In order to solve the huge memory problem, I propose a successive approximation register (SAR) histogram using binary search. memoryless in-pixel histogram is implemented and make array sensor to make scanless LiDAR sensor without rotation. In this thesis, I report on the design and characterization of a 30x32 scanless SPAD-based LiDAR sensor with in-pixel Histogram. The system uses 0.11um DBH process. It has a resolution of 30x32 and a range of 96m with 0.75m precision. This thesis is organized as follows. In Section 2, I describe SPAD-based LiDAR system and its problems. In Section 3, I introduce the concept of SAR Histogram and compensate a problem of SAR Histogram. In Section 4, I cover the sensor chip design in detail. Section 5. Finally, this thesis is concluded in Section 6.

II. SPAD-based LiDAR System

2.1 Conventional SPAD-based LiDAR System

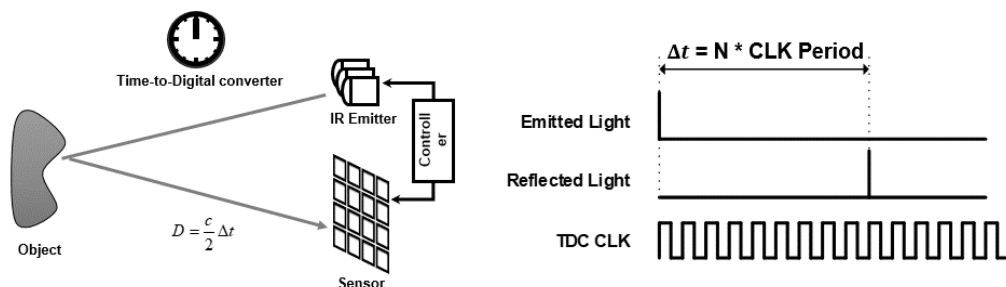


Fig 2. A Principle of Light Detection and Ranging (LiDAR)

LiDAR is a type of time-of flight (ToF), which is a method of measuring the distance by measuring the time difference between a sensor and object. The speed of light is a known value, and time difference can be measured by simply multiplying the distance between the sensor and the object. Conventional structure using LiDAR consists of light source, diode, TDC circuit, and histogram circuit. There is a problem that measuring long distances is not an easy task. Because light spreads along the sphere surface, the number of photons shot from the light source decreases exponentially in fig 3 [1]. Therefore, it is not a problem to measure close distances, but sensitive diodes are needed to measure long distances. Therefore, single photon avalanche diode (SPAD), which can respond to a single photon by pulse, is used as a diode of long distance detector. When a sensor receive reflected light through SPAD, the sensor can get the time difference between time of shooting and receiving light. This time can be measured in a time-to-digital converter using a high-speed clock. However, SPAD, which is a very sensitive device, has a low SNR due to incompleteness from low photon detection probability (PDP), dark count rate (DCR), background light (BGL) and dead time. Histogram circuit is required to solve this problem.

2.2 Single Photon Avalanche Diode (SPAD)

A photodiode receives light in the reverse bias and generates a reverse current by drift. In the case of a general photodiode, a very small current of the level of pA to fA flows and integrates it to measure light intensity. Avalanche photo diode (APD) structure that amplifies photon in avalanche by applying reverse bias at breakdown voltage has been researched and SPAD in geiger mode which amplifies a photon to infinity by adding extra voltage to breakdown voltage has been researched in fig 4. Conventional SPAD operates by applying a strong reverse bias between p + active area which is the light receiving area and n-well. By applying a high reverse bias, a multiplication region is formed between the p + layer and the n-well and a high e-field forms avalanche. The important point is that the strong e-field must be evenly spread. Therefore, SPAD has a circular structure. In addition, the e-field tends to be strong at the corner. The corner effect requires a guard-ring that lowers the corner doping concentration and lowers the corner effect to resolve uneven e-fields [8, 9]. Conventional structure, p-well Guard-ring, distributes doping evenly using low doping around p + in fig 5 and it can be confirmed through T-CAD simulation [10].

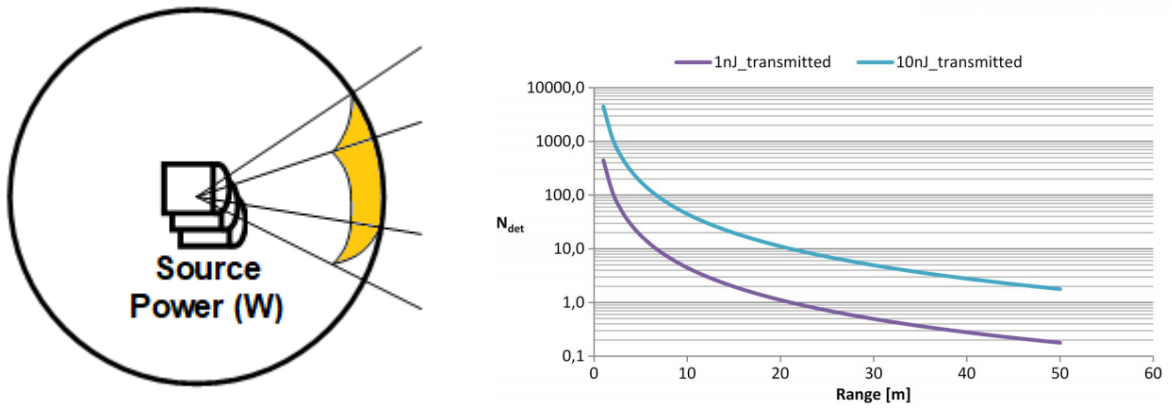


Fig 3. Light intensity at surface of sphere. The intensity of the light exponentially decreases because it spreads along the surface of the sphere.

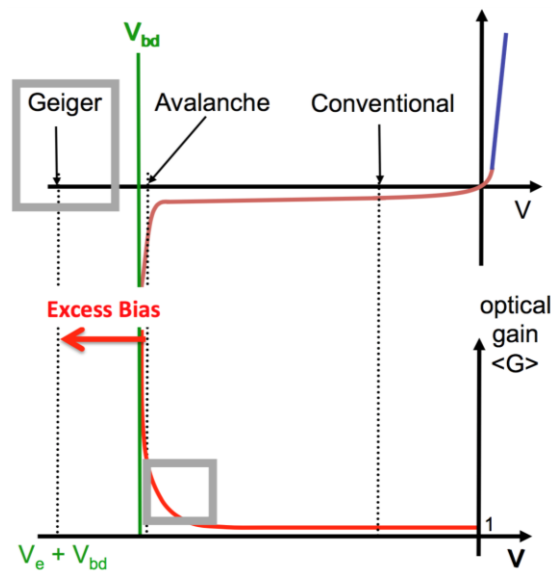


Fig 4. I-V Characteristics of photodiode. Photodiode operates at reverse bias. If the reverse bias is at breakdown voltage, it act as avalanche and if reverse bias is over breakdown voltage as excess voltage, it will be in geiger mode with infinite gain.

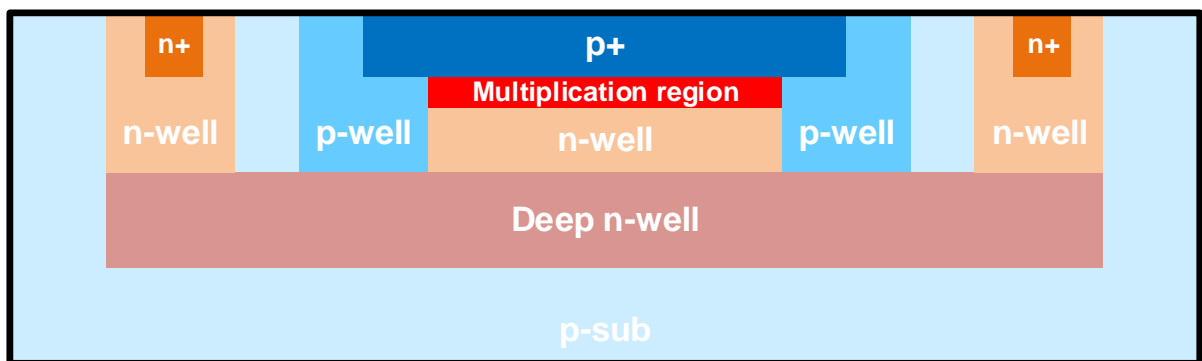


Fig 5. Cross-sectional view of a conventional p-well guard-ring for attenuating corner effect.

2.3 Quenching Circuit

The SPAD is saturated by avalanche with one photon as described above. If so, a plan is needed so that the SPAD can respond again. Quenching circuit is required for this.

SPAD Operation

1. Apply Breakdown Voltage (V_{BD}) + Excess Voltage (V_{EX}) to both ends of the SPAD.
2. Diode reacts to photon and flows a lot of current. (Avalanche)
3. The reverse bias is reduced by the voltage drop through R so that it does not respond to light (Quench)
4. Recharge the VSPAD node gradually to restore reverse bias (Recharge)
5. Repeat steps 2-4.

First, the SPAD operation responds to photon, which causes a lot of current to flow through the avalanche, and the reverse bias applied to the SPAD due to the quenching resistance weakens and exits the Geiger mode. The reverse bias is recovered by the current source R and the SPAD can react again in the geiger mode. At this point, the issue is how long should be recharged. This is because when the recharge is performed for too short a time, the amplified electrons from the previous avalanche cannot be recharged perfectly. Therefore, some electron can be trapped and react by the next avalanche. This is called secondary after-pulse. However, if the recharge time is too long, the SPAD cannot react by photon during the time and is called dead time. Therefore, after-pulse should be avoided through proper dead-time and dead time should be reduced as much as possible, generally 40-100 ns is used [3, 4, 6, 11].

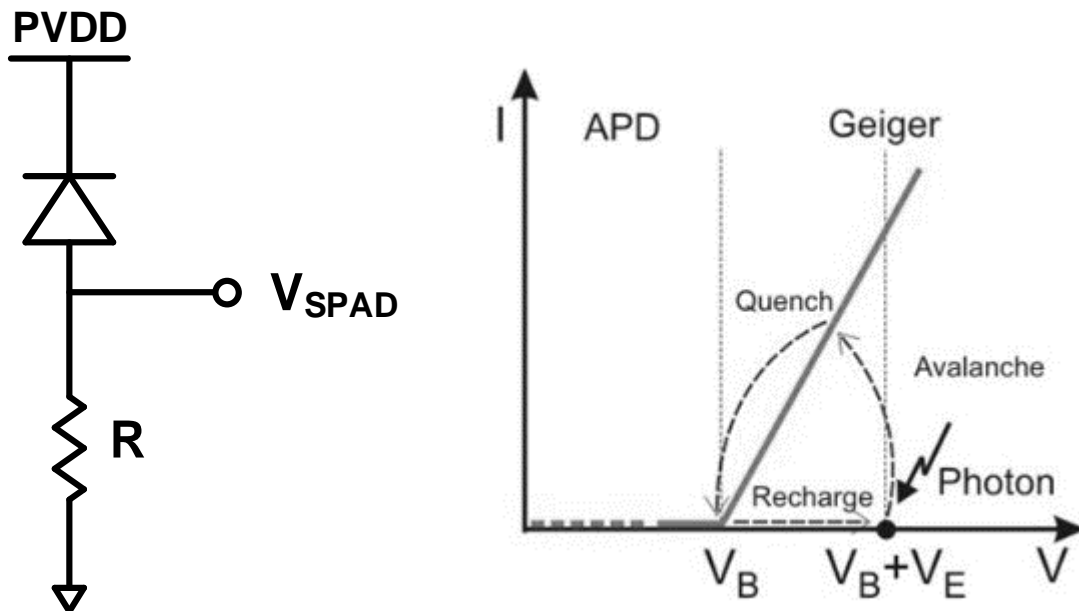
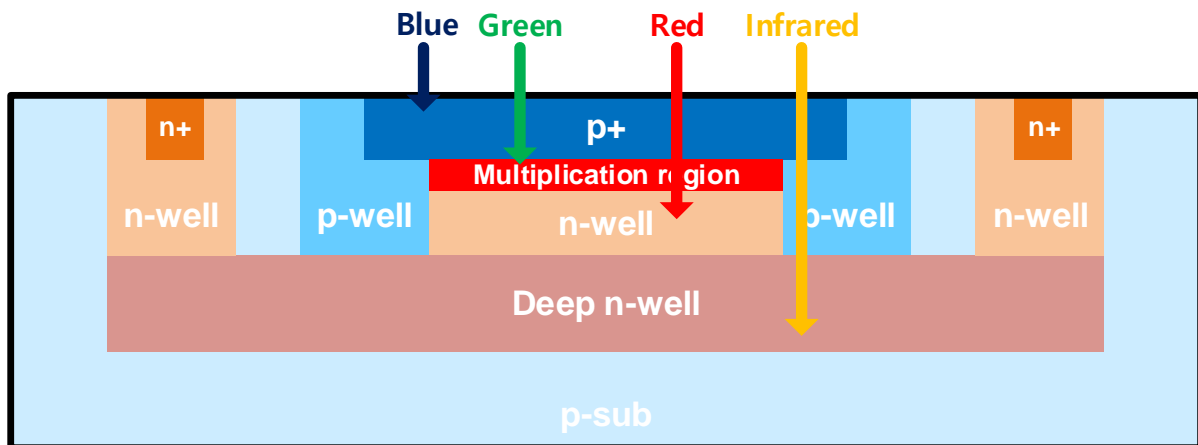


Fig 6. SPAD Operation. Voltage bias is applied as V_B (Breakdown Voltage) + V_E (Excess Voltage), and avalanche occurs by a photon when SPAD is in geiger mode. SPAD is quenched by a lowered bias to V_B and recharged for reacting again.

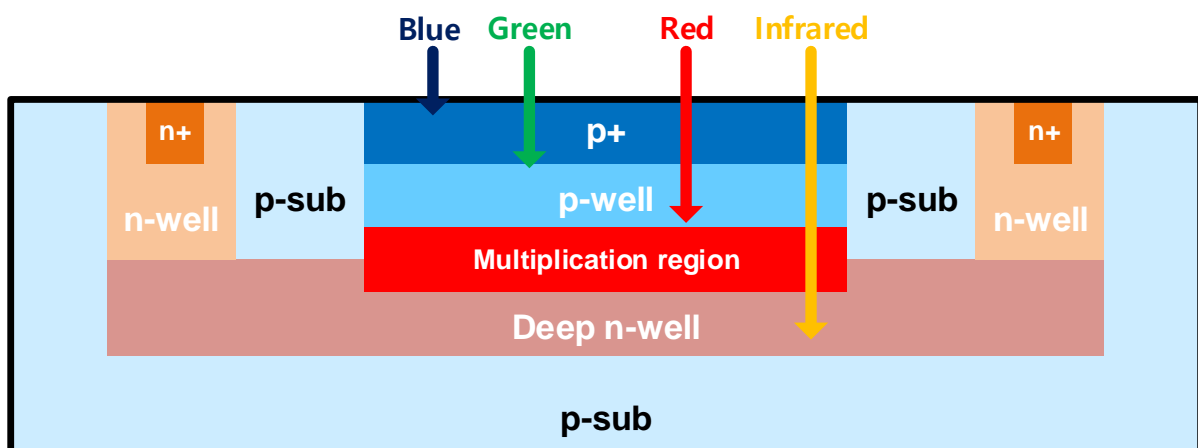
2.4 Incompleteness of SPAD

A. Photon Detection Probability (PDP)

Silicon has different absorption coefficients depending on the wavelength range of light. Therefore, the probability that a reaction can occur depends on the wavelength range. Among them, the absorption coefficients of infrared (IR)-wave used in LiDAR is too low to react in silicon due to its low coefficient. Even though the light can react well, the SPAD is a small active area that receives light compared to the diode size. The ratio of a pixel's light sensitive area to its total area is called the fill factor (FF). In the case of SPAD, FF is only 20%. Therefore, even if photon comes in, the probability of responding is low. To solve this problem, advanced virtual guard-ring SPAD is possible to secure the PDP by lowering the position of multiplication region in fig 7.



(a)



(b)

Fig 7. Infrared(IR)-waves reacts deep in silicon because of its low absorption in silicon. (a) The conventional structure has a shallow multiplication region between p+ and n well and is therefore difficult to react with IR-waves. (b) The Advanced Virtual GR structure responds well to IR-waves because it has a deep multiplication region between PW and DNW.

Electron can be generated within pn junction by thermal problem or tunneling [14]. In Geiger mode, just one expected photon such dark signal is indistinguishable with the reflected IR signal. DCR has a problem of lowering the dynamic range of the image sensor. Therefore, the dark signal source should be removed near the multiplication region to solve this problem. First, SPAD with p⁺ active region can reduce the dark signal from numerous holes in p⁺. Second, the active layer which determine creation of shallow trench isolation(STI) is applied to the whole diode's area in order to remove dark signal caused by oxidation crack due to STI [12]. Third, to reduce the effect of tunneling, the doping concentration of the layer making up the multiplication region should be lowered. Lowered doping layer will reduce the tunneling effect because the e-field is gently applied compared with high doping concentration. As shown in the advanced virtual GR SPAD, a multiplication region is formed between the low-doped p-well and the deep n-well to not only increase the PDP but also lower the DCR.

C. Background Light(BGL) & Dead time

The Active ToF Sensor, which measures the distance by measuring flight time, is always affected by the background light caused by the sunlight. Not only does it get unwanted light, it also takes a long time to measure by dead time of SPAD. To solve this problem, multi-SPADs are used to use spatiotemporal correlation through multiple SPADs in fig 8. The background light is uniformly distributed throughout the dynamic range. On the other hand, since the reflected IR is concentrated only on a specific time bin, it can be distinguished from BGL if it is measured when there is 2 or more correlations by setting a threshold. Also, it can solve the dead time problem by sharing several SPADs.

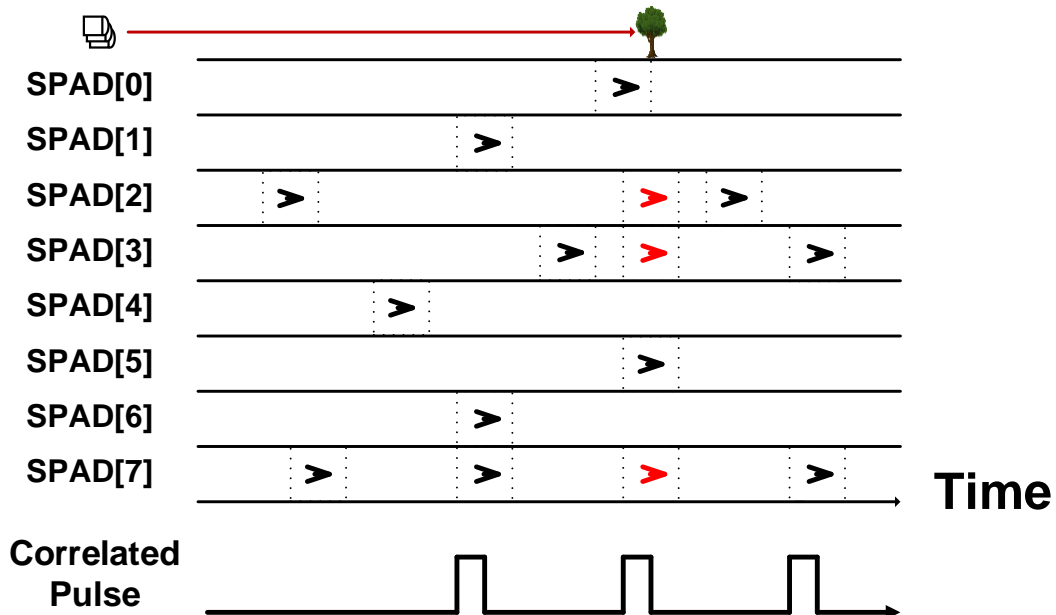


Fig 8. Multi-SPADs for spatiotemporal correlation detection. In order to distinguish background light noise(Black) from reflected IR(Red), Multi-SPADs check the correlation by checking whether more than N SPAD has reacted during one time bin. In this figure, one SPAD is regarded as noise, and two or more signals are regarded as a signal and a pulse is output when N=2.

Because of PDP, DCR, BGL and dead time, SPAD has a low SNR. To solve this problem, histogram is used to compensate for the probability by numerous number of repeated measurements. The problem is that the sensor has to make a lot of measurements for the histogram, so one pixel must be aligned with one TDC circuit and memory is required to store the lots of information. Therefore, to create an array sensor, a TDC circuit and a histogram circuit are required for each pixel, resulting in a very large size. To solve this problem, conventional SPAD-based LiDAR sensors have been using line sensors using column sharing TDC.

2.5 Time-to-Digital(TDC) & Histogram Circuit

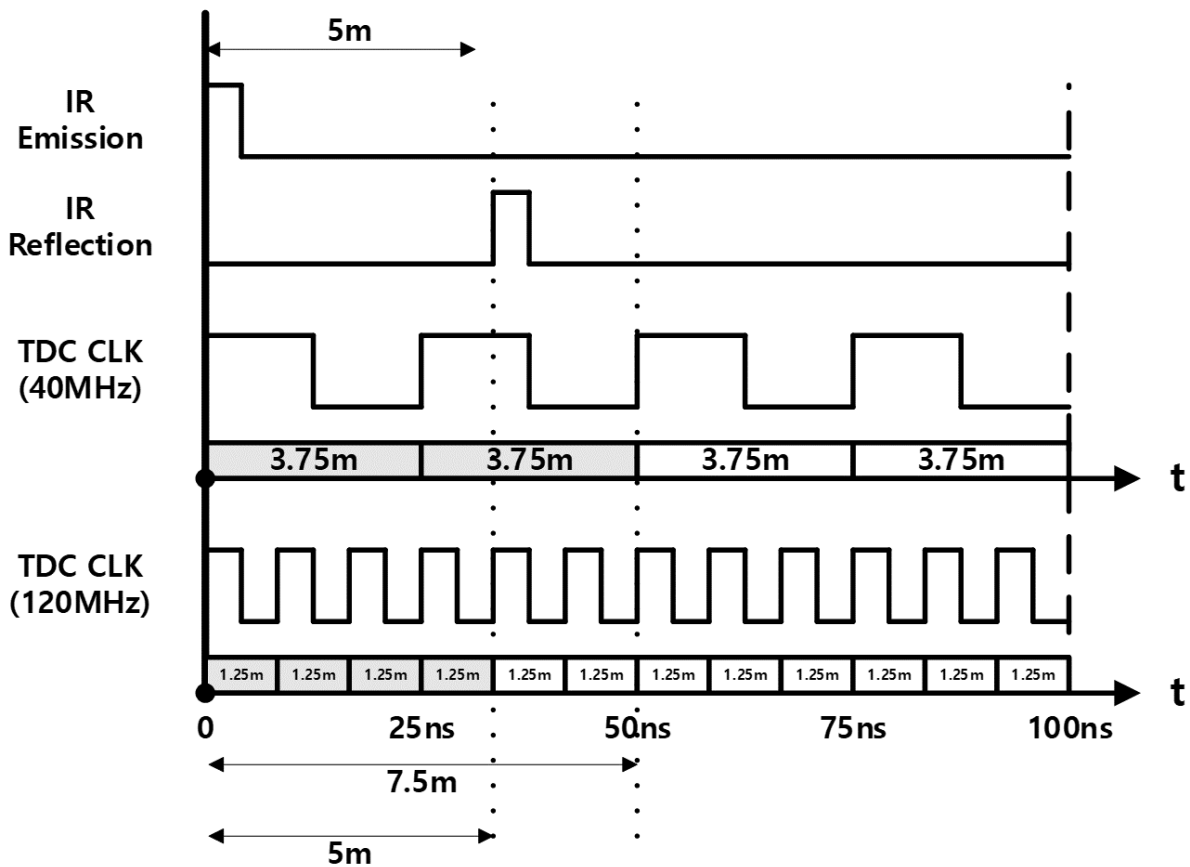


Fig. 9. TDC resolution issue. The actual distance is 5m away. If we take this distance as a 40 MHz clock with precision of 3.75 m, TDC get a result of 3.75 ~ 7 m and have a big error. If you get faster 120MHz with precision of 1.25, TDC can get a relatively accurate value from 3.75 ~ 5m.

A time-to-digital circuit is a circuit that records the time difference between IR Emission and IR Reflection. A fast and precise clock is important for accurate time measurement. For example, assume there is an object at the 5m distance. If TDC uses a slow frequency(40MHz) to measure the distance of this object, it will judge the distance of 3.75m ~ 7m as 7m with 3.75m precision, but if TDC uses fast frequency(120MHz), it can measure 3.75 ~ 5m as 5m with 1.25m precision and you can measure more accurate distance in fig 9. Therefore, a high performance frequency synthesizer is required for SPAD-

based LiDAR sensors with high resolution. In addition, a TDC and a histogram circuit to store TDC information are required for each pixel to design an array sensor. However, if designer adds up to the memory of the histogram for each pixel, the pixel size becomes too large for designing array sensor, and so the image resolution becomes too small. Histogramming TDC allocated 16b of memory per time bin to combine TDC Circuit and histogram circuit to reduce data throughput and reduce process burden with huge memory, 0.03mm^2 per TDC in fig 10 [7].

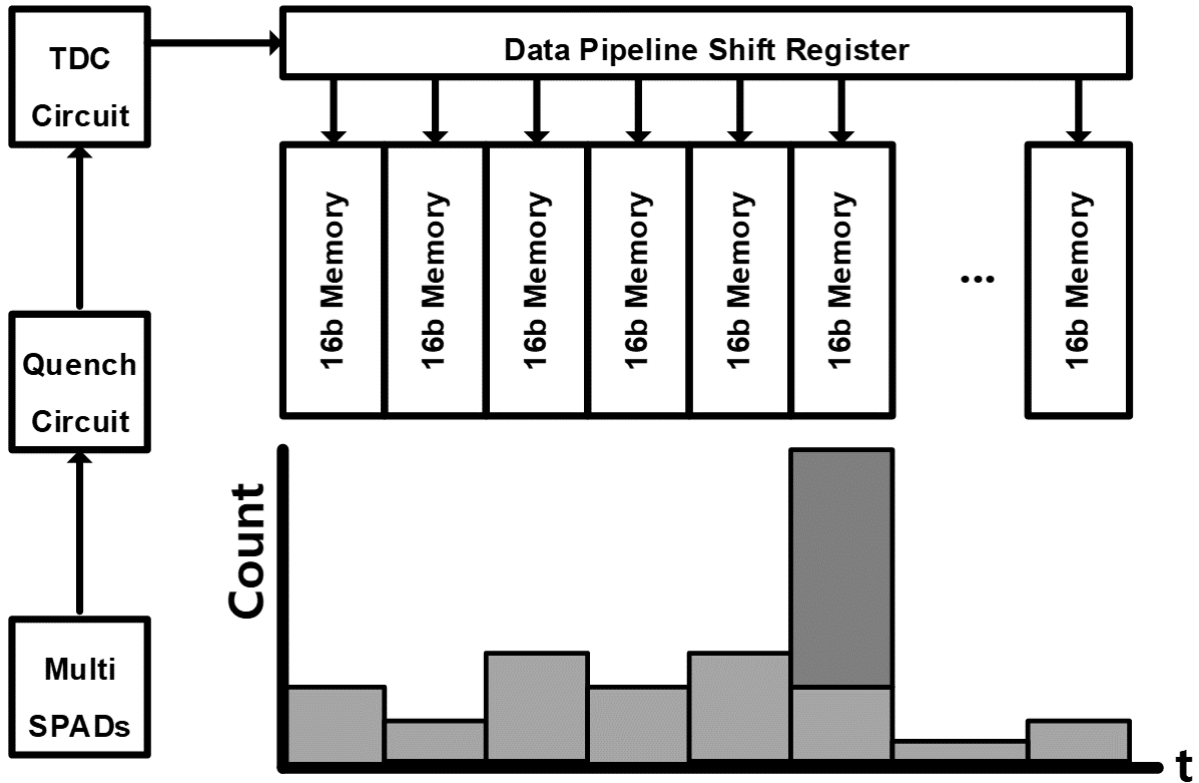


Fig. 10. Histogramming TDC combining TDC and histogram using memory. The problem is huge size by putting 16b memory in every time bin. ($\sim 0.03 \text{ mm}^2$ per 1 TDC)

III. SPAD-Based Scanless LiDAR Sensor with In-Pixel Histogram Array

3.1 Successive Approximation Register(SAR) Histogram Technique

Conventional SPAD-based LiDAR sensors are used as line sensors due to huge memory problem. However, if the memory problem can be solved, SPAD-based array sensor can be designed with high durability and low structural cost. Memoryless SAR Histogram technique is suggested for solution of huge size of in-pixel histogram. SAR histogram is an idea that can cover all dynamic range with only two UP & DOWN time bin through binary search. In addition, just one UP-Down counters is implemented to substitute 2 time bin counter for minimal size. The SAR histogram technique first divides the dynamic range into two time bins, UP and DOWN in STEP1. Then, the information is

gathered through the histogram to determine the position of the object between the two time bins. Secondly, the determined value is stored in the memory. In STEP2, measure except for the section not including object through windowing. Repeat to narrow windowing and finally check the value stored in memory in fig 11.

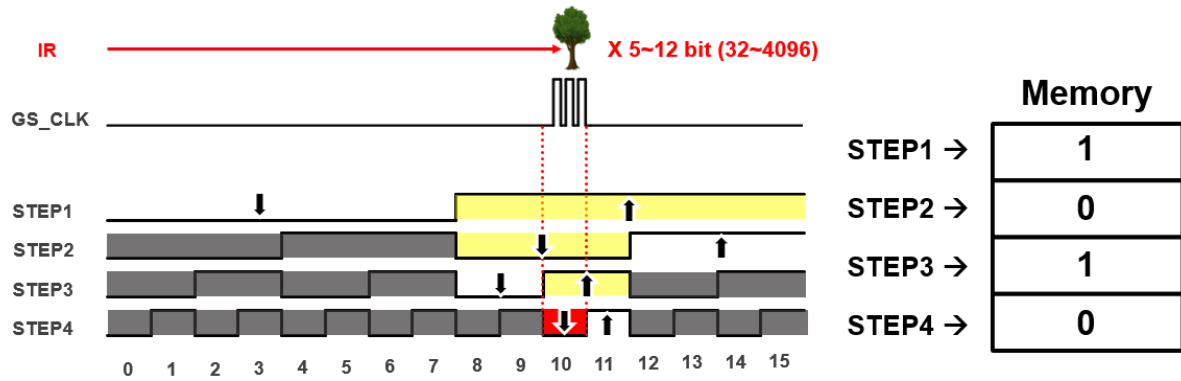


Fig 11. Proposed SAR Histogram Technique. In this figure, a simplified system operate with 4bit time bin. A method of collecting the result of matching the distance of the object and STEP in memory for using binary search and calculating the distance using only two time bin (UP and DOWN).

In this way, the distance can be measured through the value stored in the memory. This method has the advantage of covering all dynamic ranges through only two time bins with just one UP-DOWN counter, but it has a disadvantage that it requires a long measurement time as the number of STEP increases.

3.2 Exponential Photon Counting Technique

If SAR histogram technique is used for memoryless in-pixel histogram, the pixel must determine whether it is UP or DOWN in each STEP. In order to discriminate it correctly, it is designed to discriminate whether the winning time bin is higher than the other one. Exponential photon counting technique is suggested that a technique to increase the number of counting exponentially according to the number of SPADs responding in a time bin so that the multi-SPAD which was used to overcome the existing background light is further advanced and the influence of the background light is reduced and the threshold is reached quickly in fig 12. This can reduce the measurement time of STEP histogram and then compensate for the shortcomings of the SAR Histogram.

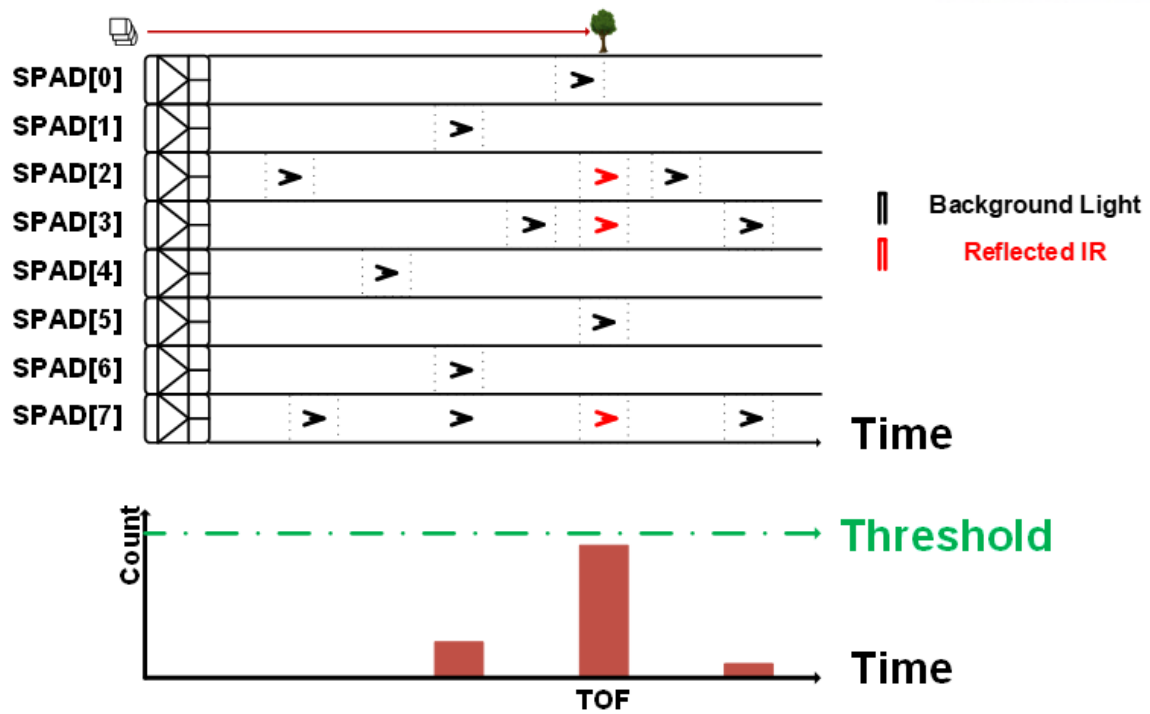


Fig. 12. Exponential Photon Counting Concept. It is a technique to shorten the measurement time by not only checking only the temporal correlation like Multi-SPADs but also reaching the threshold for distinguishing UP and DOWN by giving the exponential weight according to the number of SPADs responded.

IV. Sensor Chip Design

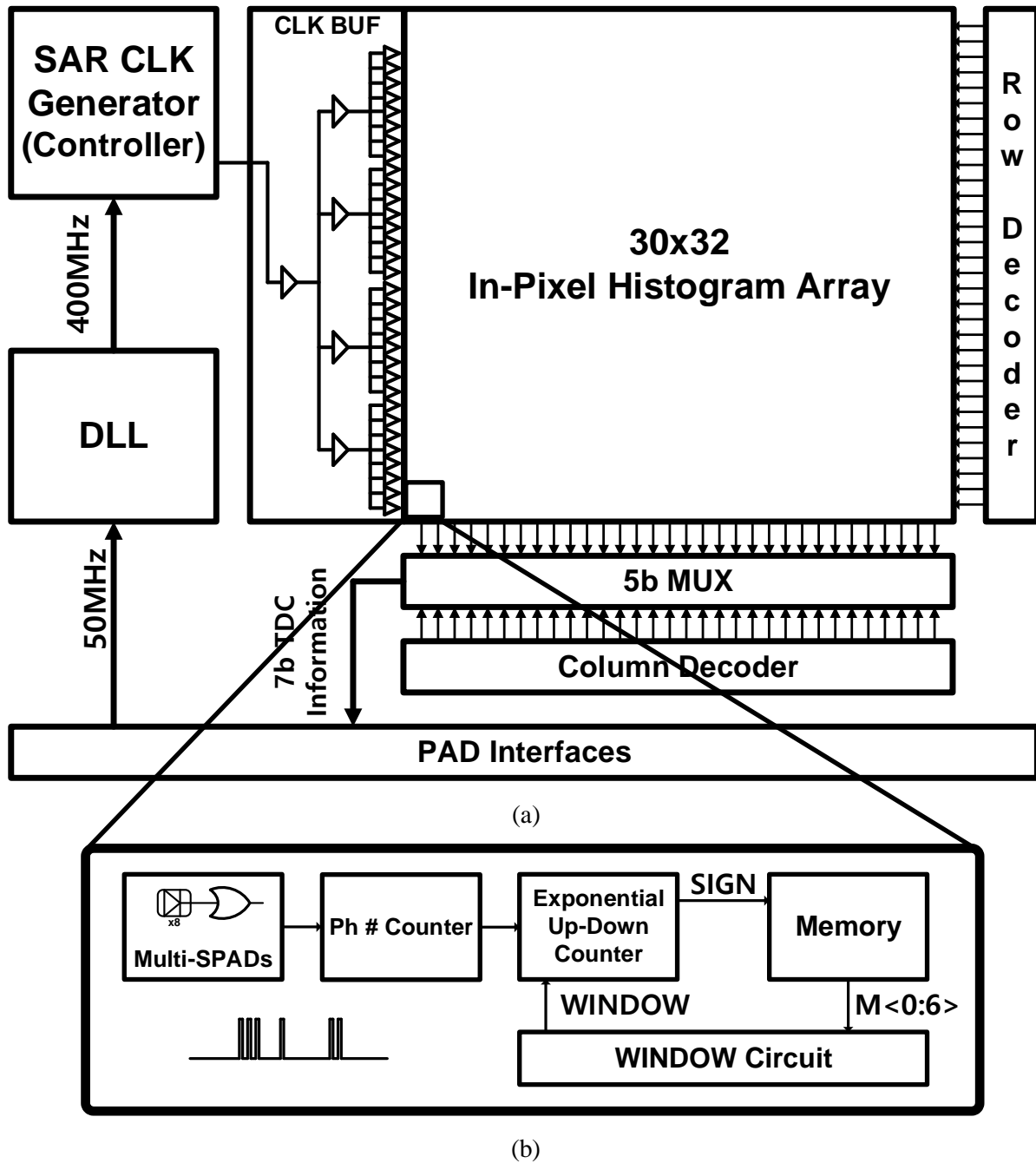


Figure 13. Proposed scanless LiDAR Sensor System with In-Pixel Histogram. (a) This system consists of a 30x32 pixel array for scanless sensing consisting of an in-pixel histogram, a DLL for generating a high speed and a SAR CLK generator act as controller to make control signal. (b) A small size in-pixel histogram is used for SAR histogram Technique.

4.1 SPAD Counter

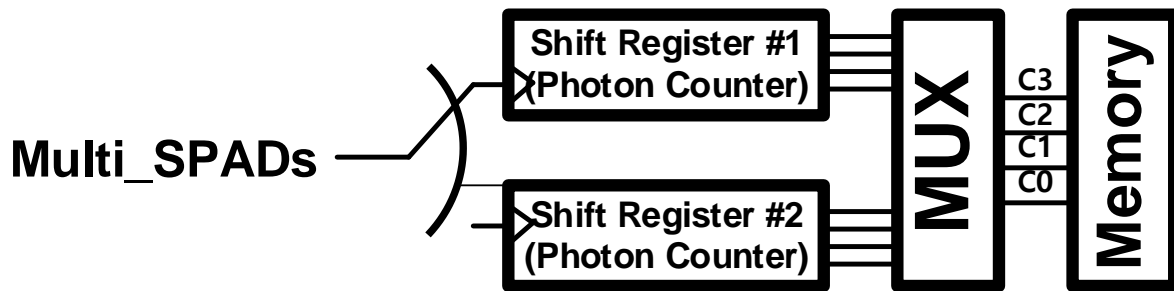


Figure 14. SPAD Counter Block Diagram. It consists of Multi-SPADs for spatiotemporal correlation, dual shift register for avoiding dead time of it, and memory for registering SPAD count during next time bin.

SPAD counter is a circuit that confirms spatiotemporal correlation by checking how many photons come in a single time bin. The pulses of multi-SPADs consisting of 8 SPADs are made into 300 ps pulse and serialized by OR to operate as clock of shift register in fig 14. Check how many pulses are in the 5ns pulse width of 100MHz. This number is used as information for the operation of exponential photon counting in UP-DOWN counter. In this operation, two shift registers are used to reduce the dead time due to the reset time of the shift register.

4.2 Exponential UP-DOWN Counter(EUDC)

Exponential photon counting is implemented by controlling clock and switch through SPAD Counter. It is assumed that this example is operated in UP Counting to simply the implementation.

EUDC Operation

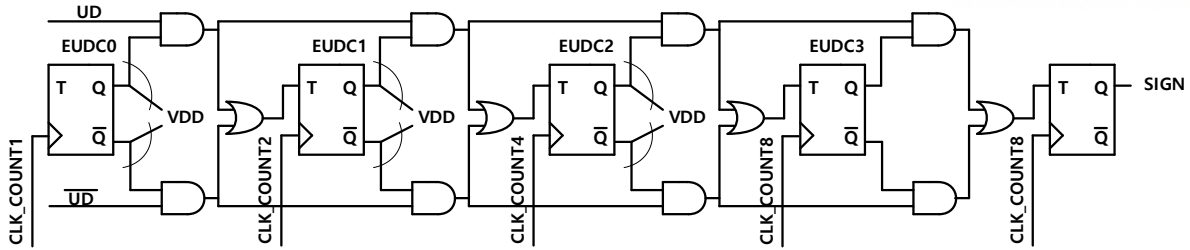
1 SPAD → Do not add the clock to EUDC.

2 SPAD → When two SPAD responds, one count is added to the EUDC. To do this, the LSB is toggled by operating the clock on all bits of the synchronous counter.

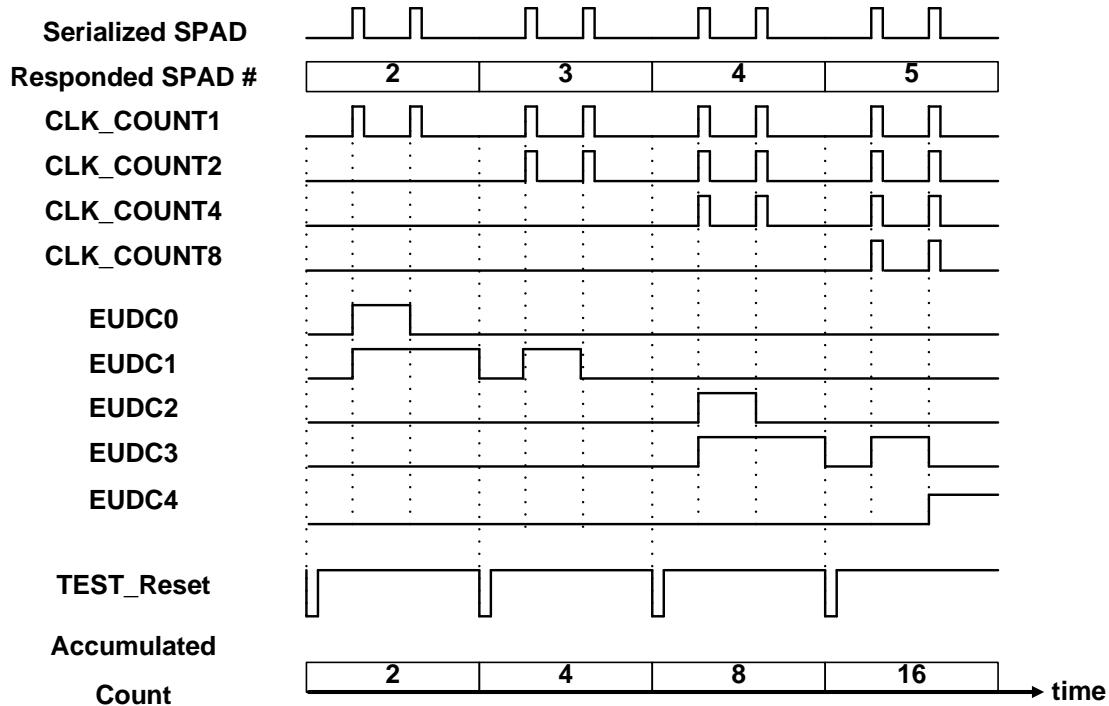
3 SPAD → When three SPAD responds, two counts are added. To do this, CLK COUNT1 is not operated on the synchronous counter, so it starts from 2nd bit instead of LSB. At this time, to toggle the 2nd bit, the value before the 2nd bit is switched to VDD.

4 SPAD → When four SPADs responds, four counts are added. To do this, CLK COUNT1,2 is not operated on the synchronous counter, so it operates from 3rd bit instead of LSB. At this time, to toggle the 3rd bit, the value before the 3rd bit is switched to VDD.

Therefore, 2, 4, 8 and 16 accumulations were observed when the histogram was performed twice for each STEP.



(a)



(b)

Fig 15. Simplified 4-bit Exponential UP-DOWN Counter schematic and timing diagram. (a) Simplified EUDC Schematic which is advanced UP-DOWN synchronous counter by using separate clocks for each flip-flop and adding a switch to toggle next flip-flop without reference to previous value. (b) Simplified EUDC's Timing Diagram for checking the function is confirmed. When the SPAD responds to the two histograms given, the exponential counting can be confirmed by the number of SPADs responded.

4.3 Threshold(TH) Controller

The Threshold Controller is a circuit on how to set the threshold to distinguish UP and DOWN from the EUDC circuit. Depending on the EUDC SIGN_B value, the logic that determines UP or DOWN by comparing count bits with threshold is different in fig 17. In the case of up counting, if one or more of the bits above threshold, TH maintains high voltage, and in the case of down counting, TH is reacted if at least one of the bits above TH is equal to zero. If the TH maintains high until the SAR histogram operation is done, the threshold controller judges Pass as the distance value is a meaningful result. If

TH is toggled by Pass CLK, it becomes Fail. If the value is Fail, it is judged that there is no response by reflected IR as the distance is not properly detected in fig 16.

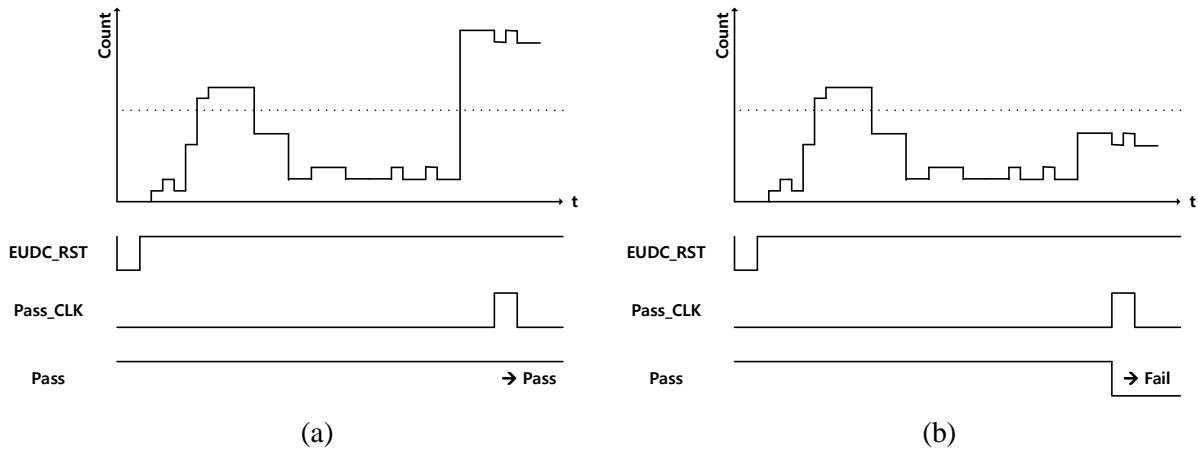


Fig 16. The concept and timing diagram of the threshold controller. The threshold controller sets the threshold to prevent inaccurate distance measurements from insecure information due to inadequate image detecting. (a) Pass. After every histogram, the Pass value remains HIGH when the number of counting exceeds the threshold. (b) Fail. If the number of counting does not exceed the threshold after every histogram, the pass signal is toggled and recognized as Fail.

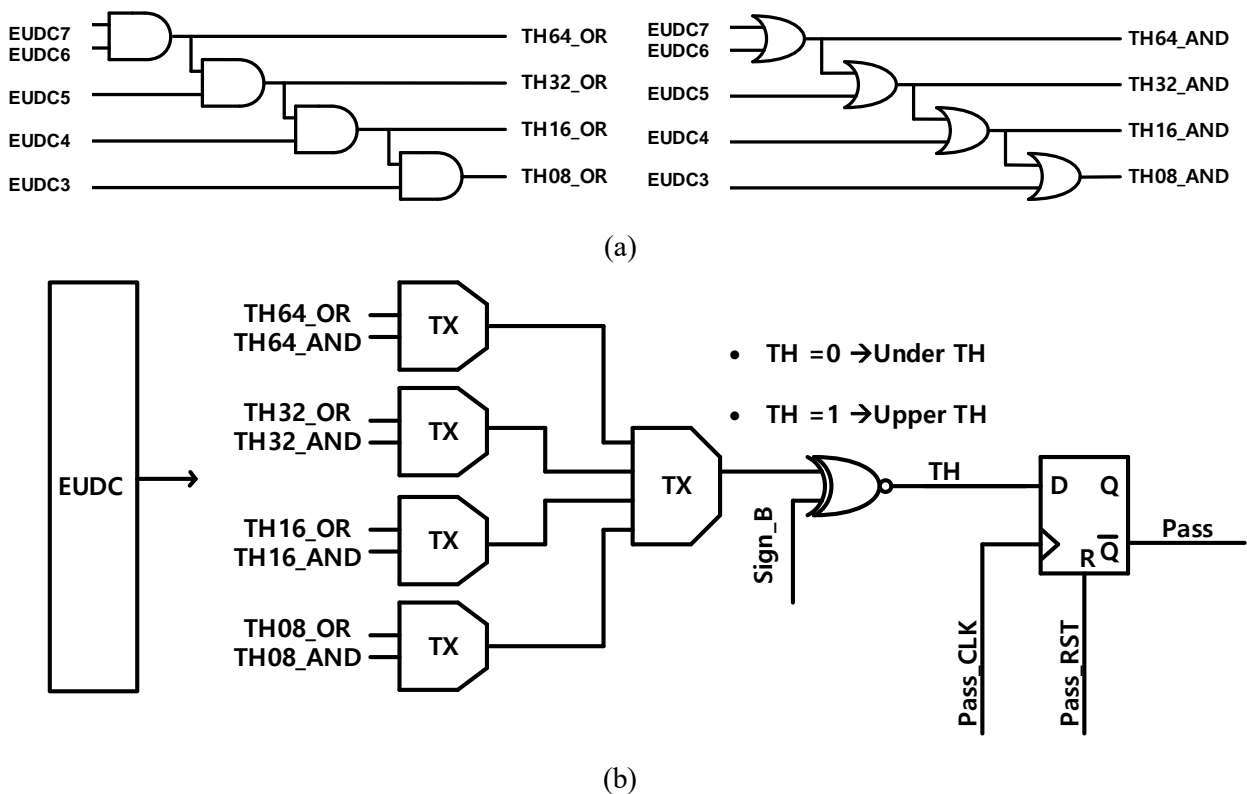


Fig 17. Threshold Level Selector. It is a selector designed to determine the threshold level to which bits of the EUDC should be set. (b) A Block Diagram of Threshold Controller. The TH value is stored in memory by using XNOR between SIGN and value from the EUDC signal passed through the threshold level selector in memory

4.4 Window Circuit

A window circuit is necessary to narrow the gating to obtain the distance through a single time bin of EUDC by substituting the number of original time bins through binary search. The window circuit is controlled by each value stored in memory during N STEPS. Use the XNOR gate to extract time information when STEP signal is equal to the signal of memory in same bit. And then, AND gate is used for narrowing gating width by overlapping each output of XNOR.

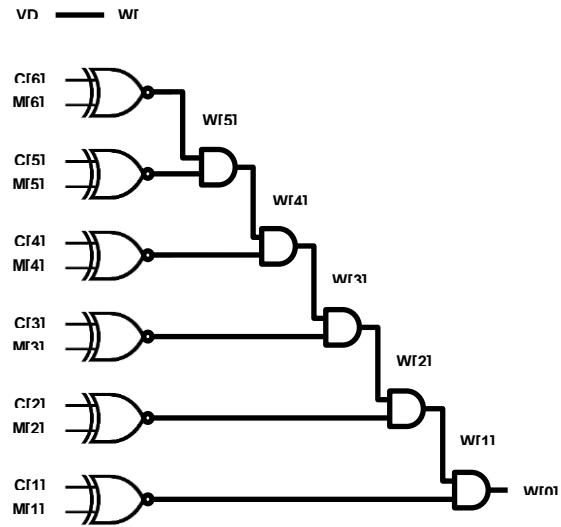


Figure 18. A schematic of window Circuit narrowing the gating by comparison STEP signal with values of memory.

4.5 Delayed-Locked Loop(DLL) Circuit

To implement the SAR histogram technique, a sensor system requires a block that can synthesize a fast clock. In order to satisfy the proposed specifications, a speed of 400MHz and a higher spec for more precise detection. A small jitter is required for accurate results. Therefore, I designed a 1.6GHz delay-locked loop (DLL) with low jitter because the jitter is not accumulated compared to the phase-locked loop (PLL) that accumulates jitter through the loop in fig 19 [15]. A current-starved delay cell induces a delay by forcing the speed of the inverter down in fig 20. The delay line is designed using 32 delay cells to accurately lock the 50 MHz reference clock (REF CLK) and delayed clock (Delayed CLK). Note that the locking range of the reference clock and the delayed clock must be carefully designed so that harmonic locking does not occur. When locking is performed, it should be designed as symmetric as possible in order to minimize the mismatch in the frequency phase detector (PFD) to ensure accurate locking. The Q_A and Q_B signals thus obtained control the switch to flow current to the CP. In this case, both the NMOS and PMOS current sources must be supplied with the same current for accurate locking in fig 21. In this case, in order to flow the correct current, the channel length modulation, which changes the current amount according to the drain value, should be removed. And the cascoded current source is used so that the NMOS and PMOS flow the same amount of current. However, a charge sharing due to parasitic capacitance, C_N and C_P , causes a problem even if the same amount of current can be flowed from current source in fig 22-(a). Depending on the parasitic size and the locking voltage level, it is difficult to achieve accurate locking. In fig (b), V_{XN} and V_{XP} nodes have a problem of fluctuation between the locking voltage(V_{CP}) and GND or VDD, and cap sharing

occurs in the condition. To solve this problem, the charge pump requires bootstrapping to make the VXN and VXP nodes maintaining each potential through the unity gain buffer. In this case, the amount of change in charge is greatly reduced, which can prevent the locking effect from degrading due to cap sharing in fig 22-(c).

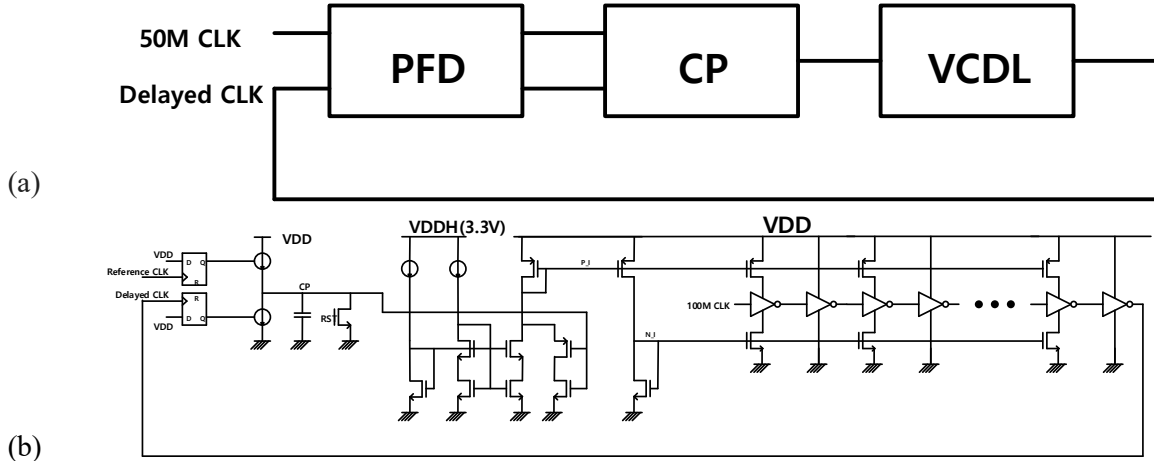


Fig 19. Delay-Locked Loop(DLL) Block Diagram (a) Simple block diagram of DLL consisting phase frequency detector(PFD), charge pump(CP) and voltage-controlled delayline(VCDL). (b) A detailed block diagram of DLL.

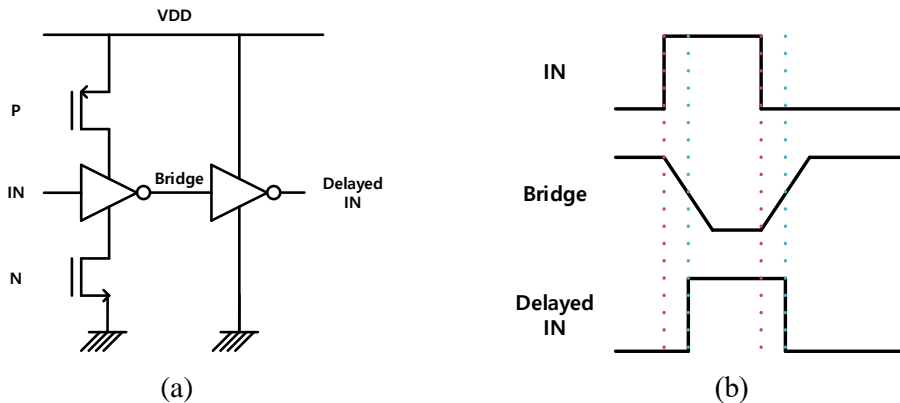


Fig. 20. Current-Starved Delay Cell. (a) A schematic of current-starved delay cell. (b) A principle of Current-starved delay. Delay the incoming pulse through the starving current source and then restore the delayed pulse through the fast inverter.

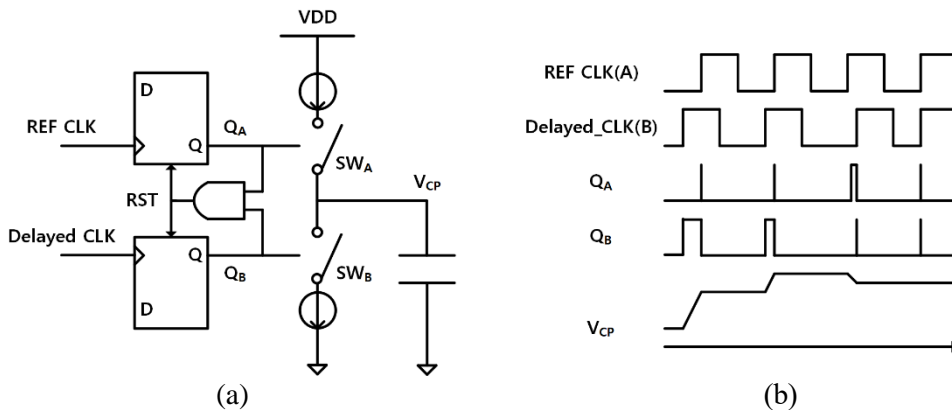


Fig 21. Phase Frequency Detector(PFD). (a) A schematic of PFD consists of 2 flip-flops to control switches as mismatch between 2 input signals. (b) Timing diagram of PFD. If there is a mismatch between input signals, control the V_{CP} by implementing the pulses, Q_A and Q_B.

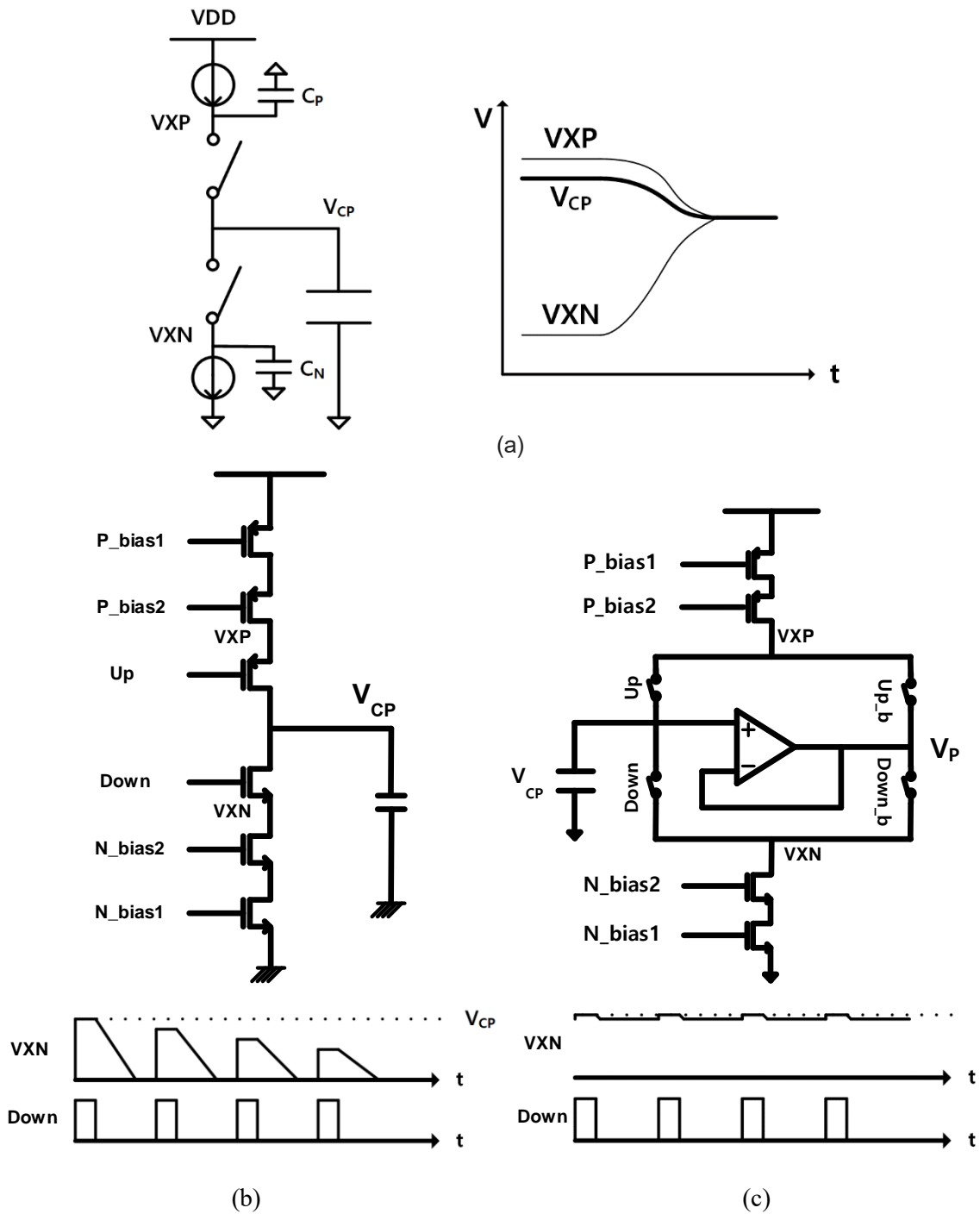


Fig 22. Bootstrapping to avoid charge sharing. (a) Charge Sharing between C_P and parasitic capacitance, C_P and C_N , causes incorrect charge accumulation. (b) General cascoded charge pump with the charge sharing (c) Charge pump with bootstrapping to avoid charge sharing.

V. Result

5.1 Simulation Result of In-Pixel Histogram with SAR Histogram

Assumption

Single Pixel Simulation

Period of repetition of emitting laser	: 640ns
Distance	: 421.5ns (+5ns → 85 th bin = 1010101)
Responded SPAD #	: 4 (16 count)
Histogram #	: 4 (1 RST Period + 3 Histogram)
Estimated Result	: 16 x 3 = 48 counts per STEP
Threshold Level	: 32 counts
The # of STEP	: 7

A. Multi-SPADs

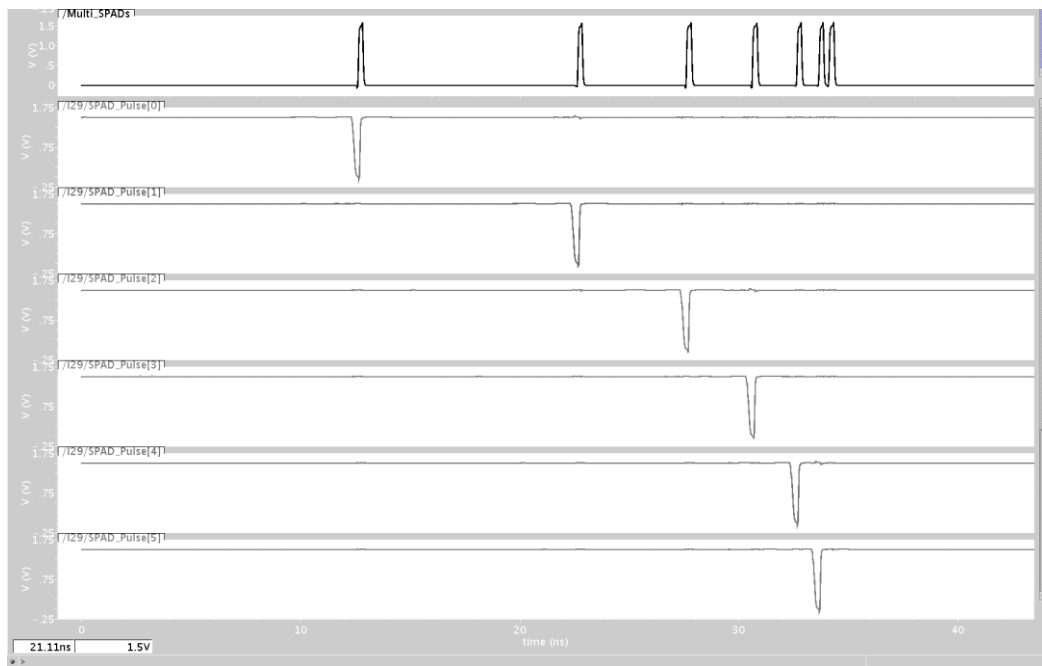


Fig 23. Simulation Result of Serialized Multi-SPADs with 300ps pulse by edge detection

Multi-SPADs are concepts using spatiotemporal correlation. To see the correlation, a SPAD Pulse with dead time of 100ns was passed through edge detector to make 300ps pulses and the pulse was serialized.

B. SPAD Counter

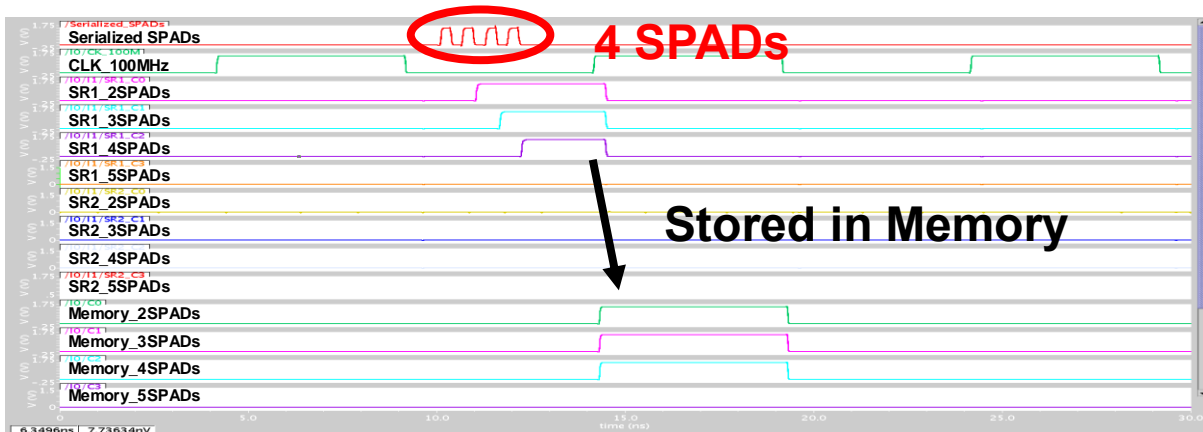


Fig 24. Simulation result of SPAD Counter showing the operation of dual shift register when 4 SPADs are responded.

The serialized pulses generated in Multi-SPADs are correlated within 5 ns pulse width at 100MHz. As one assumes, four pulses are detected. One pulse is used to distinguish from noise, and 3 pulses are stored in the shift register. At this time, in order to remove the dead time of the shift register, two shift registers operate alternately, so the value is stored in the memory before the next operation.

C. Exponential UP-DOWN Counter

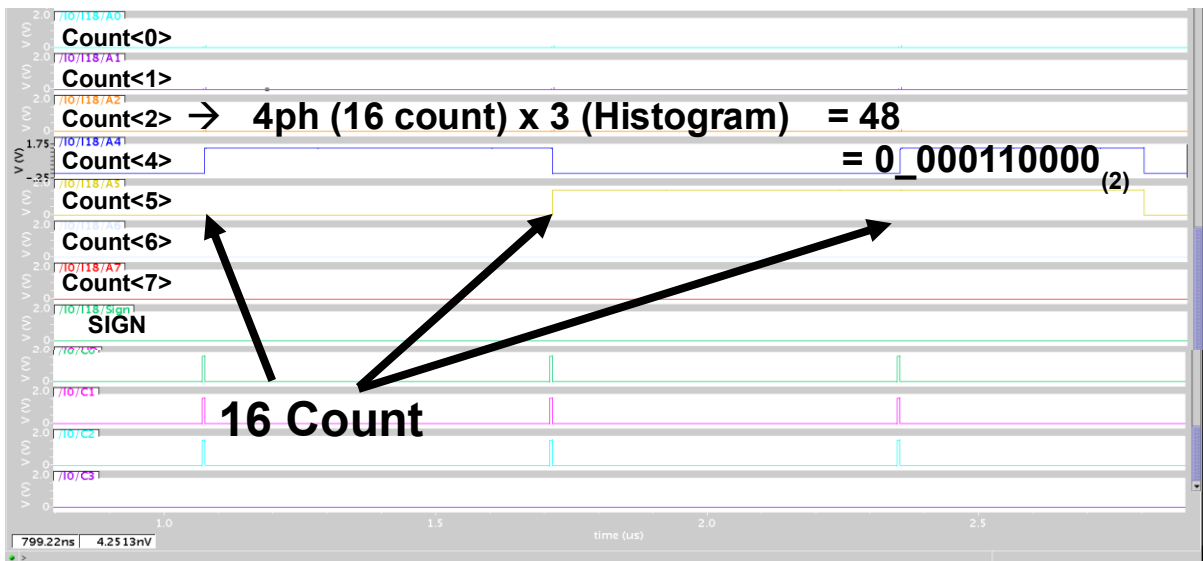


Fig 25. Simulation result of exponential UP-DOWN counter which accumulates 16 count per repetition. After 3 times repetition for histogram, 48 counts are accumulated during one STEP.

Exponential UP-DOWN Counter performs exponential counting through information obtained from SPAD Counter. In fig (), 4 SPADs must react and count 16 times at a time, so Count <4> in Count <0: 7> must be toggled. In total 4 histograms, it should be 48 counts through 3 times detection except reset period, and it can be seen that the value of 000110000 (2) was stored correctly in EUDC after 3 operations.

D. Window Circuit

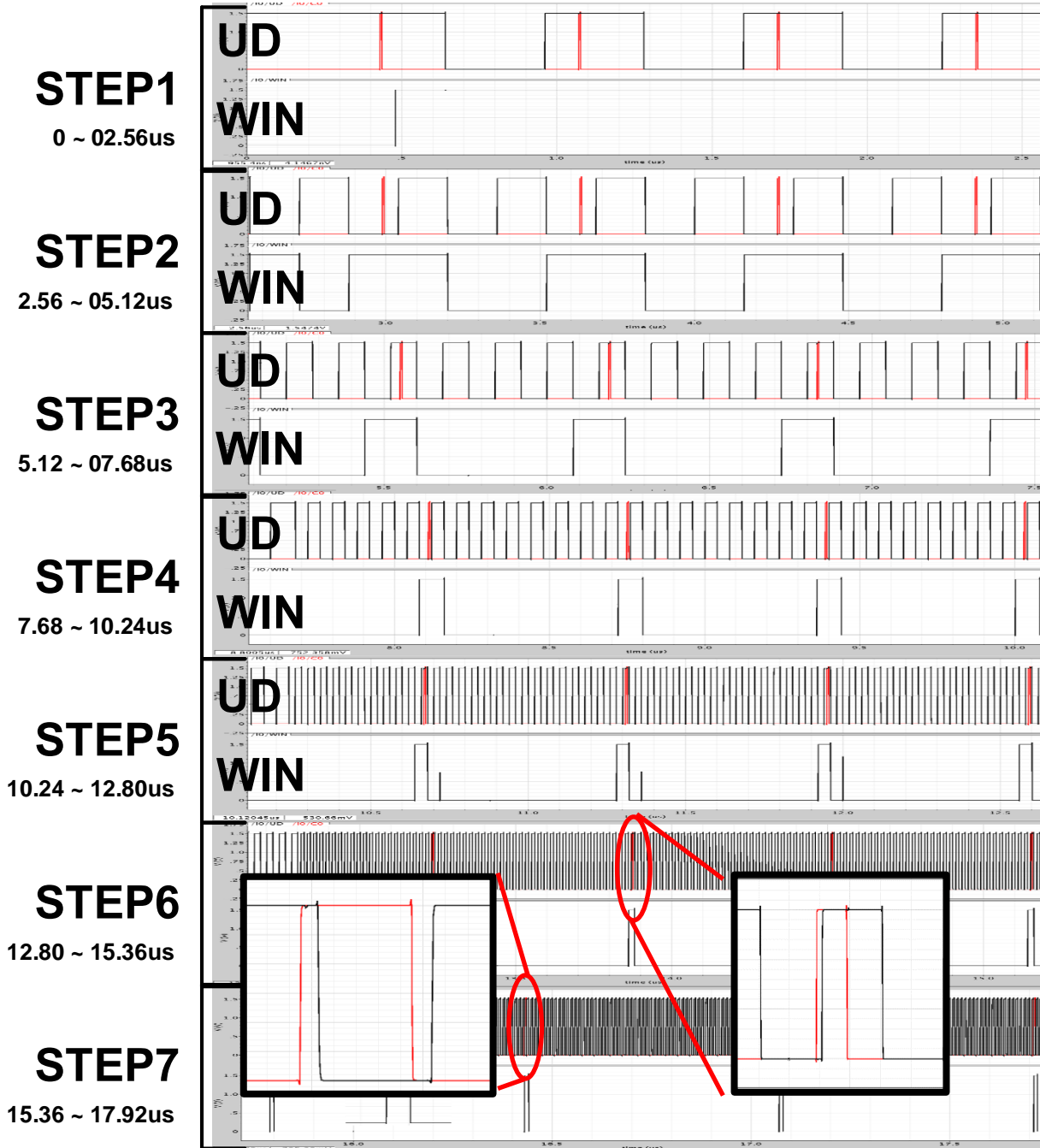


Fig 26. Simulation result of window circuit. As the 7 STEPs proceed, the UD and WIN signals become narrower, resulting in a distance to the object.

The window circuit consists of a window (WIN) signal, which means the time to confirm the response of the SPAD, and a UD signal, which distinguishes between DOWN (low) and UP (high) in WIN signal. The window works by checking the UD every 7 steps to get 7bit time bin information. The results in STEP1 check SPAD response during all of time bins, and the red signal located in the UP is confirmed. As a result of STEP1, WIN in STEP2 has decreased to UP time bins where the object is located in STEP1. In STEP2, the position of the object is located at DOWN. As narrowing the WIN signal, the WIN shrank to match the result of 1010101₍₂₎. Using the window circuit, the distance that I originally assumed 85th time bin was measured correctly by using the results stored in the memory.

5.2 Simulation Result of DLL

A. Charge Pump Current Source with cascaded current source

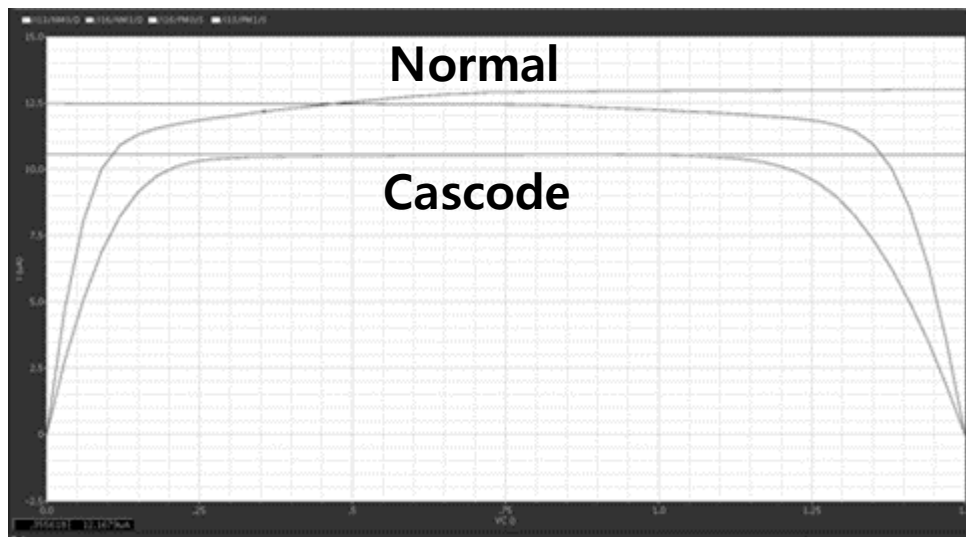
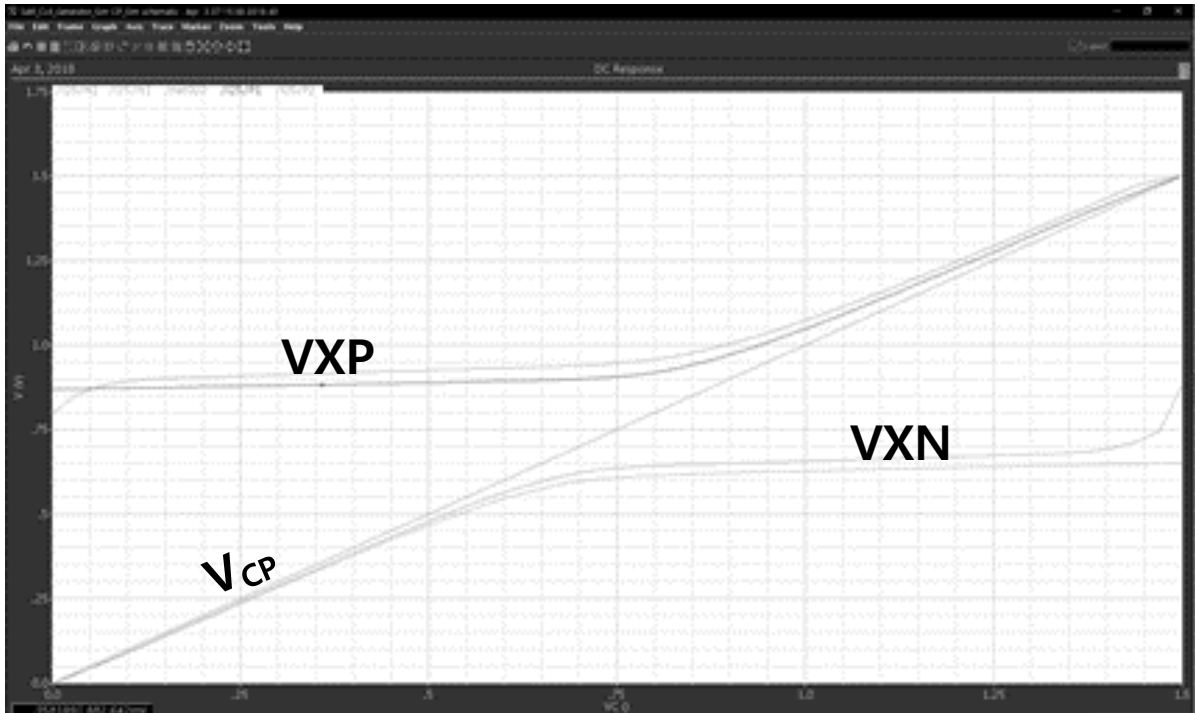


Fig 27. Simulated result of comparison between normal current source and cascaded current source.

The DLL must be able to lock precisely so that there is no mismatch between the reference clock and the delayed clock. To do this, the charge pump must be designed so that the NMOS and PMOS can flow the same current. A cascoded the current source allows charge pump to use accurate current source compared with normal current source affected by the channel length modulation the potential of the charge pump within a locking range between 0.5 and 1V. Simulation results show that the normal current source has a 7% difference between NMOS and PMOS, whereas the cascoded current source is an accurate current source with a small mismatch within 0.6%.

B. Bootstrapping charge pump



(a)



(b)

Fig 28. The simulation result of charge pump with bootstrapping. (a) DC analysis of bootstrapping to attenuate cap sharing (b) Transient analysis of bootstrapping in locking phase with small fluctuation under 0.1V.



Fig 29. The simulation result of DLL locking between reference clock and delayed clock by controlling CP switches with PFD signal, Q_A and Q_B

The bootstrapping attenuating the cap sharing is used for accurate locking of the charge pump. Same potential among VXN, VXP and locking potential(V_{CP}) were expected. In fig 28-(a), each voltage is different among VXN, VXP and V_{CP} in the locking range between 0.5 and 1 V in dc analysis. Because the capacitance of 10pF is controlled by 10uA of current source, a constant V_{DS} is required to flow the current through the switches. However, since it has a constant value, there is no problem in removing cap sharing. The transient analysis with reduced fluctuation under 0.1V confirms the results of bootstrapping in 28- (b). With the charge pump with bootstrapping, which allows a precise current flow, the accurate locking under 20 ps spur is achieved regardless process variation in fig 29.

5.3 Layout of Sensor System

A. SPAD Structure

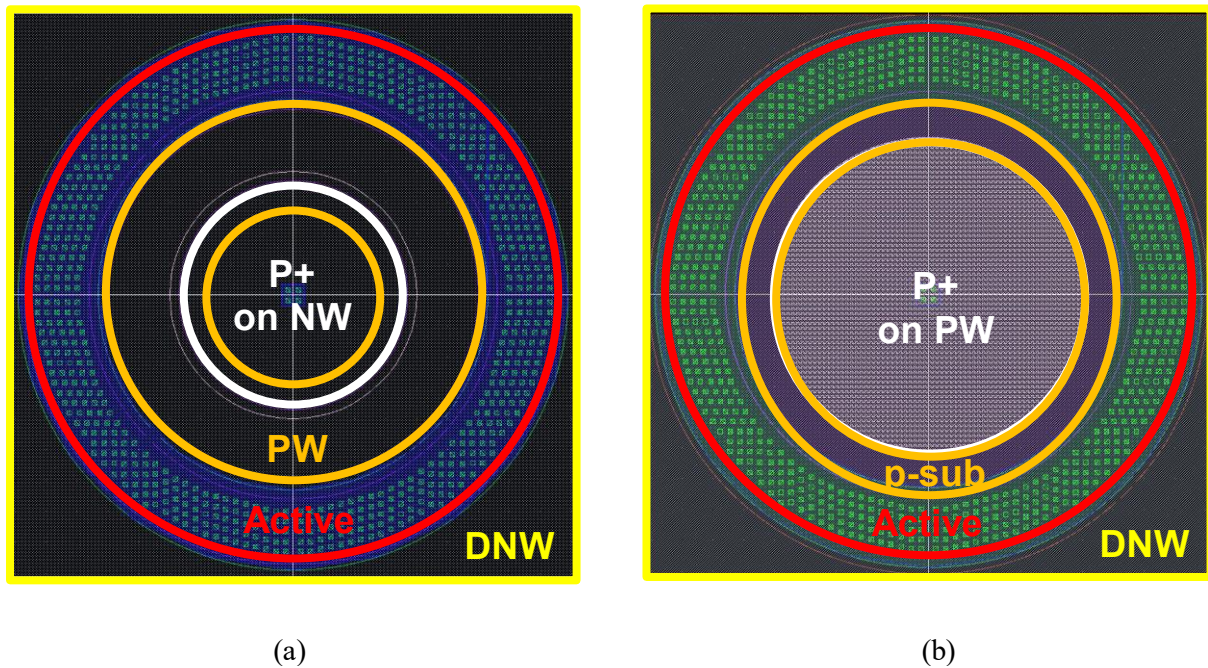


Fig 30. SPAD Layout. (a) Conventional p-well GR SPAD with 20 μm pitch and 4.5 μm radius active region. (b) Advanced Virtual GR SPAD with 20 μm pitch and 5 μm radius active region

It is a SPAD structure which is a key device in LiDAR Sensor. In fig 30-(a), the conventional structure has a pitch of 20 μm and the radius of p + region is 4.5 μm . The breakdown voltage of conventional SPAD is 10V. In order to mitigate the corner effect, a guard-ring is formed in the p-well around the active area. As a result, DCR of 20kHz is obtained when an excess voltage of 1.1V is applied. In 30-(b), the advanced virtual guard-ring SPAD has a 20 μm pitch and the radius of p + region is 5 μm . The breakdown voltage of advanced SPAD is 15V. We used a virtual guard-ring structure in which the multiplication is located at a lower place to improve the PDP in the IR-wave while mitigating the corner effect. As a result, 7% PDP was obtained at 1kHz DCR and IR-wave when 1V Excess voltage was applied.

B. Pixel

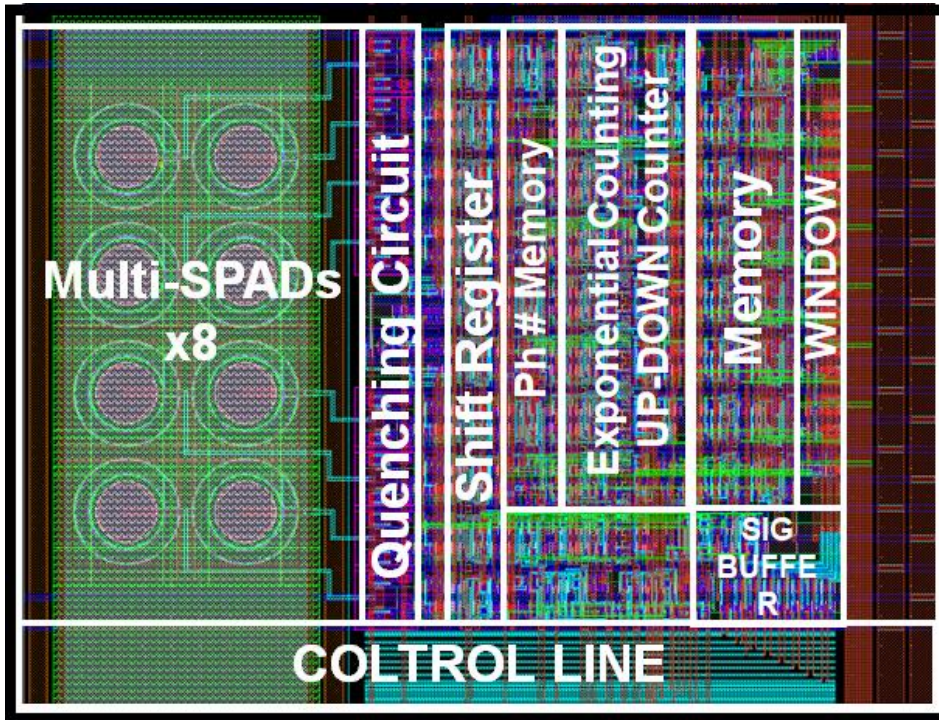


Fig 31. 155µm x 115µm in-pixel histogram layout

C. Sensor system Layout

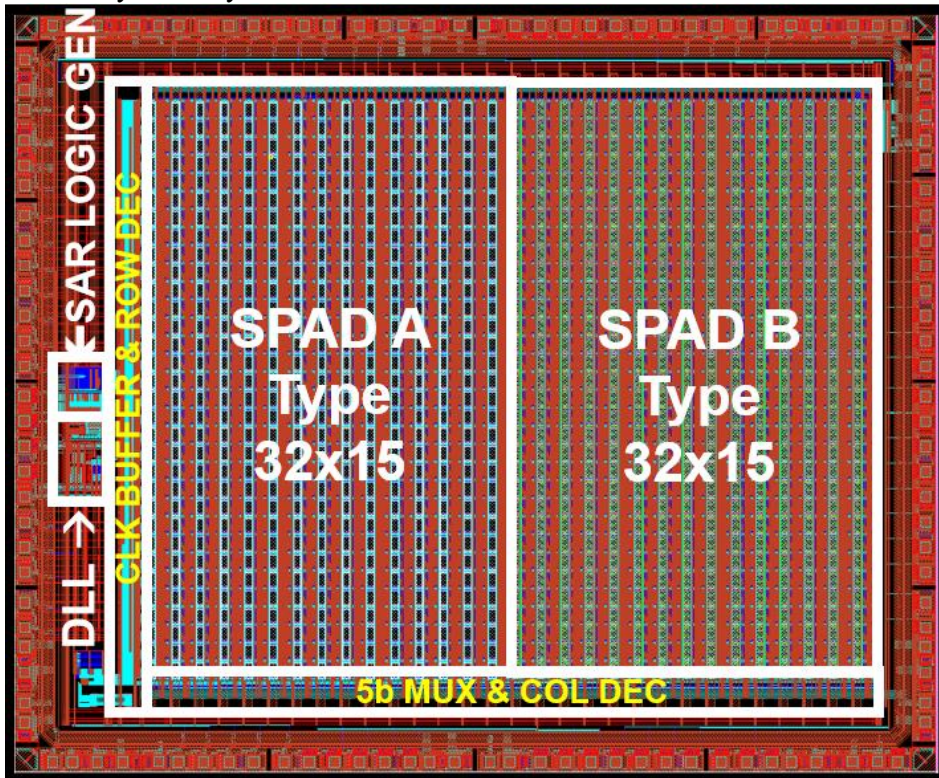


Fig 32. 4850µm x 5900µm scanless SPAD-based LiDAR System layout

VI. Discussion

Table 1. Comparison of performance with State-of-Art Papers

Parameter	Unit	Niclass JSSC 2013[3]	Niclass JSSC 2014[4]	Perenzoni ISSCC 2016[11]	Ximenes ISSCC 2018[16]	This Work
Depth Image Resolution	Pix	340x96	202x96	64x64	256x256	30x32
CMOS Process	-	0.18um HV	0.18um HV	0.15um 6M standard	45/65nm 3D-Stacked	0.11um DBH Imaging
Fill Factor	%	70	70	26.5	31.3	19.6
Frame rate	Fps	10	10	7	-	-
Distance range	m	100	100	6000	150-430	96
Repeatability error(σ)	cm	< 10	14.2	< 50	15~47	75
Background Light	klux	80	70	In space	-	-
Scan		O	O	-	O	X

Table I shows a performance comparison of this work to state-of-the-art devices in CMOS technology. The most important thing in this table is that the proposed sensor to implement a scanless system. Other sensors have problems of low frame rate, high cost due to structural issues and low durability, while proposed sensors can solve these problems. However, this sensor has a lower resolution than other systems. Some sensors were able to achieve high resolution by consuming time with a small size system through a line sensor. In another case, high resolution can be achieved by increasing the chip area using a 3D-stacked process. In the case of a proposed sensor, the in-pixel histogram is larger than the conventional structure using other line sensors or event driving. Since proposed sensor implement large size technique, the sensor can benefit greatly from shrinking pixel size by changing process. In terms of frame rate rather than size, the proposed scanless sensor is expected to have a better specification than other sensors with 10 fps. A proposed sensor detecting 96 m range with 0.75 m precision was designed for coarse mid-range detection. This sensor will also have great immunity in background light. To overcome the problem of longer measurement time when SAR histograms for memoryless in-pixel histograms are used, I propose exponential photon counting by enhancing the spatiotemporal correlation of multi-SPADs.

SPAD-based sensors are basically vulnerable to background light noise and require a large number of measurements for histogram. In the future, a coarse detection that the proposed sensor can be used quickly finds the approximate location of the object and then reduces the time that SPAD can react through the window. Then, it is possible to detect a very accurate and fast fine signal after coarse detection. I have a plan to design a high performance SPAD-based LiDAR sensor that works well regardless of the background light intensity.

VII. Conclusion

This thesis proposes a 32 x 30 SPAD-based scanless LiDAR sensor with in-pixel histogram Array. The SPAD-based scanless LiDAR sensor was intended to make an array sensor and make a low cost solid-state scanless sensor. In the existing structure, huge memory for Histogram could not be made as an array sensor. To overcome this problem, I propose a SAR Histogram technique based on binary search covering all dynamic ranges with only two time bins. The sensor implemented a small size memoryless in-pixel histogram with this technique. Instead, the problem is that the frame rate must be lowered because the measurement time is lengthened as the number of STEP. To solve this fatal problem, I propose exponential photon counting to measure as many SPADs as spatiotemporal correlation using Multi-SPADs. This technique can quickly compensate for slower measurement times. In simulation result, SPAD# counting through multi-SPADs, I confirmed proper operation of exponential UP-DOWN counter. And the result is stored in memory and it is narrowed down to the window, and it is confirmed that the target distance can be detected properly. Designed SPAD-Based LiDAR sensor can measure distance of 96m with precision of 0.75m with coarse detection of long distance and implemented 30x32 array sensor through small size in-pixel histogram in 110nm DBH process. This makes it possible to realize a low cost solid-state LiDAR sensor.

In the future, I have a plan to design a high performance SPAD-based LiDAR sensor regardless of the background light with the proposed sensor which can detect coarse range in small size in-pixel histogram array.

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