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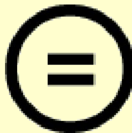

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Master's Thesis

Development of an On-chip Health Monitoring System for Solder Joints using Bit Error Rates

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Department of System Design and Control Engineering

Graduate School of UNIST

2018

ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

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A thesis
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Master of Science

Insun Shin

1.13.2018

Approved by

Advisor
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1.13.2018

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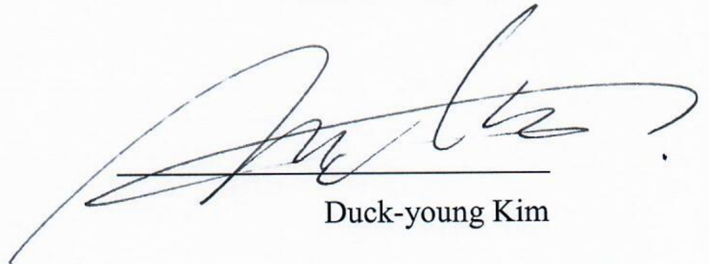

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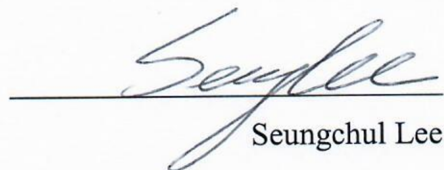

Seungchul Lee

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Abstract

Electronic systems are widely used as industrial network systems, control devices, and data acquisition devices that play an important role in automated production lines. Failures of electronic systems or components can lead to unexpected plant downtime, resulting in loss of productivity, direct labors for repairs, and delay in product and service development. maintenance strategies are tied into reliability-centered maintenance which optimizes the availability of the asset based on comprehensive maintenance infrastructure. One of key technologies associated with proactive maintenance is sensors and measurement technologies because it is necessary to collect sensor data for fault diagnosis and prognosis. These existing methods, however, often require external and additional sensing devices such as multimeters, oscilloscopes, and network analyzers, which can disturb system operation and eventually increase operating costs.

This study develops an on-chip monitoring system for non-destructive and non-invasive health monitoring of electric components and systems. BER which represents states of digital signals was selected to measure without external sensing devices. The monitoring system was developed using a digital transceiver toolkit. And solder joint corrosion test was conducted to collect the degradation data based on BER measurements and DC resistance. Features from BER measurement: eye width, eye height, eye size, and BER average were extracted and evaluated through statistical comparison based on Fisher's discriminant analysis that assesses the separation between normal and abnormal states. The normal and abnormal states were classified on basis of the conventional failure criteria of DC resistance. Eye size from BER showed the highest separation out of the feature sets. Times to failure derived using eye size was close to the times to failure based on the conservative failure criteria using DC resistance.

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I. Introduction

1.1 Background

Electronic systems are widely used as industrial network systems, control devices, and data acquisition devices that play an important role in automated production lines. Failures of electronic systems or components can lead to unexpected plant downtime, resulting in loss of productivity, direct labors for repairs, and delay in product and service development [1]. Figure 1 shows impacts of unexpected downtime caused by equipment failures. According to [2], one of the major losses at manufacturing plants is unexpected downtime of 2.64hours due to equipment failures. As a result of unexpected outages, manufacturing plants eventually lose millions of dollars. For example [3], one of the world's largest automotive parts manufacturers spent 1.3 million dollars an hour due to unexpected downtime in manufacturing facilities. Therefore, timely maintenance of electronic systems is necessary for preventing loss of revenue from unexpected downtime by manufacturing system failures.

Maintenance strategies have developed to be more proactive and optimized for increasing the availability of manufacturing facilities while making maintenances economical. Figure 2 (a) shows maintenance strategies [4] which is from reactive maintenance to reliability-centered maintenance. Reactive maintenance is maintenance which is letting a specific asset run to fail and repairing after breakdown. Reactive maintenance can be conducted when failures of the asset do not affect overall production process and costs for proactive maintenance is larger than benefits of preventing failures. Preventive maintenance is conducting regular maintenance action by periodic inspection and repairs. Condition-based maintenance is more proactive maintenance by monitoring performance and

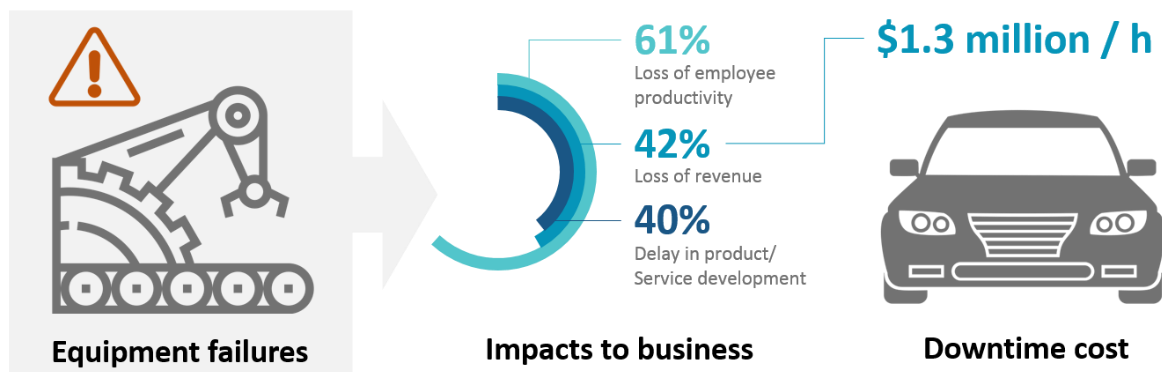

Figure 1 Impacts of unexpected downtime caused by equipment failures [1][3]

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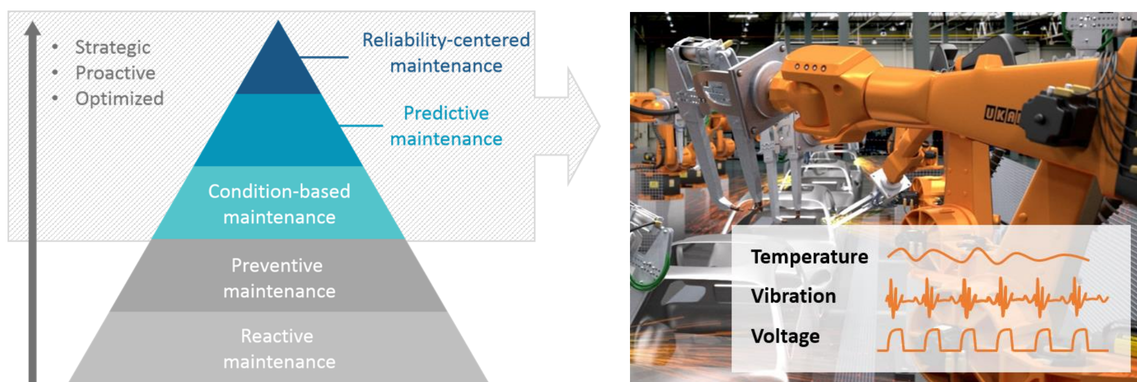
environmental conditions of the asset. And condition-based maintenance tries to maintain the asset by preventing failures or repairing at the right time through analyzing condition data based on algorithmic logics. Predictive maintenance is maintenance before failures under understanding of impending failure issues and expected lifetime before failures of an asset through combination of physics of failures and artificial intelligence technologies. Finally, maintenance strategies are tied into reliability-centered maintenance which optimizes the availability of the asset based on comprehensive maintenance infrastructure.

1.2 Motivation and Problem Statement

One of key technologies associated with proactive maintenance is sensor and measurement technologies because it is necessary to collect sensor data for fault diagnosis and prognosis, as shown in Figure 2 (b). And many researchers have studied to develop monitoring technologies based on the representative measurement techniques. The representative measurement techniques are based on electrical parameters, time domain reflectometry, and S-parameter.

Gershman and Bernstein [5] suggested a quantitative measurement tool based on serial ohmic resistance changes in solder joints. The serial ohmic resistance was applied to monitor crack propagation of solder joints in quad flat non-leaded (QFN) package. The results showed that the serial ohmic resistance increased the growth of crack length and the suggested method can be used as a prognostic tool to predict remaining useful life of QFN packages. Ji et al. [6] developed a condition monitoring method for insulated-gate bipolar transistor power modules using voltage measurement. The authors designed the additional measurement circuitry in the monitoring system



(a) Maintenance strategies [4] (b) Measurement of device health

Figure 2 Maintenance strategies and measurement of device health

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for voltage measurement.

Wang et al. [7] used joint time-frequency domain reflectometry (JTFDR) for monitoring premature failures of power cables. JTFDR was measured in a thermal accelerated aging test of power cables including cross-linked polyethylene, ethylene propylene rubber, and silicone rubber. The results showed that the JTFDR time-frequency cross correlation peak increased during the aging test and JTFDR techniques has a potential to monitor the cable status continuously.

Okoro et al. [8] used a vector network analyzer (VNA) to measure S- parameter of through-silicon via (TSV) stacked dies. Using the radio frequency (RF) based measurement technique, the authors assessed the effect of thermal cycling on the reliability of the TSV daisy chain. The results showed the RF signal of the TSV daisy chain degraded with the number of thermal cycles and RF-based measurement techniques could be a metrology tool for the reliability of TSV stacked dies.

These existing methods, however, often require external and additional sensing devices such as multimeters, oscilloscopes, and VNA, which can disturb system operation and eventually increase operating costs. For example, when measuring resistance of a component by using a multimeter, the component should be disconnected from any circuit and power sources for accurate measurement. Otherwise, it is required to use an additional oscilloscope to measure TDR. As a result, the operation of the electronic circuit is interrupted, and eventually operating time and costs increase. Therefore, non-destructive and non-invasive monitoring techniques without external and additional sensing devices are required to reduce monitoring time and costs for fault diagnosis and prognosis.

1.3 Objectives

This study develops an on-chip monitoring system for non-destructive and non-invasive health monitoring of electric components and systems. On-chip monitoring techniques are measurement circuitry techniques included in the same integrated circuit as a given device. A digital signal transceiver system consists of a transmitter, a communication channel, and a receiver. In an on-chip monitoring system, health monitoring can be performed using existing components without additional and external devices. For example, the receiver can conduct health monitoring of the digital signal transceiver system with the existing function to receive digital signals. Using an on-chip monitoring system would reduce time and costs to monitor health of electronic systems for fault diagnosis and prognosis.

The on-chip monitoring system was developed using a new monitoring parameter based on digital signal characteristics. BER which represents the number of error bits generated depending

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on states of digital signals was selected to measure digital signal quality. Using the developed monitoring system, BER was measured under an accelerated life test of solder joints for verifying that the parameter can be used to measure the health of an electronic component. An existing measurement technique, resistance measurement using a datalogger, was also used to assess whether the new monitoring parameter can replace the existing measurement for monitoring health of solder joints. Finally, faults of solder joints were detected using a feature from the monitoring parameter.

This thesis is organized as follows. Digital signal characteristics are introduced to present how BER was determined to be measured in Section 2. The monitoring system using BER is explained in Section 3. Experimental methodology including the accelerated life test, feature extraction, fault diagnosis are described in Section 4. The analytical results from the experiment are discussed in Section 5, followed by the conclusions in Section 6.

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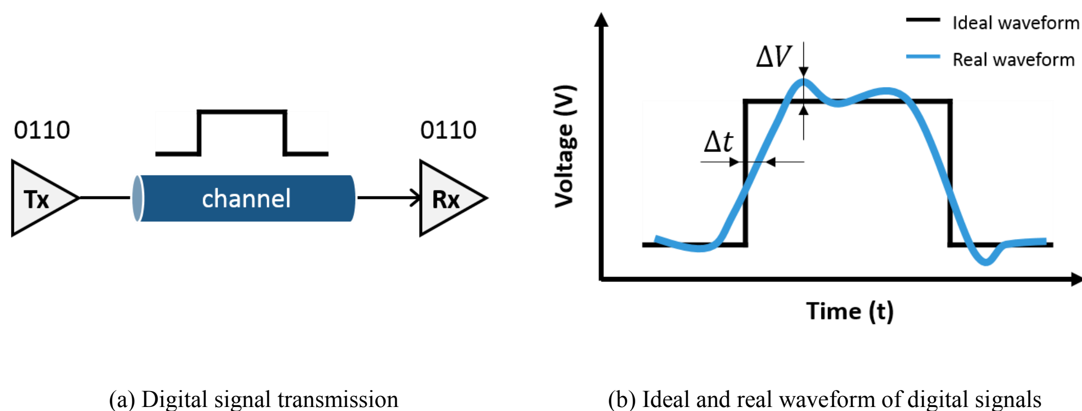
II. Digital Signal Characteristics

Electronics often operate on digital signals which are a series of discrete pulses representing 1 bits and 0 bits. Because digital signals have advantages relative to analog signals [5][8], digital signal transmission is widely used in communicating and computing systems. Digital signals have high network capacity because multiplexers enable multiple conversations to share a communications channel, and hence can achieve efficient transmission systems. And power requirement is low because only two discrete pulses are needed to be transmitted. Furthermore, digital data offer better security relative to analog signals because an encryption algorithm can be used on digital information.

Digital signal characteristics and ideas for the monitoring system are introduced in this section. This section is organized with digital signal quality, issues on digital signal quality, and ideas for the on-chip monitoring system.

2.1 Digital Signal Quality

The transmission of digital signals is through a medium or a channel which is usually wire-bond connection and interconnects in electronics. Figure 3 (a) shows a transmission system of digital signals consisting for a transmitter, a receiver, and a channel. Although digital signals are a sequence of discrete pulses, noise is always generated and added to ideal digital signals, as shown in Figure 3 (b), because the signals are fundamentally analog pulses.



(a) Digital signal transmission (b) Ideal and real waveform of digital signals

Figure 3 Transmission and waveforms of digital signals

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The deviation of a noisy signal from the ideal can be viewed from two aspects; timing deviation (Δt) and amplitude deviation (ΔV) [10]. The timing deviation is defined as timing jitter and the amplitude deviation is defined as amplitude noise. The impacts of timing jitter and amplitude noise is independent. Timing jitter affects performance of a transmission system only at edges of signal transitions (i.e. at changes from 0 to 1 or changes from 1 to 0). On the other hand, amplitude noise which is a constant function can affect system performance all the transmission time.

Signal integrity (SI) is a set of measures of the quality of digital signals involving timing jitter and amplitude noise. SI analysis evaluates whether the signal reaches its receiver as scheduled and the signal has valid logic levels in a broad sense. Likewise, a digital signal with good signal integrity has fast transitions, valid logic levels, and accurate placement in time [11]. Representative measurement techniques for SI analysis are TDR, eye diagram, and they can measure digital signal quality related to termination, crosstalk, loading effects, etc. The purpose of SI analysis is to verify stable high-speed data transmission [14]. SI analysis is widely used at all steps of electronics packaging and assembly to evaluate electrical performance of internal connections in an integrated circuit (IC), a printed circuit board (PCB), a backplane, and inter-system connections.

2.2 Issues on Digital Signal Quality

Customers continually demand higher speed digital systems with reduced power requirements. The amount of data transmission and digital signal processing has been growing, and its processing speed has been required to be faster for high quality graphics, high-quality audio, and fast-streaming video. For example, personal computers are hardly a typing tool anymore, today they drive 3D games and computer-aided design programs [11]. Additionally, cell phones are required to drive videography, 3D games, and navigation with limited power sources. Numerous computer application technologies are pushing advancements of data rate and transmission power.

In the early 2000s, these demands in a world of big data sparked a drastic shift from parallel to high-speed serial digital communication buses [15]. The serial digital communication buses have led to digital systems with much higher data throughput and lower power requirements. High-speed serial buses send encoded data that contains both data and clocking information in a single differential signals, so the high-speed serial links today reach at 10Gbps commonly. Furthermore, multiple lanes of bus links can be coherently in serial communications, and the number of pin counts in in integrated circuits (ICs) can be reduced. Figure 4 shows the number of lanes and data rates of representative parallel and serial bus standards.

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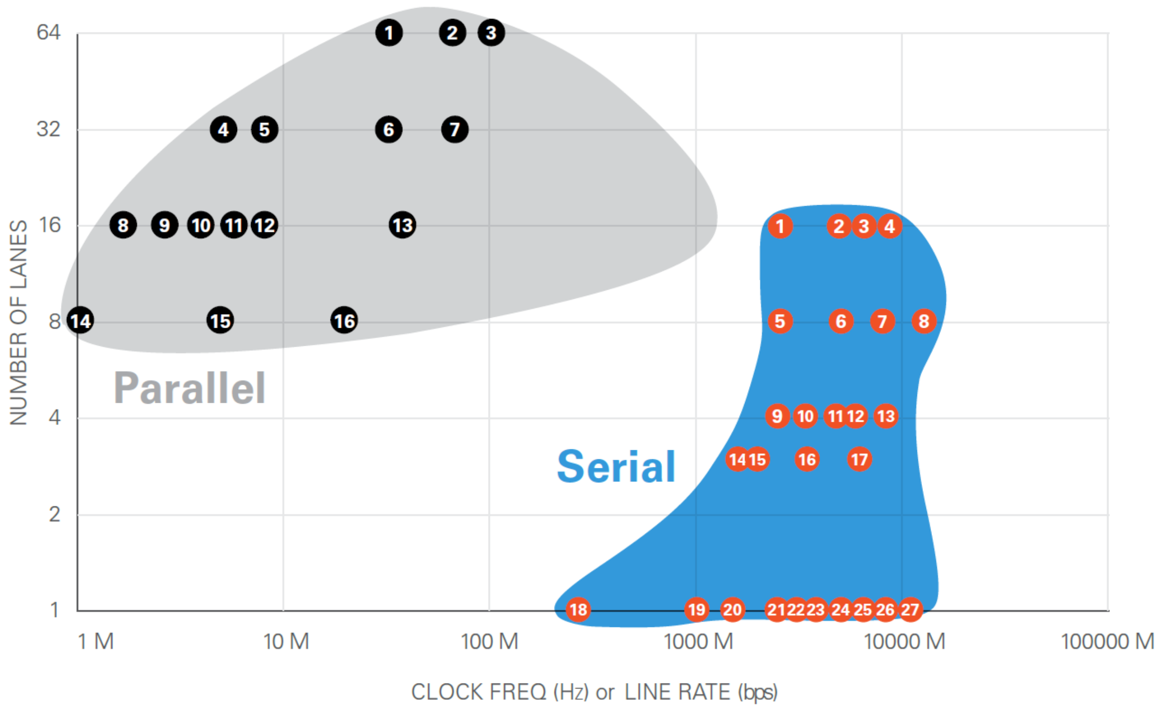
The faster data rates, however, required present additional design challenges. To achieve this improvement, edge speeds (i.e., rise time) today are now a hundred times faster than before. Rise time of a digital signal can carry much higher frequency components than its repetition rate might



Parallel Bus

1. PCI 64-bit/33 MHz
2. PCI 64-bit/66 MHz
3. PCI 64-bit/100 MHz
4. Front Panel Data Port
5. EISA
6. PCI 32-bit/33 MHz
7. PCI 32-bit/66 MHz
8. IDE (ATA PIO 0)
9. ATA PIO 1
10. ATA PIO 2
11. ATA PIO 3
12. ATA PIO 3
ISA 16-bit/8.33 MHz
13. Ultra-2 wide SCSI
14. RapidIO Gen1.1
15. GPIB
16. SCSI
ISA 8-bit/4.77 MHz

Serial Bus

1. PCIe Gen1x16
2. PCIe Gen2x16
3. Serial RapidIO Gen2
4. PCIe Gen3x16
5. PCIe Gen1x8
6. PCIe Gen2x8
7. PCIe Gen3x8
8. JESD204B
9. PCIe Gen1x4
10. Serial RapidIO Gen1.3
11. PCIe Gen2x4
12. DisplayPort
13. PCIe Gen3x4
14. HDMI 1.0
DVI
15. HDMI 1.3
16. HDMI 2.0
17. SD-SDI
18. Gigabit Ethernet
19. SATA 1.0
20. Serial FPDP
PCIe Gen1x1
21. SATA 2.0
3G-SDI
JESD204A
10G Ethernet
22. PCIe Gen2x1
USB 3.0
23. SATA 3.0
24. PCIe Gen3x1
25. USB 3.1

Figure 4 The number of lanes and data rates of representative parallel and serial bus standards [15]

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imply. It's actually the higher frequency components that create the desired fast transitions in a digital signal. Signal integrity problems increase at high frequencies. Transmission line effects are critical. Impedance discontinuities along the signal path create reflections, which degrade signal edges. Faster edge speeds generally also require higher currents to produce them. Higher currents tend to cause ground bounce, especially on wide buses in which many signals switch at once. Also, higher current increases the amount of radiated magnetic energy and, with it, crosstalk.

An ideal digital pulse is cohesive in time and amplitude, is free from deviations and jitter, and has fast, clean transitions. As system speeds increase it becomes increasingly more difficult to maintain ideal signal characteristics, requiring careful consideration of signal integrity issues. Therefore, signal integrity should be monitored for ensuring electronic devices.

2.3 Ideas for an On-chip Monitoring System

An on-chip monitoring system can be established by measuring existing parameters. Digital signals can serve as a monitoring means of detecting solder joint degradation based on skin effect [12],[13]. Skin effect is a phenomenon that the high frequency signal concentrate to the surface of the conductors, aging of solder joints such as crack propagation. Based on skin effect, aging of solder joints finally induce loss of digital signals.

According to [12], Yoon et al. presented a diagnosis method for solder joints by monitoring eye diagram parameters which indicate signal integrity. Eye diagram parameters were collected under the solder joint degradation test. As a result, jitter showed significant deviation with aging of solder joints in the thermo-mechanical stress. The authors suggested continuous monitoring of digital signal parameters including jitter for a non-destructive diagnosis method. Lee and Kwon [13] constructed a health monitoring system based on eye diagram parameter measurement. Eye height extracted from eye diagram showed gradual degradation under an accelerated life test of solder joints and the authors used eye height for anomaly detection of the solder joint. The times to failure of solder joints using eye height was faster than that using DC resistance. It indicated that eye diagram parameters can be used for detecting interconnect damage in diagnosis system. Those related studies imply that the digital signal characteristics can be a measure for fault diagnosis of electronic components that operate with digital signal.

There is a method to measure digital signal quality without any external measurement equipment; bit error rate (BER) that is determined depending on the digital signal quality and can be measured without external sensing devices. BER is the number of error bits relative to the total number of bits

received over a data communication channel. In a digital transmission, error bits are generated when incoming digital signals do not satisfy the bit decision criteria of a receiver because digital signals are affected to noise, distortion, and loss of digital signals by damaged transmission channel. BER is widely used to describe the overall performance of a communication channel by the rate of error bits because a channel transmits and receives giga bits for a second.

Figure 5 shows an example of bit errors within a communication channel. As shown in the figure, assume the transmitted bit sequence is 0111010010 and the following received bit sequence is 0111000110. In this case, the number of bit errors is 2 and the BER is 0.2 or 20%.

Accordingly, this study develops an on-chip monitoring system for non-destructive and non-invasive health monitoring of solder joints using BER. There are two main this performed in this study. The first one is development of a monitoring system using BER. The second is experimental verification of the monitoring system based on accelerated life tests of solder joints.

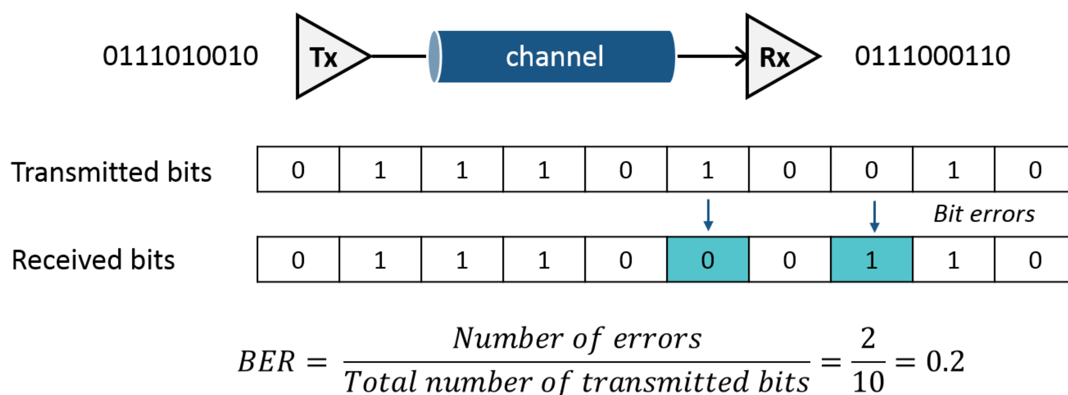

Figure 5 Bit error rate

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III. Development of a Monitoring System using BER

This section focuses on the development of a monitoring system using BER. Bit error mechanisms has been expressed first with descriptions to address how do jitter and noise impact the BER. Finally, the monitoring method of the system will be described.

3.1 Bit Error Mechanisms

Bits are classified based on a sampling point of the channel receiver. Figure 6 (a) shows an example of data transmission of a synchronous bus. A receiver samples transmitted data in keeping time with clock. The clock determines a sampling time of t_s. At the sampling time, the receiver classifies incoming bits whether it is 0 or 1 by a threshold voltage V_s. Figure 6 (b) shows a sampling point of a receiver and how the receiver determines bits. The receiver recognizes bit 1 if the signal voltage is over the threshold voltage, or bit 0 if the signal voltage is lower than the threshold voltage. the receiver recognizes bit 1.

In the presence of jitter and noise, the rising and falling edges of signals can move along the time axis, and the voltage level can move along the amplitude axis. Figure 7 shows examples of bit error generation due to jitter, noise, and signal loss. As such, the correct bit detection conditions for sampling time and voltage may not be satisfied, resulting in a bit error due to bit 1being detected as bit 0. The violations of sampling conditions can occur in three scenarios [16]:

1) The crossing time of the rising edge lags behind the sampling time, $t_r > t_s$
2) The crossing time of the falling edge is ahead of the sampling time, or $t_f < t_s$
3) The logical 1 voltage is below the sampling voltage, or $V_1 < V_s$

where t_r is the rise time, t_f is the fall time, and V_1 is the voltage of bit 1. For a bit 9 detection, the correction detection condition becomes $t_r < t_s < t_f$ and $V_0 < V_s$. Similarly, the violation of correct sampling condition causes a bit error because bit 0 is received as bit 1. The violation scenarios are opposed to the correction detection condition.

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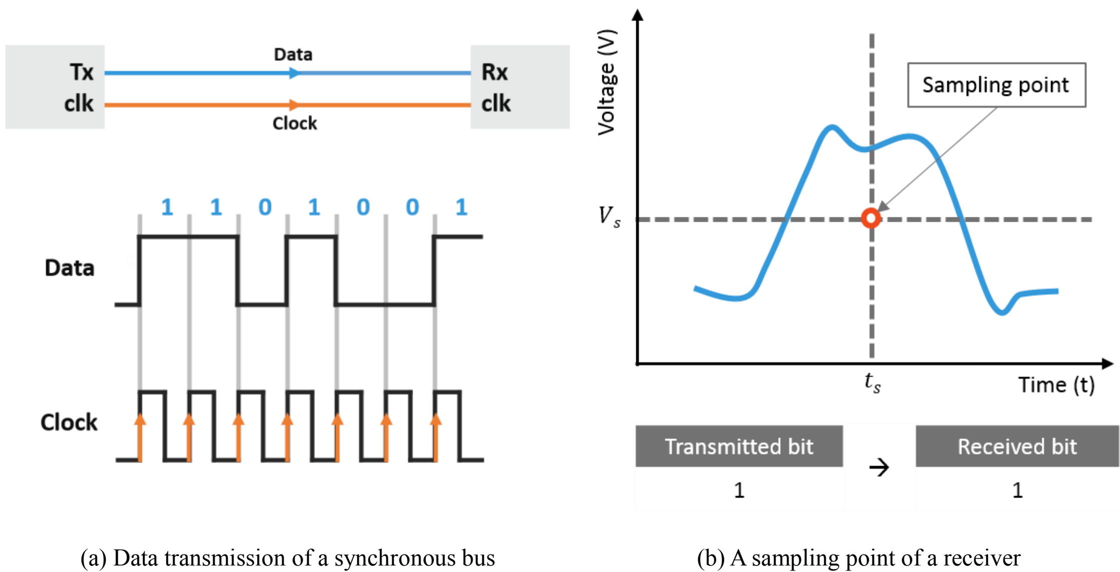
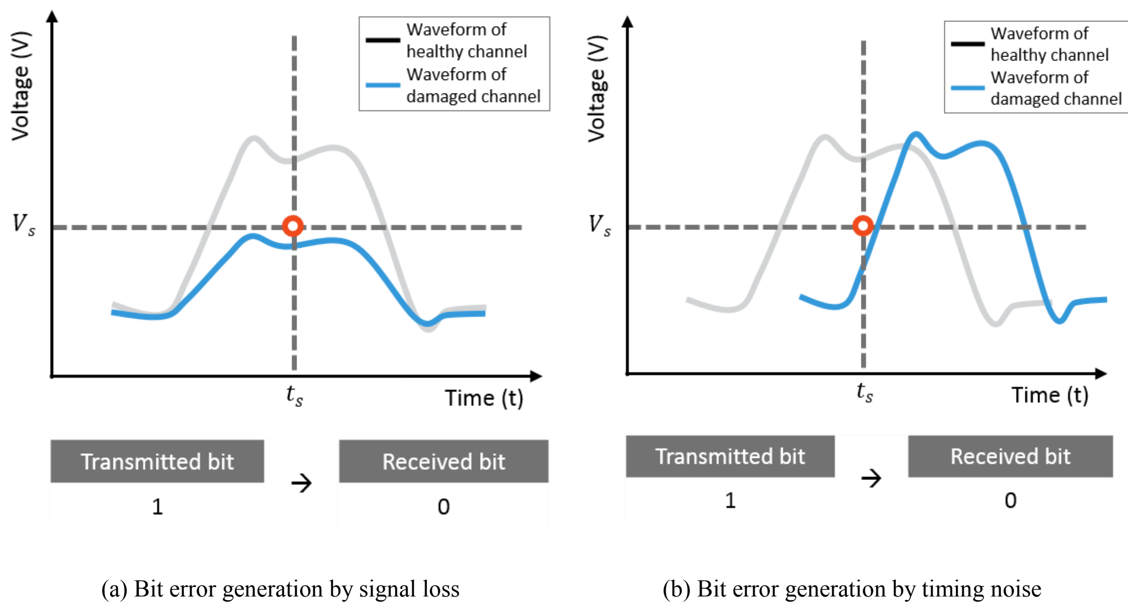
3.2 A Monitoring System using Bit Error Rates

A monitoring system using bit error rate was developed based on the bit detection mechanism. In order to monitor the gradual degradation of digital signals, sampling points was moved across an entire input unit interval of digital signals, and violation of bit detection was induced along to the



(a) Data transmission of a synchronous bus (b) A sampling point of a receiver

Figure 6 A sampling point of a receiver where V_s and t_s are the threshold voltage and the samples time, respectively



(a) Bit error generation by signal loss (b) Bit error generation by timing noise

Figure 7 Bit error generation scenarios due to signal loss and timing noise

waveform. Figure 8 shows sampling points of the developed monitoring system by moving the sampling times and the threshold voltages. Circuitry generates 32 horizontal and 127 vertical sampling points within a unit interval of received input. The sampling times moved from t_0 to t_{63}, and the threshold voltage moved from V_0 to V_{126}. Finally, the number of sampling points was 4064. BER was measured at all sampling points and eventually was built as a matrix, as shown a matrix (1).

$$\begin{bmatrix} BER_{0,126} & BER_{1,126} & BER_{2,126} & \cdots & BER_{31,126} \\ & \vdots & & \ddots & \vdots \\ BER_{0,2} & BER_{1,2} & BER_{2,2} & & BER_{31,2} \\ BER_{0,1} & BER_{1,1} & BER_{2,1} & \cdots & BER_{31,1} \\ BER_{0,0} & BER_{1,0} & BER_{2,0} & & BER_{31,0} \end{bmatrix} \quad (1)$$

where $BER_{a,b}$ is the BER at a sampling point when the sampling time is t_a and the threshold voltage is V_b. The BER matrix was measured to monitor the quality of the received data. Clearly BER matrix depends on data rate, jitter, and noise in the communication system.

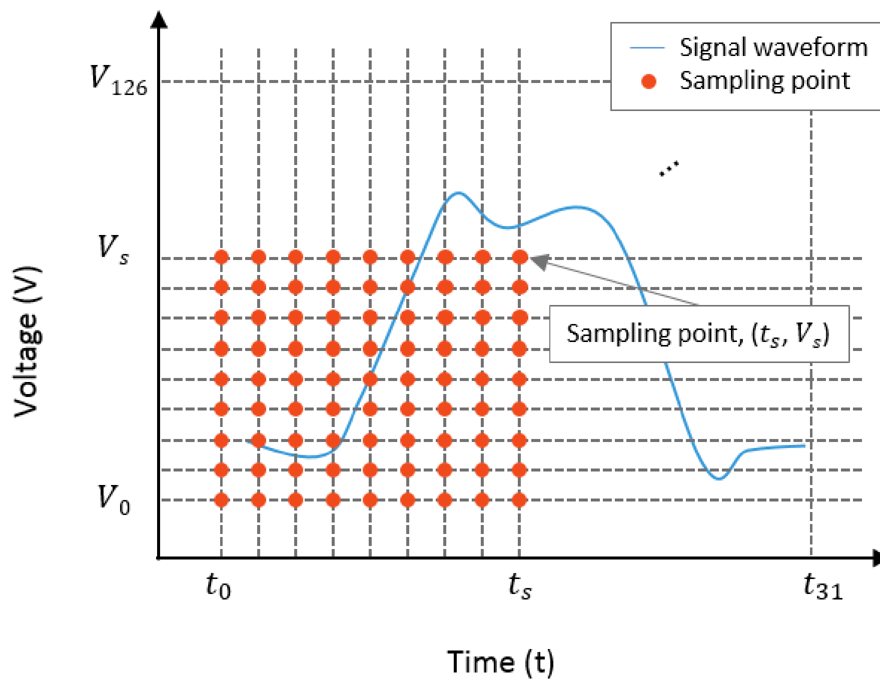


Figure 8 BER sampling points of the monitoring system

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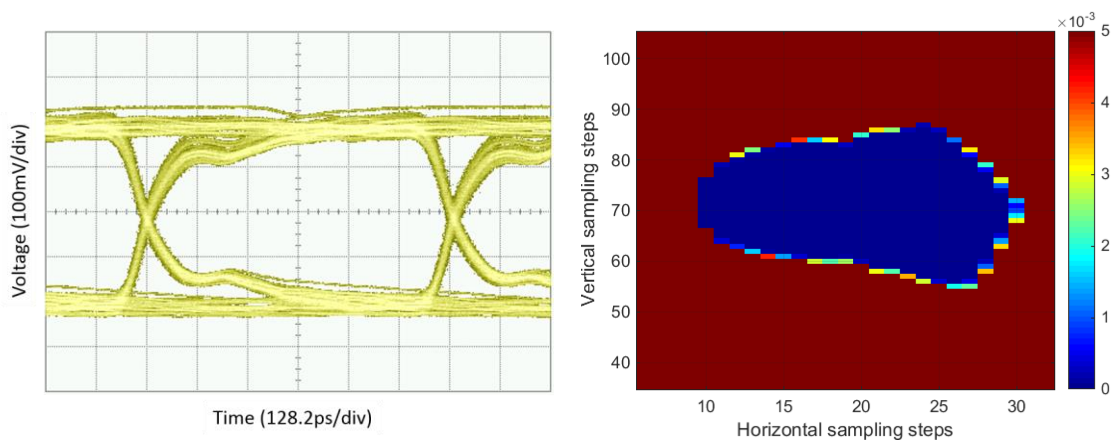
In order to measure the BER matrix, Bit-error rate test (BERT) function with pseudo-random binary sequence (PRBS) pattern generator and checker was used to develop the health monitoring system. EyeQ in Altera Stratix V, which has BERT function, is widely used for signal integrity test because it analyzes the received data recovery path, including the receiver's gain, noise level, and recovery clock jitter. But it has been not applied to monitor continuous degradation states of electronic components. By tcl script programming, BER was measured continuously for monitoring degradation states.

Figure 9 shows the real waveform of digital signals measured by eye diagram and the digital signal form measured by BER of a healthy solder joint. The digital signal form by BER showed a distorted circle which is similar the eye opening of the real signal waveform. It is because that EyeQ uses a phase interpolator (PI) and sampler (SMP) to estimate the horizontal eye opening. Controlled by a logic generator, the PI generates a sampling clock and the SMP samples the data from the receiver output. The SMP outputs parallel data that is monitored for BER errors. When the PI output clock phase is shifted by small increments, the data error rate goes from high to low if the receiver is good.



(a) Real waveform of digital signals (b) The digital signal form measured by BER

Figure 9 Real waveform of digital signals and the digital signal form measured by BER

IV. Experimental Verification

This section focuses on the experimental verification of the monitoring system based on accelerated life tests of solder joints. This study conducted the accelerated life test and fault diagnosis of solder joints to demonstrate whether the BER measurements can detect solder joint degradation prior to interconnect failures and the BER can be features for monitoring the health of solder joints. Figure 10 shows the process of the experiment. In the first step, solder joints were tested to collect degradation data under stress conditions in the accelerated life test. Second, features were extracted from the BER matrix. And features were evaluated based on a statistical comparison method. Finally, a feature showing states of solder joints most clearly were used to detect the failure of solder joints.

4.1 Accelerated Life Test

The purpose of the accelerated life test was to induce failures of solder joints and to collect the degradation data using the health monitoring system. The accelerated life test provides real experimental data that characterize the degradation of the solder joints. The accelerated life test consisted of four parts; determination of stress conditions, determination of measurement parameters, experimental setup, and experiment and data collection.

Chemical stress was induced for generating failures of the solder joint. The solder joints were exposed under the fume of 10M from 0.05ml nitric acid solution. Corrosion of the solder joints was

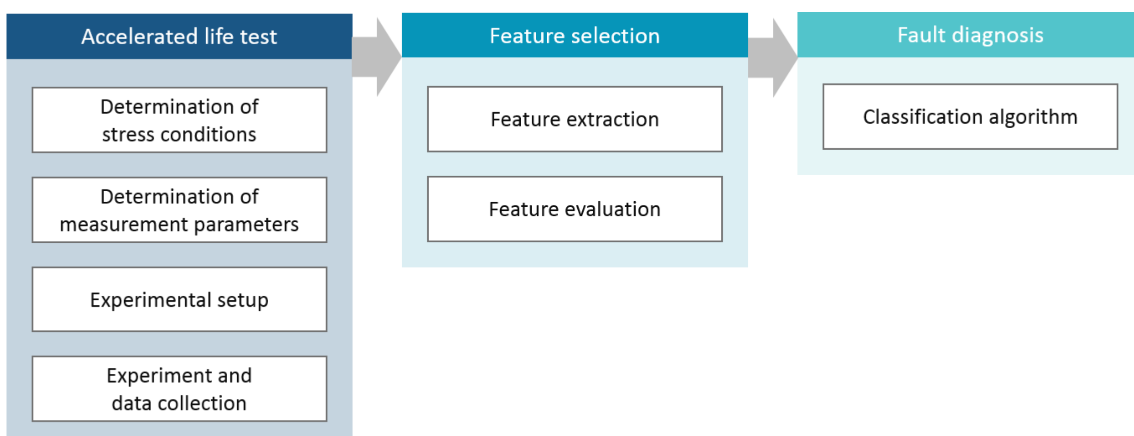


Figure 10 Process of the monitoring system experiment

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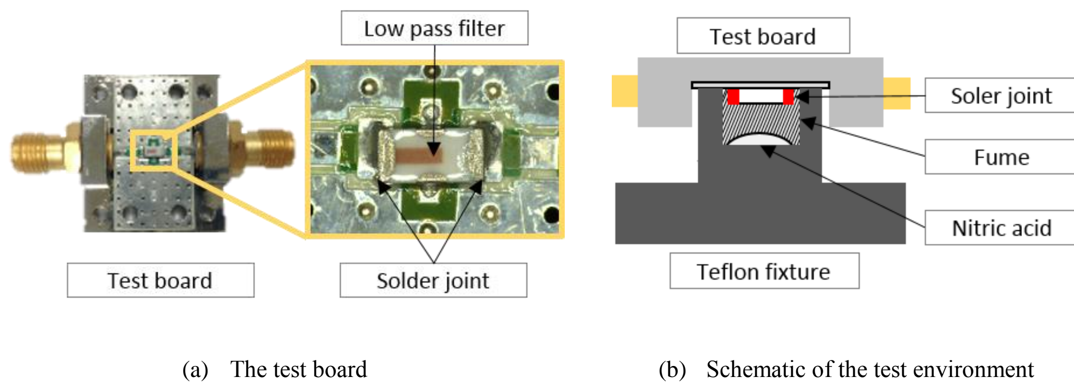
progressed by the acid atmosphere continuously. The device under test (DUT) used in the experiment was a controlled impedance test board where a low pass filter component is soldered to transmit digital signals, as shown in Figure 11 (a). SAC305 solder alloy was used to solder the low pass filter to the test board. A Teflon fixture was produced in order to expose the fume to the solder joints not to other interconnects and ground pass. Figure 11 (b) shows the schematic of the test environment. The solder joints were enclosed with the Teflon fixture, and the nitric fume affected to the low pass filter and the solder joints. Total 3 test boards were used in the accelerated life test.

DC resistance was measured to examine failure sensing capability of BER measurements because a common approach to reliability testing is to monitor electrical resistance DC resistance [17]. There are four international standards are currently in use by the electronics industry to specify solder joint failure criteria during reliability and qualification tests; IPC-SM-785 [18], IPC-9701 [19], JESD22-



(a) The test board (b) Schematic of the test environment

Figure 11 The DUT test board and schematic of the test environment [13]

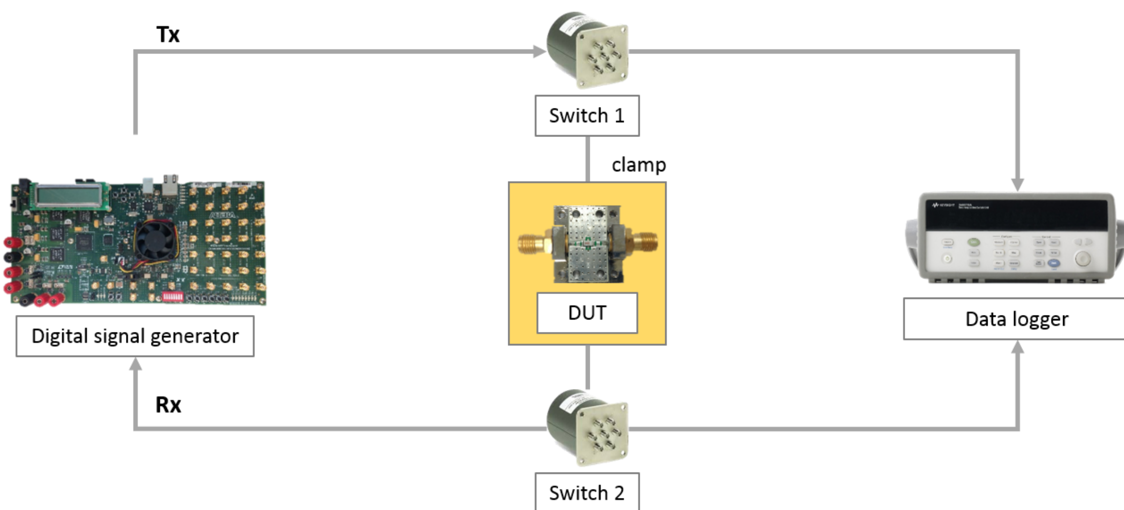


Figure 12 Schematic of the accelerated life test

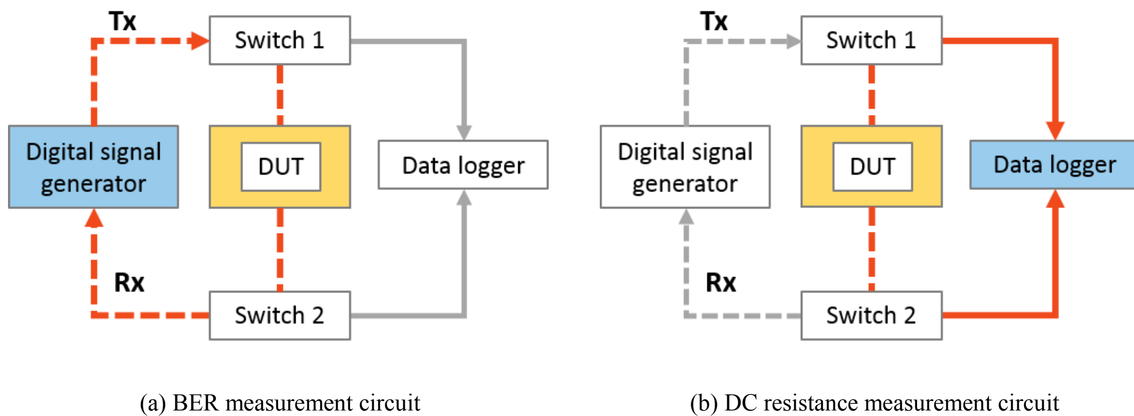
B111 [20], and IPC/JEDEC-9702 [21]. DC resistance commonly showed abrupt changes at time to failure.

Figure 12 show the schematic of the accelerated life test setup that consists of a digital signal generator, the DUT, a data logger, and switches. An Altera Stratix V GX was used to generate PRBS7 (Pseudo-random Binary Sequence) digital signals with a speed of 1.25Gbps. The PRBS7 digital signals was conveyed to the DUT through a switch. During the test, 4-wire DC resistance of the test board was monitored using a Keysight 34970a datalogger.

BER and 4-wire DC resistance were measured by turns, and the measurement circuit was composed by switches. Figure 13 shows the measurement circuits. In the figures, dotted lines express the PRBS7 signal pass. Orange lines present the used wire at the moment of measurement and blue box means the used equipment for generating digital signals and the measurement. BER measurement circuit needs only one equipment, the digital signal generator, that generates signals with measuring BER. 4-wire DC resistance measurement circuit only needed the data logger, but the digital signal pass was destructive. It means the monitoring technique cannot be conducted during system operation and online measurement. The measurement circuits were created sequentially by controlling the switches. The measurement was repeated every about 2 mins.

4.2 Feature Selection

Feature selection was performed to select subsets of relevant features which are extracted from BER measurements for health monitoring and fault diagnosis of solder joints. The feature sets from



(a) BER measurement circuit (b) DC resistance measurement circuit

Figure 13 Schematic of measurement circuits for the monitoring parameters

BER were evaluated using a statistical comparison.

4.2.1 Feature Extraction

Feature sets were extracted based from BER matrix (1) for reducing the dimension of datasets. There are four features from BER matrix. Figure 14 and Table 1 shows the feature set description. Normally, the number of sampling time steps and threshold voltage steps of valid data, which of BER is lower than 10^{-17}, is defined as the eye width and eye height, respectively. Thus, eye width and eye height from BER measurement are designated as eye width and height of BER. The novel feature sets are eye size and BER average.

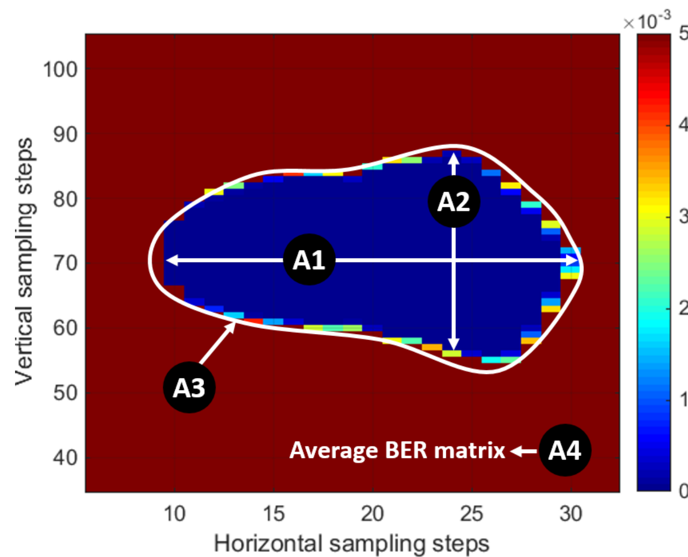


Figure 14 Feature sets based on the BER matrix

Table 1 Feature set description

No.	Feature	Description
A1	Eye width	The number of sampling time steps where BER is lower than 10^{-17}
A2	Eye height	The number of threshold voltage steps where BER is lower than 10^{-17}
A3	Eye size	The number of BER sampling points where BER is lower than 10^{-17}
A4	BER average	Average of BER matrix

4.2.2 Feature Evaluation

In order to evaluate whether the extracted feature sets validate to detect the solder joint failures, the distribution of the feature sets was assessed based on the solder joint states. The solder joint states were classified on basis of the existing failure criteria for solder joints. After that, mean and variance of the feature sets in normal and abnormal states were used to the feature selection.

To define the failure events from the monitored degradation data, existing failure criteria for solder joints were used. The failure criteria of solder joints are traditionally defined on the basis of three key characteristics of solder joint failure in IPC-9701 [19] and JEDEC-9702 [20]: the magnitude of the resistance increase due to loss of electrical continuity, the duration of interruption of electrical continuity, and the frequency of occurrence of interruptions. Figure15 shows the schematic of the failure criteria of solder joints. The detailed descriptions of key characteristics are follows:

1) Magnitude: the magnitude of the resistance increases due to loss of electrical continuity. An increase of 20% of the initial resistance value for six or more consecutive readings is a failure characteristic.

2) Duration: The resistance keeps the increment during more than 1us.

3) Frequency: The frequency of interruption occurrence by resistance increase should be 9 or more within an additional 10% of the cyclic life.

Based on the failure criteria using DC resistance, the failure of solder joints was defined. And then the time series data of solder joint degradation were classified into the normal and abnormal conditions.

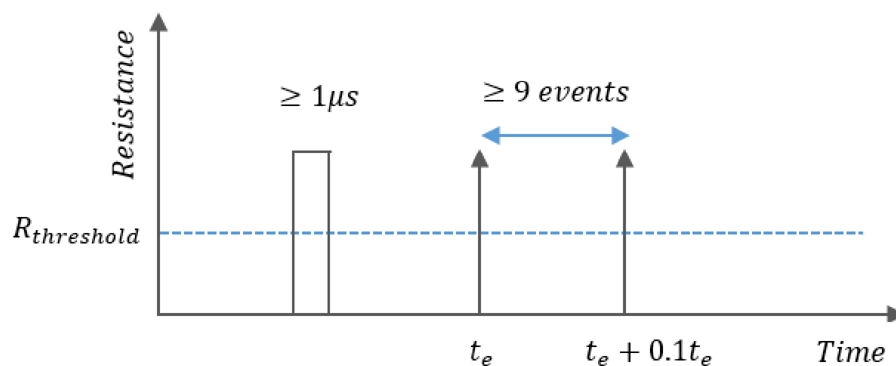


Figure 15 Failure criteria of solder joints

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Feature sets was evaluated and selected using the separation based on Fisher's linear discriminant. Fisher's linear discriminant doesn't make the assumptions about classes such as normal distribution or equal covariances. Fisher's linear discriminant is based on the idea that when features have maximum distance between classes and minimum variance within each class, classification using the features is clear.

Suppose two classes (0,1) of observations have means $\vec{\mu}_0$, $\vec{\mu}_1$and covariances σ_0^2, σ_1^2. Then the linear combination of features $\vec{\omega} \cdot \vec{x}$ will have means $\vec{\omega} \cdot \vec{\mu}_i$ and variances $\vec{\omega}^T \sigma_i^2 \vec{\omega}$, for $i = 0, 1$. Note that the vector $\vec{x}$ is the observations and $\vec{\omega}$ is the normal to the discriminant hyperplane. Fisher [23] defined the separation (S) between these two distributions to be the ratio of the variance between the classes to the variance within the classes:

$$S = \frac{\sigma_{between}^2}{\sigma_{within}^2} = \frac{(\vec{\omega} \cdot \vec{\mu}_1 - \vec{\omega} \cdot \vec{\mu}_0)^2}{\vec{\omega}^T \sigma_1^2 \vec{\omega}, + \vec{\omega}^T \sigma_0^2 \vec{\omega},} = \frac{\left(\vec{\omega} \cdot (\vec{\mu}_1 - \vec{\mu}_0)\right)^2}{\vec{\omega}^T (\sigma_0^2 + \sigma_1^2) \vec{\omega}} \quad (2)$$

This measure is a measure of the signal-to-noise ratio for the class labelling. It can be shown that the maximum separation occurs when

$$\vec{\omega} \propto (\sigma_0^2 + \sigma_1^2)^{-1} (\vec{\mu}_1 - \vec{\mu}_0) \quad (3)$$

In a two-dimensional problem, the line that best divides the two groups is perpendicular to $\vec{\omega}$. In this study, a separation index was used instead of $\vec{\omega}$ in order to rank the feature sets, not find the normal to the discriminant hyperplane. Because this study focuses the feature selection to find the sensor methodology for fault diagnosis or fault prognosis, not finding a new projected dimension for reduction the number of features, equation for assessing the class separation was only used. The separation index (I) was defined in common with $\vec{\omega}$ to find the best feature sets showing maximally separated means and minimized variance of each class. The separation index is shown in equation (4).

$$I = (\sigma_0^2 + \sigma_1^2)^{-1} (\vec{\mu}_1 - \vec{\mu}_0) \quad (4)$$

Feature sets having high separation index were used to detect faults of solder joints.

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4.3 Fault Diagnosis

Fault diagnosis is to detect faults or abnormal conditions of systems and to identify components that could potentially cause system failures [24]. Thus, fault diagnosis is classified into two categories: fault detection and fault isolation. In this study, fault detection was performed using the selected features sets to verify that the extracted and evaluated features can be used to be feature sets for detecting abnormal states of electronic components.

Fault detection was conducted using the threshold criteria of DC resistance. To apply the same criteria with resistance, an increase of 20% of the initial value was determined to be the failure criteria.

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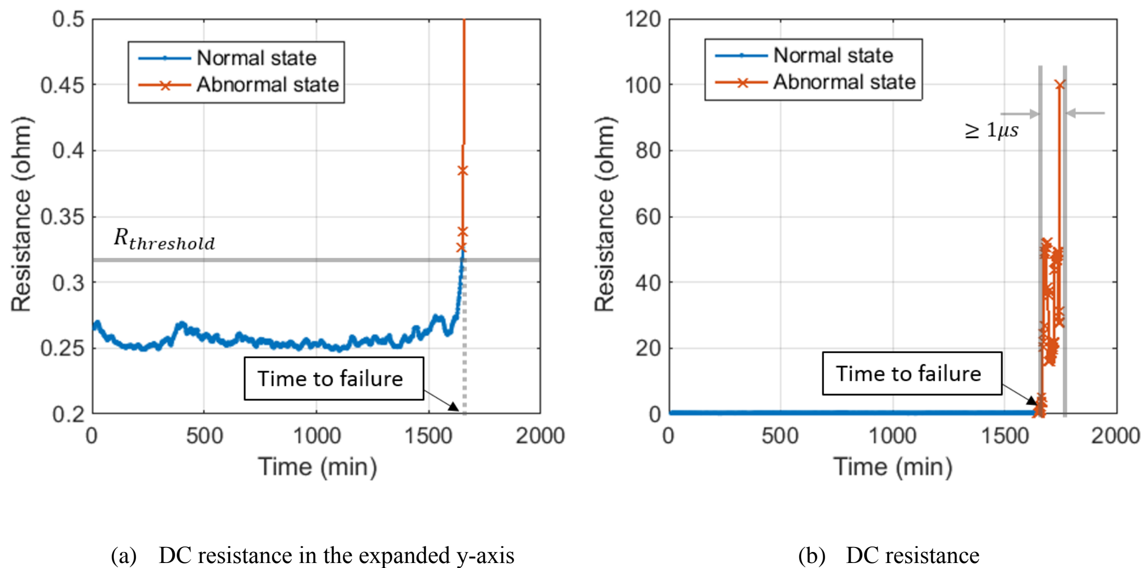
V. Experimental Results

This section shows the experimental results of the accelerated life test, feature selection, and fault diagnosis. Times to failure of the solder joints are given firstly, and then normal and abnormal states are classified based on the failure times. Second, a feature was selected based on the statistical feature evaluation. Fault detection using the feature will be also explained finally.

5.1 Time to Failure of the Solder Joint

Time to failure of the solder joints in the first test sample was 1650 mins based on the failure criteria using DC resistance. Figure 16 shows the DC resistance and time to failure of a test sample. The consecutive readings that were measured by data logger was average 0.27ohm and the threshold resistance that increase of 20% of the initial resistance value for six or more readings was 0.32ohm. At 1650 mins, the resistance was over the 0.32ohm and the value lasted for more than 1us. Thus, the resistance satisfied the magnitude and duration conditions of the failure criteria of solder joints. The number of data in normal state and abnormal state was 840 and 50, respectively.

Based on the time to failure, the time series data of solder joint degradation were classified into the normal and abnormal conditions. Consequently, all feature sets including the resistance were



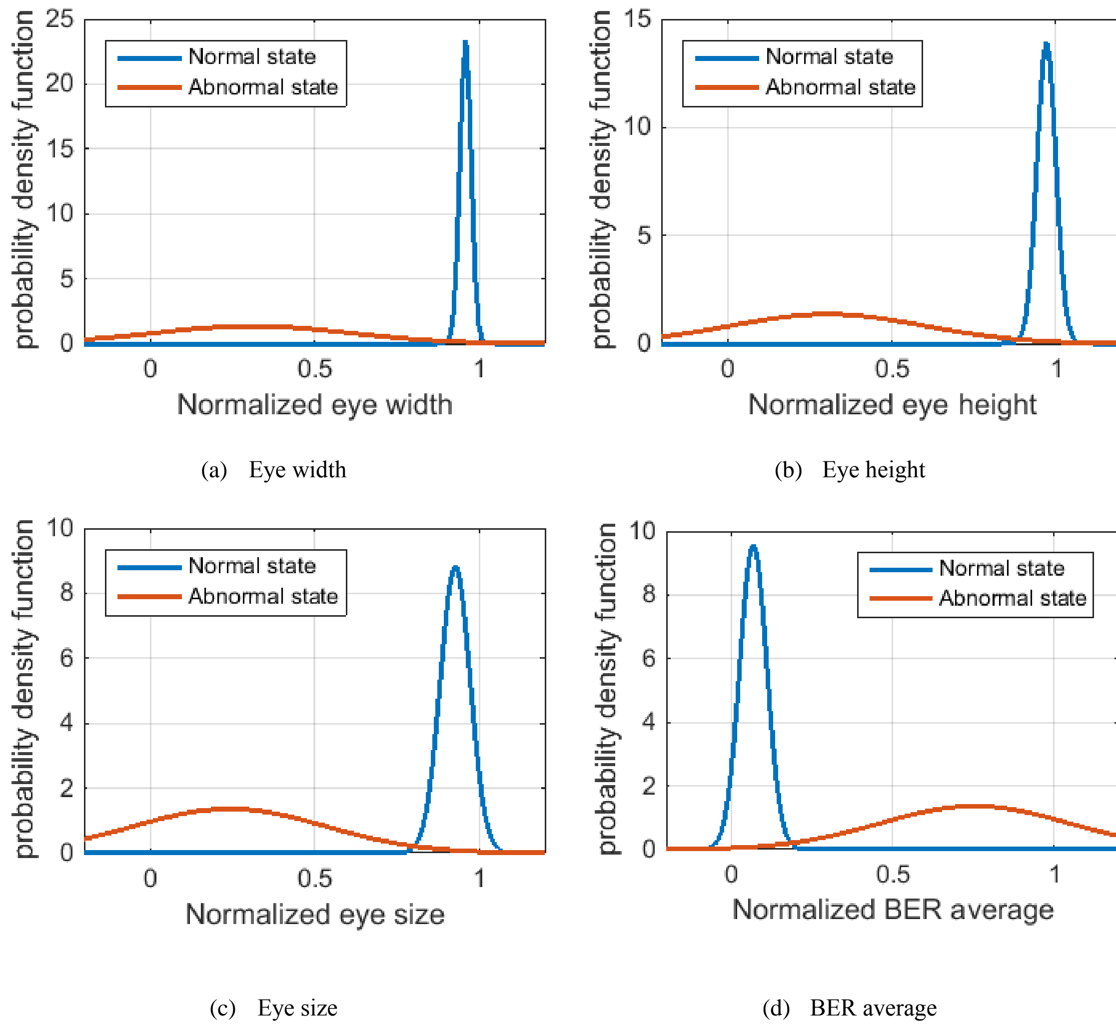
(a) DC resistance in the expanded y-axis (b) DC resistance

Figure 16 DC resistance and time to failure based on the failure criteria of solder joints (sample #1)

classified into normal state when the time was lower than the time to failure, and abnormal state when the time was over the time to failure. Before the classification, all feature datasets were normalized to place within [0,1] for comparison of different datasets in a reference alignment. By aligning the datasets to [0,1], the relative changes of the features could be observed. The feature sets were normalized by,

$$Normalized\ z_i = \frac{z_i - \min(z)}{\max(z) - \min(z)} \tag{5}$$

where z_i denotes specified feature values at time i.



(a) Eye width (b) Eye height

(c) Eye size (d) BER average

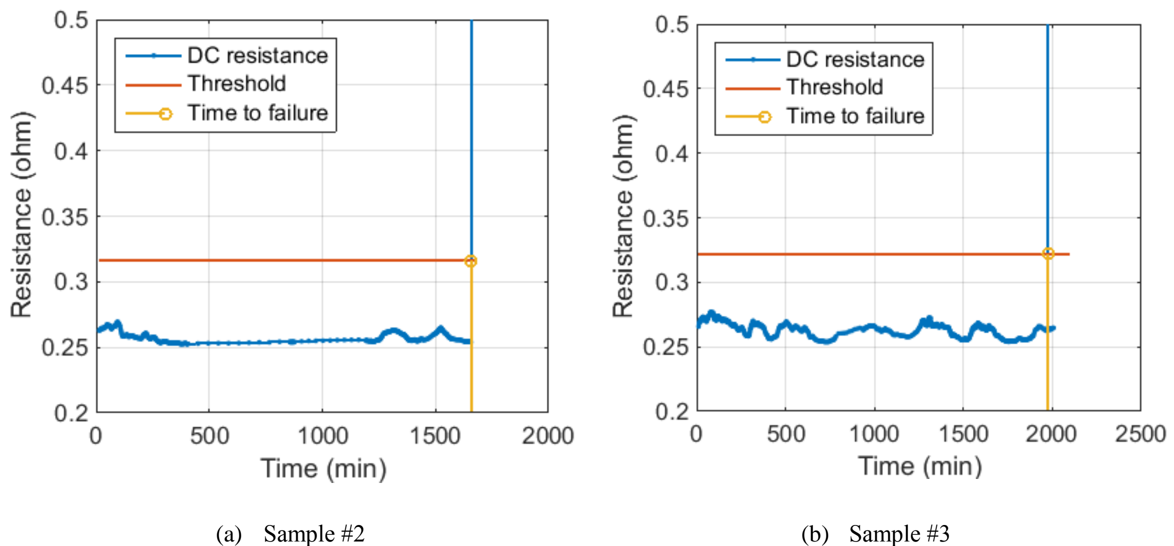
Figure 17 Probability density function of the features extracted from BER matrix (sample #1)

Figure 17 shows the probability density function of the classified features extracted from BER matrix. Distribution of normal and abnormal states was assumed to be normal. Because the higher eye width, eye height, and eye size means more healthy state, measurements indicating the normal state was located near to 1. With the deterioration of the solder joints, the measurement decreased to the minimum of the feature values. On the other hand, higher BER average means the large number of bit errors in the BER matrix, normal state data was located near to 0. Even though the number of abnormal state data is much smaller than that of normal state data, it was observed that the difference between the data of each states was significant large because distribution of the normal state data shows narrow dispersion.

Times to failure of the rest test samples were produced by the same failure criteria. Figure 18 shows the DC resistance and the times to failure of sample #2 and #3. The times to failure of sample #2 and #3 were 1658mins and 1946mins respectively. Based on the times to failure, normal and abnormal states of the solder joints were determined, and then feature datasets were classified as the previous procedure.

5.2 Feature Selection

The separation index that was defined in (4) was calculated to select a feature that has maximally separated means and narrow dispersions of normal and abnormal states. Figure 19 and Table 2 show the separation analysis results of BER features. Features extracted from the BER matrix



(a) Sample #2 (b) Sample #3

Figure 18 DC resistance and time to failure based on the failure criteria of solder joints

showed different separation index depending on the samples. Variation within samples was larger than variation within the features. It means that relative comparison of separation index between the features can be performed rather than focusing on the absolute value of the separation index.

Generally, eye size showed the highest separation index out of the features. This is because the eye size contains more general geometric information about the digital signal integrity than other features. Eye size reflects the size of regions where digital signals pass the error detection criteria. On the other hand, eye width and eye height address whether the digital signal passes or not the error detection criteria fragmentarily, in horizontal and vertical views. Thus, eye width or eye height might not change with the signal degradation depending on the quality issues. If jitter noise increases more over than the signal level, eye height might not change, while eye width would decrease. Therefore, eye size showing the total signal size was determined to be used for fault diagnosis in this study.

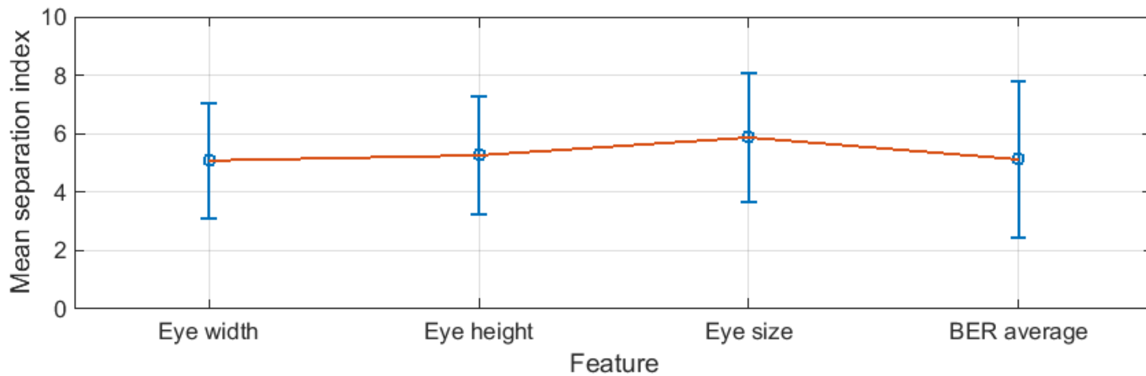


Figure 19 Mean separation index of BER features

Table 2 Separation analysis results of BER features

Feature	Separation index			Mean	Std
	Sample #1	Sample #2	Sample #3		
Eye width	7.31	4.28	3.64	5.08	1.96
Eye height	7.59	4.63	3.57	5.26	2.01
Eye size	8.19	5.63	3.78	5.87	2.21
BER average	8.18	3.88	3.25	5.12	2.67

5.3 Fault Diagnosis

Fault detection using the failure threshold was conducted using eye size and time to failure was calculated depending on measurement features. Figure 20 shows eye size, DC resistance, and times to failure that were detected based on the features of sample #1. It was showed that eye size gradually decreased during the test time and presented fluctuation from about 1000min. After about 1700min, eye size dropped dramatically. On the other hand, DC resistance changed in lower variations during the test time and showed dramatic changes near to the time to failure. The times to failure based on eye size and DC resistance were 1680min and 1671min, respectively. The time to failure using DC resistance was earlier than that using eye size, but the difference between them was relatively small compared to the overall lifetime. The time difference was 9.6mins and proportion of the difference in the time to failure based on DC resistance was 0.005.

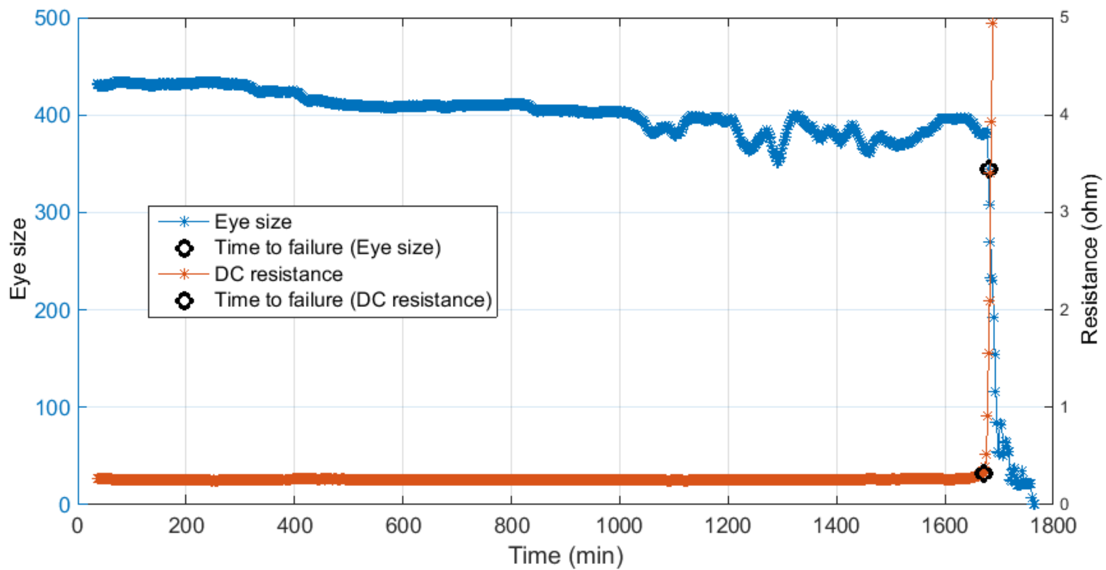


Figure 20 Eye size, DC resistance, and times to failure depending on the feature (sample #1)

Table 3 Time to failure depending on measurement features

Measurement	Feature	TTF (min)		
		Sample #1	Sample #2	Sample #3
DC resistance	Resistance	1670.7	1668.9	2043.2
BER	Eye size	1680.3	1676.5	2033.8
Average		1675.6	1672.7	2038.5
Relative accuracy $\left(\frac{BER - Resistance}{Resistance}\right)$		0.0057	0.0046	-0.0046

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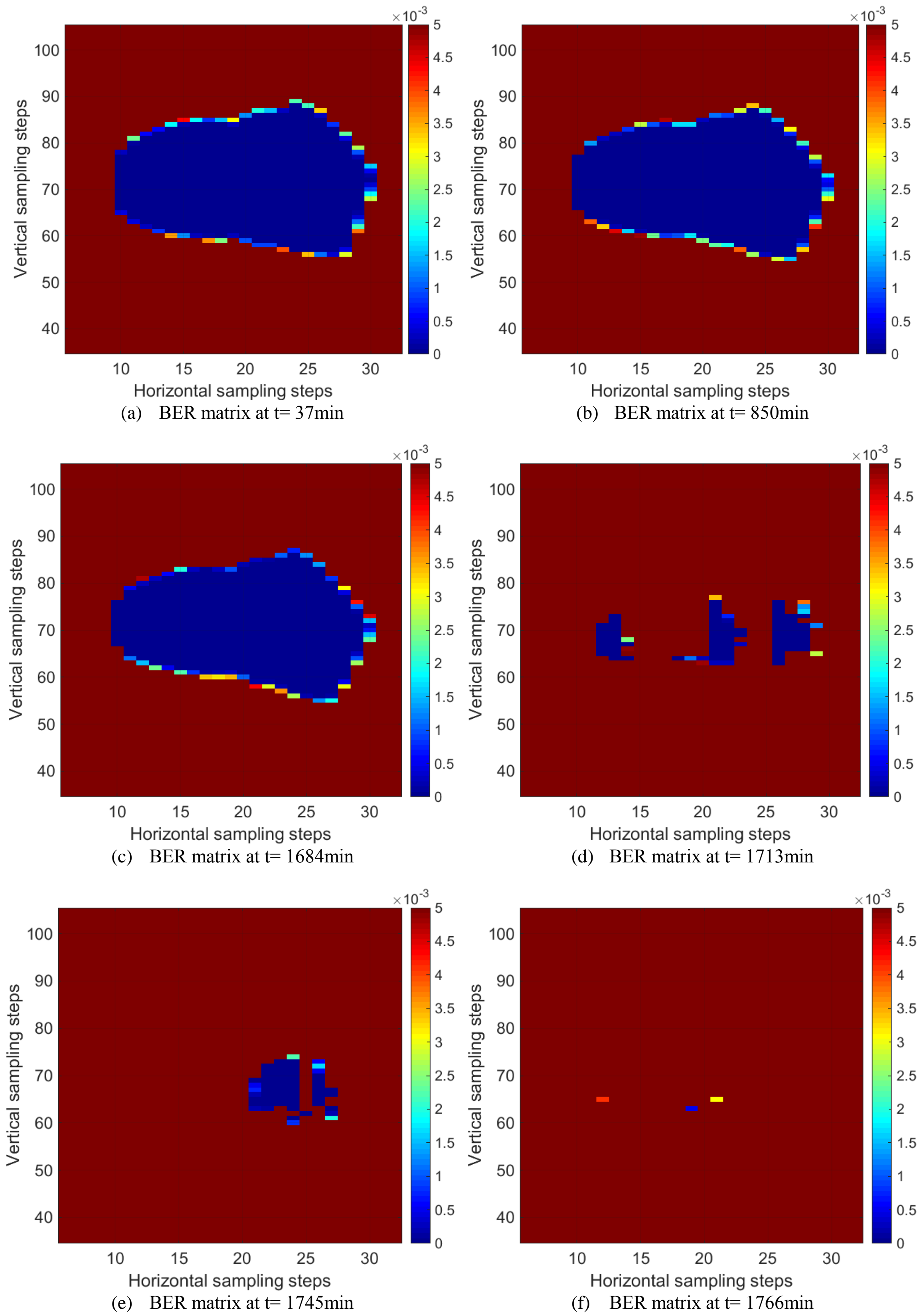

Figure 21 BER matrix during the test time (sample #1)

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Table 3 shows the times to failure depending on measurement features of all samples. Broadly, eye size derived similar times to failure when using DC resistance. The fault detection accuracy using BER features showed 0.005 relative accuracy in an assumption that the real time to failure is the time to failure based on resistance failure criteria. And two of samples showed later detection when using BER features than when using resistance data.

Figure 21 presents BER matrix of sample #1 during the test time. BER matrix showed slightly small eye size at1684min near to the time to failure according to eye size. Eye shape of the BER matrix got out of its original shape rapidly after the time to failure, while eye shape barely changed before the time to failure. It means that BER matrix reflects the signal integrity and presents the health of solder joints.

The experimental results showed that the fault detection using eye size derived similar times to failure with that using the existing monitoring parameter and failure criteria. It presents that the capability of features extracted from the BER matrix to detect faults of solder joints. Furthermore, BER measurements and the features reflected degradation of solder joints sensitively through showing the gradual changes and fluctuation during the test time. It shows potential capability of BER measurement to be used for the anomaly detection of solder joint failure to give more sufficient time to prepare maintenance and repairs.

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VI. Conclusions

6.1 Conclusions

This study developed an on-chip monitoring system for nonintrusive health monitoring of solder joints. BER which represents states of digital signals was used because the measurement can be conducted without external sensing devices while measuring the state of bits passed through the transmission channels. The monitoring system was developed using a digital transceiver toolkit, Stratix V of Altera. It was verified that the BER measurement through the monitoring system can be used to detect the solder joint degradation through an accelerated life test of solder joints. BER and DC resistance were collected under the accelerated life test. Features from BER measurement: eye width, eye height, eye size, and BER average were extracted and evaluated through statistical comparison based on Fisher's discriminant analysis that assesses the separation between normal and abnormal states. The normal and abnormal states were classified on basis of the conventional failure criteria of DC resistance. Eye size from BER showed the highest separation out of the feature sets. Times to failure derived using eye size was close to the times to failure based on the conservative failure criteria using DC resistance.

This study contributed to develop the on-chip monitoring system and showed that the capability of BER measurement to detect faults of solder joints. Since the developed monitoring system is an on-chip system which measures the solder joint states without external sensing devices, maintenance of electronic systems including solder joints can be performed much easier at a low price. And the experimental results showed the gradual changes and fluctuation with the degradation of the solder joints. The monitoring system finally can be used for fault diagnosis and prognosis of solder joints. Furthermore, the on-chip monitoring system can be applied to general electronic components and systems, not only solder joints. If BER checkers and reference data passes are implemented in circuit boards, the health of electronic components operating with digital signals can be monitored likewise solder joints based on the digital signal characteristics. For example, the health of microprocessors and interconnects in electronics that have high risks of failure depending on operating and environmental conditions can be managed, and their failures can be prevented by detecting faults or predicting lifetime of components prior to failures. To improve the monitoring system based on BER measurement and verify the monitoring system, degradation data of various electronic components under different stress conditions should be conducted.

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Meanwhile, the on-chip monitoring system has limitations in terms of measurement methodology and conditions. Because the on-chip monitoring system measure the BER from the digital signals, the electronic components to be observed should be on operation with digital signals. And a transmitter and a receiver are needed across the electronic components to construct a signal transmission channel. Therefore, failure risk priority should be analyzed to concentrate digital signal pass to measure BER on components of high risk of failures for economical monitoring system.

6.2 Recommendations for Future Works

There are recommendations for future works of the on-chip health monitoring system development. The recommendations are based on the difficulties and limitations that the author faced in this study. The recommendations can be classified into three parts likewise the experimental verification; accelerated life test, feature selection, and fault diagnosis.

6.2.1 Accelerated Life Test

Additional accelerated life test should be conducted to collect degradation data of various electronic components under different stress conditions. The additional degradation data can be used to verify whether the monitoring system can be implemented in real operating environment of various applications. Performing the accelerated life test of microprocessors and interconnects to provide wide application coverage of the monitoring system is left for future work. When conducting accelerated life tests, stress conditions in particular should be controlled accurately to control the test time and failure modes. For example, nitrate concentration in the corrosion tests conducted in this study affected to the time to failure of solder joints. The volume of cotton to create the nitric fume was critical to control the stress conditions as well. An excessive amount of cotton in the Teflon fixture caused to liquid connection between the signal pass and ground, eventually resulting in short.

6.2.2 Feature Selection

The results of the experiment showed that BER can be a measure to detect faults by using one of features of BER measurement preferentially. However, fault detection performance changes depending on the variety of features and the number of features. Eye width, height, size, and BER average are examples of features that can be extracted from BER. Other features should be tried

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for improving fault detection performance. For example, shape of eye from the BER matrix can be used as a feature and give detailed behaviors of digital signal deteriorations. Eventually, shape of eye can be an evidence for failure modes of electronic components such as open or short. And maintenance and repair methods can be determined based on the estimated failure modes. The number of features is also importance to estimate states. Large number of features usually lead accurate fault detections, but can lead computational overloads by adding redundant information.

Feature evaluation method can be improved as well. The feature selection conducted in this study was regardless of time information by gathering the normal and abnormal data without time feature. The evaluation method can miss gradual value changes variating from normal to abnormal conditions, and give small score to the feature showing that changes. For example, BER average showed sensitive changes likewise eye size during the aging process of solder joints, but the separation index was low in the results of two samples. This is because that gradual changes of BER average increased the variations of the normal states. In order to solve this problem, states of solder joints can be classified into three stages; normal, uncertain, and abnormal. And normal states can be determined with the same time range of abnormal states. Using this method, normal and abnormal states could be separated clearly. Thus, the feature evaluation with time information is next study to lead useful feature selection for fault diagnosis and prognosis.

6.2.3 Fault diagnosis

Various fault diagnosis algorithms based on machine learning can be applied to improve the detect performance with consideration of their pros and cons. The conventional failure criteria (20% increasing from original values) had limitations that cannot be used to BER average feature. It is because BER average ranges from 0 to 1 and the original values were over 0.8. Thus 20% increase of the normal states is over the BER average range. In order to use BER average was a feature, the failure detection technique is needed to be modified in consideration of each feature characteristics. And the threshold method usually doesn't fit to the anomaly detection or features having large variations. To overcome the limitations, complex statistical classification or clustering algorithms can be applied to detect anomaly and predict the failure of solder joints.

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Acknowledgements

Although this dissertation is an individual work, I could never have achieved or explored the depths without the help, guidance, and commitment of many people.

Firstly, I would like to express my special appreciation and thanks to my advisor professor Daeil Kwon for his endless support and encouragement. He offered me a precious chance to join his lab, and it was a great pleasure to be a member of ISR lab. He always gives careful attention to my opinions and guided me with kindness and patience. His advice on both research as well as on my career have been priceless. Secondly, I would also like to thank my committee member, professor Duck-young Kim and Seungchul Lee for serving as my committee members even with their busy schedule. I also want to thank you for letting my defense be a memorable moment, and for your brilliant comments and suggestion. Thirdly, a special thank you to Jeong-ah Yoon, Jinwoo Lee, Geumtaek Kim, and Jiwon Lee for their commitment and cooperation. I could spend pleasant time in the lab thanks to them.

Finally, I would also like to thank my parents and my younger brother. They always support and encourage me with their best wishes. May joy and peace abide in us all.