NONLINEARITY COMPENSATION AND HIGH VOLTAGE PROTECTION OF CURRENT STEERING DAC

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2016

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A thesis
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Master of Science

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12. 14. 2015

Approved by

Advisor

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Abstract

Current steering digital to analog converter (DAC) always suffer from lots of problem like mismatch errors and timing related dynamic errors. Diverse studies from art-of-the-state suggest methods for compensate some of these errors. Typical examples of compensation methods are segmentation, quad-quadrant (Q^2) random walk and dynamic element matching (DEM). These compensation methods reduce lots of fundamental errors while used together with other proposed technique in this thesis.

This thesis propose two structure. One structure is related with industrial applications. Industrial application usually requires 10V swing for voltage driving and 20mA swing for current driving. Conventional industrial DAC satisfy these swing requirement with high voltage driving amplifier. But driving amplifier consumes additional power and adds its own distortion to output signal. High voltage protection structure is proposed to satisfy industrial swing requirement and solve the problems of driving amplifier combined DAC. Proposed high voltage protection structure decrease cost of manufacturing by decreasing number of high voltage transistor. Proposed structure also increases linearity by changing effective output impedance and decreases additional current consumption while satisfying industrial swing requirement.

The other proposed structure is related with resolution improving. Recent current steering DAC becomes fast enough to cover over GHz range with developing technologies. However resolution is still limited by matching properties. Current steering DAC with resolution improving sigma-delta ($\sum\Delta$) modulation is proposed. It increase resolution by noise shaping of $\sum\Delta$ modulation while sacrificing speed. It still fast because recent current steering DAC is very fast. $\sum\Delta$ modulator only randomize LSB side and shaping LSB related noise. Q^2 random walk and DEM are also included to randomize MSB side and reduce MSB related noise.

Two version of test chips are tested. 12bit random rotation-based binary-weighted (RRSB) DEM current steering DAC is implemented in 130nm compliment metal-oxide semiconductor (CMOS) process. Test result shows the effect of MSB side randomizing DEM from art-of-the-state. Proposed 14bit resolution improved DAC with high voltage protection is implemented in 180nm bipolar + compliment + double-diffused metal oxide semiconductor (BCDMOS) process. Test result verify performance improvement in frequency domain.

Operation voltage and resolution of DAC can be changed by each proposed method. DAC can be applied to various application that require various operation voltage and resolution by using both method properly.

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Nomenclature

∑Δ.	Sigma-delta.
ADC	Analog-to-digital converter
BCDMOS	Bipolar-CMOS-DMOS metal oxide semiconductor
CMOS	Compliment metal-oxide semiconductor.
DAC	Digital-to-analog converter
DEM	Dynamic element matching
DEMOS	Drain extended metal oxide semiconductor
DMOS	Double-diffused metal–oxide–semiconductor
DNL	Differential Non Linearity
HD3	Third order harmonic distortion.
HV	High voltage
HV MOS	High voltage metal oxide semiconductor transistor.
IC	Integrated circuit
INL	Integral Non Linearity
LDMOS	Laterally diffused metal oxide semiconductor
LSB	Least significant bit
LV	Low voltage
MOS	Metal oxide semiconductor.
MOSFET	Metal oxide semiconductor field effect transistor
MSB	Most significant bit
NTF	Noise transfer function.
Q^2	Quad-quadrant
RRBS	Random Rotation-based Binary-weighted

RZ	Return-to-zero
SAR	Successive approximation register
SFDR	Spurious-free dynamic range
SNR	Signal to noise ratio.
STF	Signal transfer function.

Chapter I

Introduction

Data converter, such as digital-to-analog converter (DAC) and analog-to-digital converter (ADC), plays a role as a bridge of analog signal that actually exist in the world and digital signal processed in many kinds of circuit or processor. With developing the technology, the number of digital devices used in everyday life is significantly increased and the sort was also diversified. According to this change in our life, data converter also used in various areas. In addition, the degree of integration of the digital processor is increased with the development of the technology and the performance is also gradually advanced, data converter still plays an important role although the various circuits are replaced with a digital circuits.

Especially, DAC is used in various applications such as audio and communications. The necessary performance of the DAC also has been growing continuously according to the rapid development in the various fields such as communication that DAC is frequently utilized. This thesis examines the various causes that limit the performance of the DAC and apply some appropriate method to improve them. In addition, high voltage protection scheme which spreads the use of range and improve the performance is proposed to be able to use in various purpose.

1.1 DAC Basics.

1.1.1 DAC architecture.

DAC is a device that is applied to the digital input and print out the appropriate analog voltage. In other words, it must be able to print out many kinds of analog voltages with electronic devices. The various devices are used to make an analog voltage in DAC. Resistor, capacitor, and transistor are mainly used. And DAC prints out a desired voltage using the complementary metal-oxide semiconductor (CMOS) switch with these elements.

1.1.1.1 Resistive DAC.

Resistive type DAC is a basic and the simplest structure. Let N denote the resolution of DAC and let V_{ref} denote reference voltage for DAC output swing. Easiest way to construct N bit resistive DAC is

connecting 2^{N-1} resistor between the V_{ref} and ground in series. 2^N-1 different output voltage is made by the voltage dividing from the ratio of the resistors. If the output voltage is directly connected to a load, an effective resistance changes and consequently output voltage also changes. Therefore, an analog buffer is usually used at the output stage to reduce the change in the output resistance when they drive the load. Resistive DAC provide 2^N-1 different voltage simultaneously, even though some modified structures of it aren't. It commonly used in flash ADC because flash ADC compare analog input voltage to various reference voltage simultaneously.

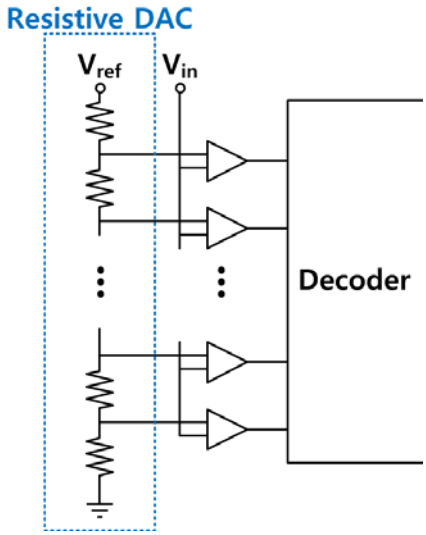


Fig. 1. Flash ADC with basic resistive DAC.

R-2R DAC has a structure that modified from the basic resistive DAC with a reduced number of resistor. R-2R structure just needs about 3N number of resistors while the basic resistive DAC needs 2^N-1 resistors. Fig. 2 show R-2R DAC architecture. It constructed with two types of resistor which are R and 2R. Resistors are connected in π shape. Parallel connection of two 2R resistors have R effective resistance. Series connection with two R resistors have 2R effective resistance. Continuous connection with R and 2R resistor make same effective resistance at each node. It makes equal current dividing at each node and binary weighted resistive DAC.

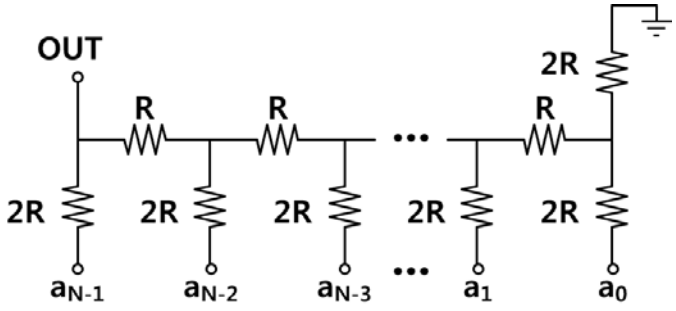


Fig. 2. R-2R DAC architecture.

1.1.1.2 Capacitive DAC.

Capacitive type DAC which is similar to the resistive DAC generates an output voltage from a capacitor ratio. Each binary weighted capacitor stores charges, and these charges are redistributed to generate proper output voltage depending on input code. Capacitive DAC cannot drive output directly because it generates output using the stored charges in each capacitors. Capacitive DAC also requires an analog buffer at the output stage like a resistive DAC. Meanwhile, it is a major difference of capacitive DAC compared to resistive DAC that capacitive DAC doesn't occur a direct charge path with resistor. Capacitive DAC are frequently used in the successive approximation register (SAR) ADC.

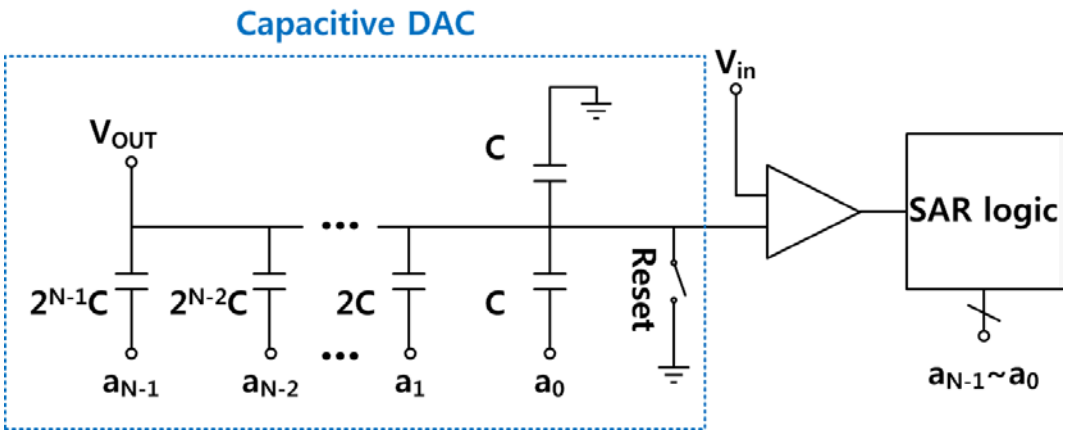


Fig. 3. SAR ADC with capacitive DAC.

Capacitor has a large size compared to other elements and basic capacitive type DAC requires 2^N number of unit capacitors to implement resolution of N bit. However, it is difficult to implement high resolution using capacitive DAC due to the size of capacitor. So a split capacitor DAC is a complemented structure from the basic capacitive DAC. Conventional capacitive DAC generate voltage by redistributing charge stored in binary weighted capacitors. By adding the bridge capacitor which splits most significant bit (MBS) side DAC and least significant bit (LSB) side in the middle, effective charge redistributed by LSB is reduced by $2^{N/2}$. MSB side DAC and LSB side DAC can have similar size of capacitor array by splitting each other. MSB side capacitor array which occupy most of silicon area can be reduced. With this split capacitor DAC architecture, the required number of capacitor reduced by $2^{N/2}$.

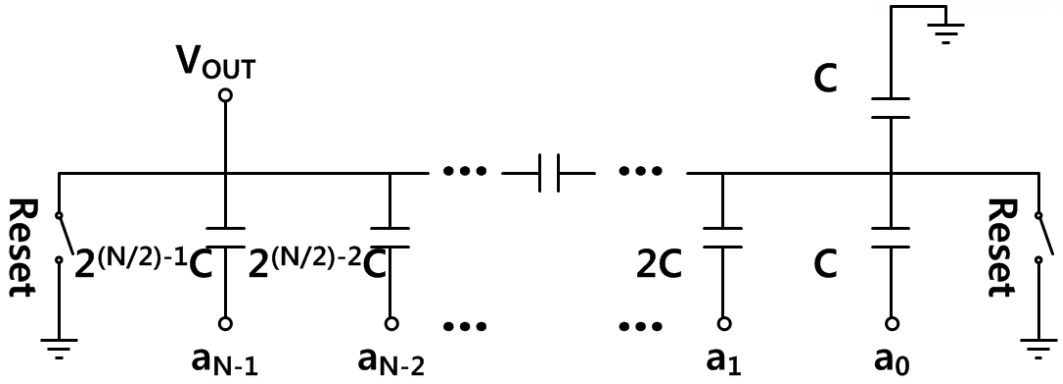


Fig. 4. Split capacitor DAC architecture.

1.1.1.3 Current steering DAC.

Current steering DAC is a structure that prints out an analog output current switching each current sources following an input data. In general, we use a metal oxide silicon field effect transistor (MOSFET) as a current source. Due to the current type output, it is the biggest difference between resistive and capacitive type DAC and current steering DAC that the load is directly driven without buffer. And it is fastest DAC compared to other DAC architectures.

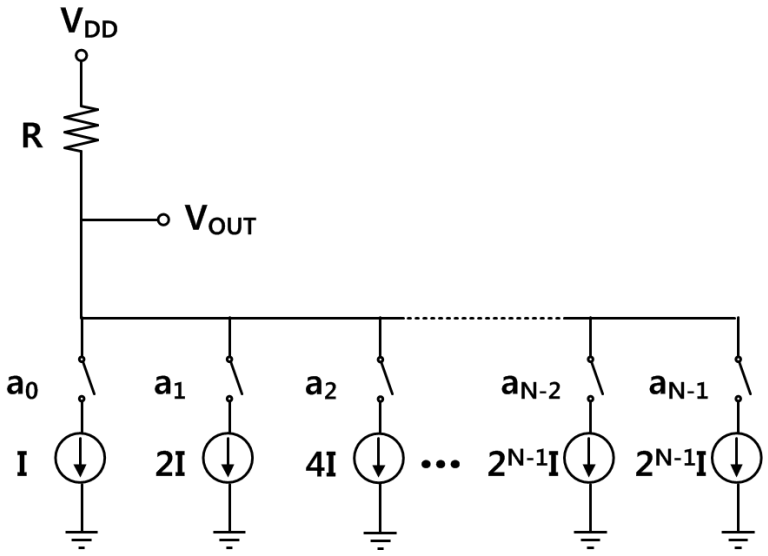


Fig. 5. Current steering DAC architecture.

In general, current steering DAC activates each switches following the input data to use a binary weighted current cell. Let I_n denote current of n^{th} bit current, I_u denote current amount of unit current cell, b_n denote nth bit input code. Current amount of n^{th} bit is as in the following.

(1)

$$I_n = 2^n I_u$$

Total current I_T of binary weighted current DAC expressed as following equation.

$$I_T = \sum_{n=0}^{N-1} b_n I_n = \sum_{n=0}^{N-1} 2^{n-1} b_n I_u \tag{2}$$

However, in some special cases, input code is used as form of thermometer code which decoded from binary weighted code. Decoded input x is like this.

$$x = \sum_{n=0}^{N-1} 2^{n-1} b_n \tag{3}$$

Output current of thermometer current steering DAC is

$$I_T = x I_u \tag{4}$$

It looks similar with binary weighted DAC. Difference of these two types of DAC is explained in chapter 3.

1.1.1.4 Sigma-delta DAC.

Sigma-delta (∑Δ) DAC is one of most popular DAC architectures. Important difference of Sigma-delta DAC is oversampling. Conventional Nyquist rate DAC has signal bandwidth about half of sampling frequency (f_s). Contrary to other DAC architecture, oversampling DAC has smaller signal bandwidth than Nyquist rate DAC. Rather than signal bandwidth, sigma-delta DAC has high resolution by noise shaping.

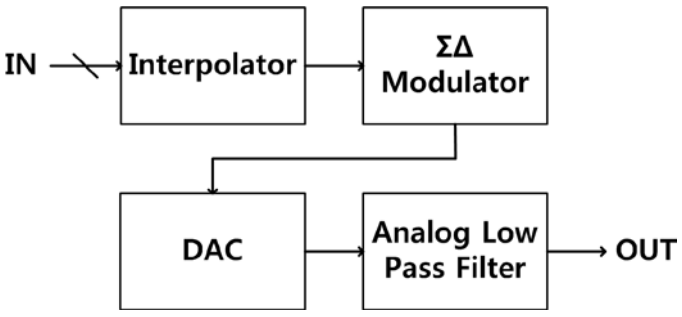


Fig. 6. Fundamental structure of sigma-delta DAC.

Fundamental sigma-delta DAC structure is show in Fig. 6. Multi bit input is converted to noise shaped digital signal. Usually sigma-delta structure using single bit DAC. Single bit DAC output looks similar with just logic value like 0101. But, this signal show proper analog signal in frequency domain. This noise shaping comes from sigma-delta modulator.

Sigma-delta modulator has different transfer function for signal and noise. With input X(z) and quantization error E(z), Output Y(z) become

$$Y(z) = X(z) + (1 - Z^{-1})E(z) \tag{5}$$

(5) is simplest example of noise shaped signal. It show signal transfer function 1 and noise transfer function $1\text{-}Z^{-1}$. This represent only noise transfer function is high pass filter. Other sigma-delta modulator also has high pass filtering noise transfer function. Because most of noise move to high frequency, Signal and noise in low frequency look high resolution DAC.

Because most of sigma-delta DAC construct of digital block, it consume little power. By oversampling, it has very high resolution but slow speed.

1.1.2 DAC specification.

The DAC in reality could have some errors and limits to operate. Therefore the performance of DAC is decided by the ratio of errors and similarity with ideal DAC. There are some quantified factors that can represents the performance of DAC.

For example,

Resolution - Resolution means how DAC concisely express analog output. The minimum step size is $\frac{V_{ref}}{2^N}$.

Gain error - The difference between slop of ideal DAC transfer function and slop of non-ideal DAC transfer function.

Monotonicity - Monotonicity represents the same tendency of DAC input and output without inversion part. If the output increases while the input also increases, we consider the DAC is monotonic.

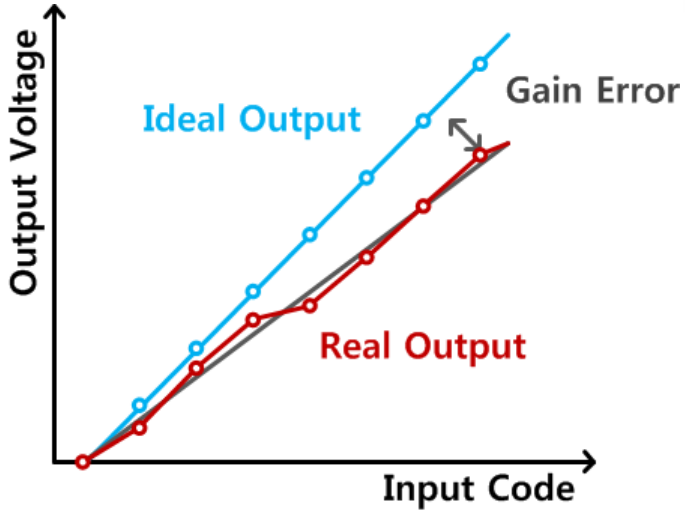
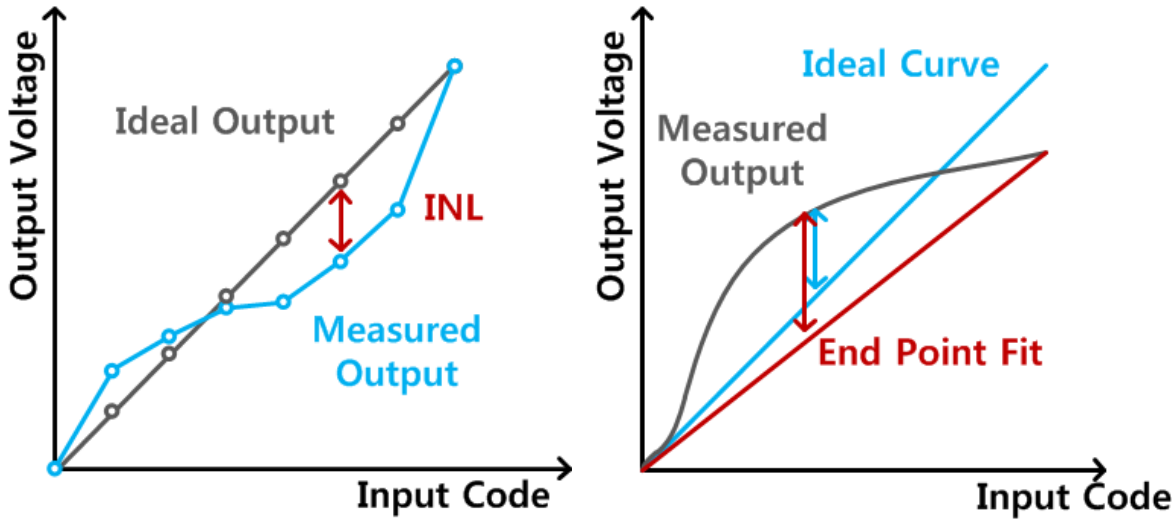


Fig. 7. Gain error of DAC

There are some other specifications which can stand for the characteristic of DAC.

1.1.2.1 Integral non linearity (INL).



(a) (b)

Fig. 8. (a) Meaning of INL and (b) two definition of INL

INL is an index that shows the difference of ideal DAC output and non-ideal DAC output comparing with LSB. There are two methods commonly used to express INL. First method is made up by comparing ideal DAC output and non-ideal DAC output as I said before. Second method is to compare with non-ideal DAC output in perspective of endpoint-fit line. INL must be 0 at the starting point and end point when second method is used.

In reality, second method is more commonly used than first one. We can find out the reason in the structure of non-ideal current steering DAC. The result could be very different if the resistor connected to the output node of the current steering DAC has an error. When the first method is used in this case, large INL occurs. Even if the performance of DAC core is good, INL does not consider this performance well and affected by inaccurate resistors. However, the second method can ignore the resistor error since the error is included in end point value. Consequently, the second one is commonly used because it can express the performance of DAC core more than first one.

1.1.2.2 Differential non linearity (DNL).

DNL represents the difference between step size of non-ideal DAC output and that of ideal DAC output comparing with LSB size.

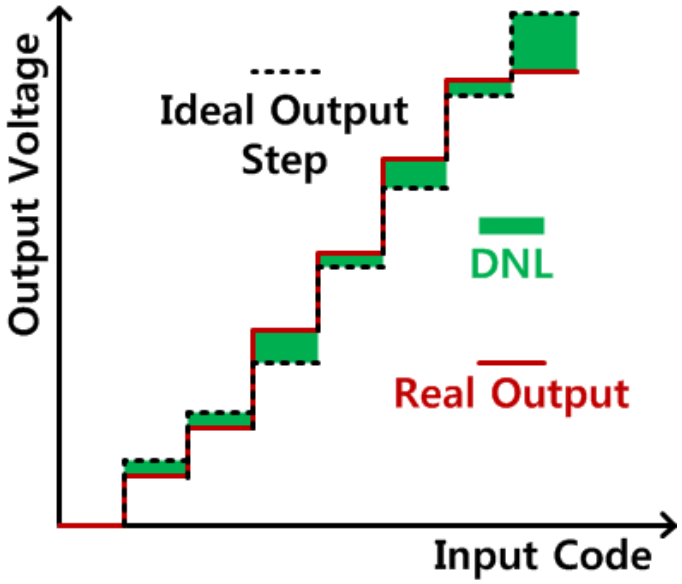


Fig. 9. DNL of DAC.

If DNL is less than -1, code inversion occurs at that part. There are some cases that output value decreases while input value increases.

INL & DNL are direct indexes which stand for the degree how non-ideal DAC is similar with ideal DAC. Thus, these are regarded as important indexes in expression of DAC performance.

1.1.2.3 Spurious-free dynamic range (SFDR).

SFDR is an index which represents the dynamic performance of DAC. SFDR is the ratio of the RMS value of the signal amplitude to the RMS value of the highest spurious spectral component in the first Nyquist zone. SFDR is a good index for confirming the harmonic distortion value of DAC. SFDR is very important factor in communication system. In communication systems, there are lots of channels that are used in transmitting and receiving signal. Frequency and strength of signal also diverse. Spur generated by large signal may occurred in various frequency like other channel frequency. This spur also can have strong power that comparable with other channel signal strength. Like this, suppress spur in DAC is necessary to avoid interference with other channel.

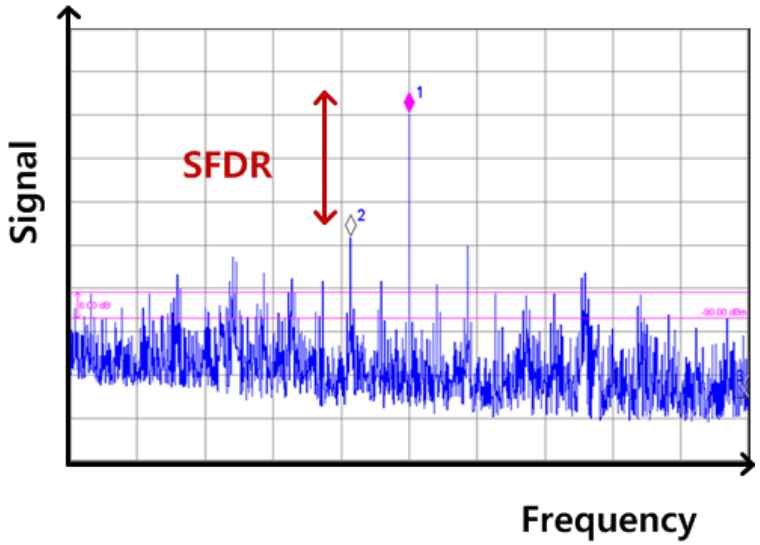


Fig. 10. Spurious-free dynamic range of DAC.

1.2 Sources of Nonlinearities and Dynamic Errors.

Non-ideal digital to analog converters always suffer from non-linearity. What's the sources of these nonlinearities and other errors that degenerate performance of digital to analog converter.

Following contents show and classify causes of non-ideal performance in digital to analog converter.

1.2.1 Non-identical current cell design.

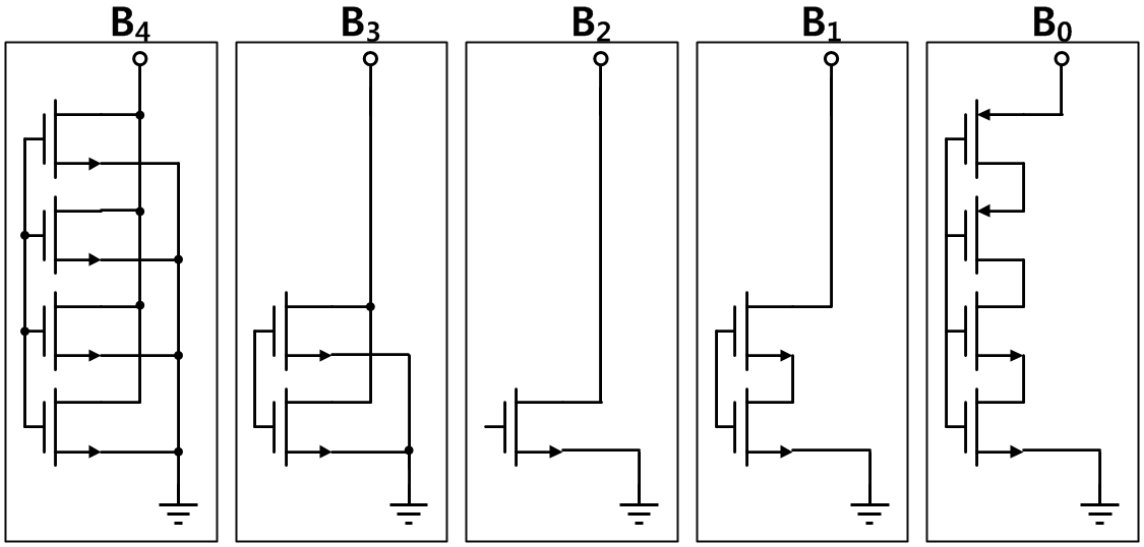


Fig. 11. Circuit diagram of current cells with slightly different unit current.

Nonlinearities usually comes from non-ideal current sources that supply less or more amount of current than ideal amount. Simplest reason for non-ideal current cell may be a difference in current cell design. Of course nobody try to design a DAC with current error even in schematic design. But several DACs are sometimes designed not to ensure the perfect linearity. Easiest way to implement exact current amount in ideal schematic simulation is to connect identical unit current cells in parallel. In the [17], [18], DACs does not use the unit current cells which have same form with MSB current cells in case of LSB current cells. It designed to make the current flow by reducing effective channel length with cascaded current. Although it is seemed that there can be some errors in the design step, it does not matter since these kind of things are designed not to affect to the performance of the DAC. Even, DAC can be designed with this series connection structure to have less than few % LSB of current error. This type of design method cannot be a problem since it gives other advantages such as reducing complexity of DAC or random matching advantage because of increased current cell size.

1.2.2 Random mismatching errors.

1.2.2.1 Mismatch classification.

Generally, the main cause of linearity such as INL, DNL is each current cell's mismatch. The output value which made by summation of current affected by errors which from current cell mismatching and difference between ideal current. Let mismatch of n^{th} code current cell is ε_n, current of each cell is

$$I_n = 2^{n-1} I_u + \varepsilon_n \tag{6}$$

and total output current I_T in (2) is revised as follows.

$$I_T = \sum_{n=0}^{N-1} b_n I_n = \sum_{n=0}^{N-1} b_n (2^{n-1} I_u + \varepsilon_n) \tag{7}$$

INL at input k is described as below.

$$I_T(k) - kI_u = \sum_{n=0}^{N-1} b_n I_n - kI_u = \sum_{n=0}^{N-1} b_n (2^{n-1} I_u + \varepsilon_n) - kI_u = \sum_{n=0}^{N-1} b_n \varepsilon_n \tag{8}$$

INL has various mismatch offset like above, the error limit DAC's performance. In case of |INL|<0.5LSB, DAC's monotonicity is guaranteed.

The mismatch comes from various error. For example, current source's width and length which has different value of designed result, MOSFET oxide thickness, doping concentration can make errors. There is also a way to modeling for relative deviation for unit source's current mismatch. So some research estimate yield in advance [2].

According to the research in [14], parameter P described like this.

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \tag{9}$$

Where A_P is the area proportionality constant and S_P is the spacing proportionality constant for parameter P. This means mismatching in current cell can be divided into two types. One is short distance variation and second is long distance variation. Short distance variation has smaller correlation distance than dimension of transistor. This type of variation is inversely proportional to the area of transistors. Long distance variation has much larger correlation distance. Between two types of variation, there is trade off condition with size scaling. Large area decrease short distance variation and increase long distance variation, and small area increase short distance variation and decrease long distance variation.

1.2.2.2 Gradient error.

Basically, mismatch is occurred randomly, it is difficult to decrease random mismatch. Especially short distance variation has very small correlation distance than controllable scale. There are almost no method to for reducing effect of this, except for increasing device area.

In case of long distance variation, correlation distance is large. That scale of distance can be controllable. Even if long distance variation has regularity and directivity, effect of this can be reduced with good modeling of variation regularity and careful design for compensate this variation.

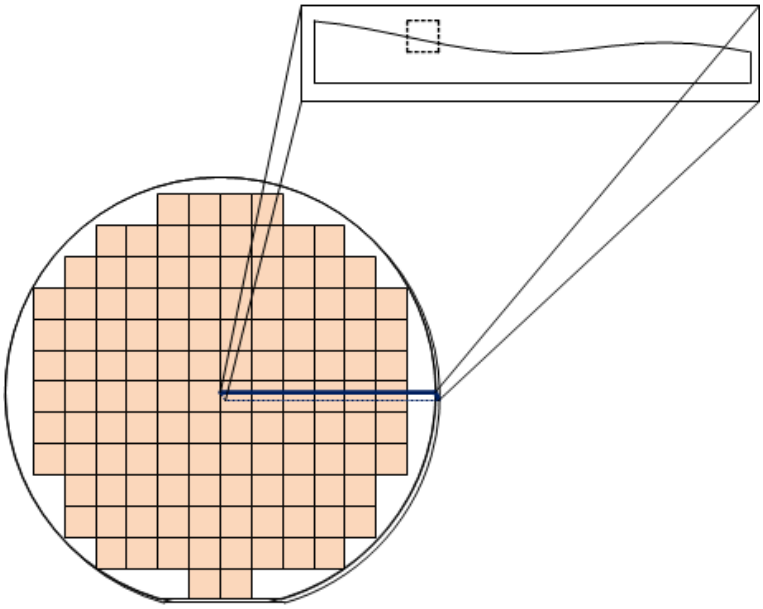


Fig. 12. Variation along silicon wafer and cross sectional view of it.

Fig. 12 shows some of long distance variation along with silicon wafer. Common variation in fabricated silicon wafer is circular shape distributed variation. It can be oxide thickness, or other process variation. Upper right side of Fig. 12 show cross section. Parameters are along whole wafer. However size of single chip is much smaller than boxed with dotted line area. Size of single chip is small enough to approximate mismatch along the chip area with Taylor approximation.

Most of mismatch error approximated by linear (first order) and quadratic (second order). With this simplified mismatch model, applying compensation algorithm can be feasible. Some compensation methods are explained on following chapter.

1.2.2 Code dependent output impedance.

Not only error of current affect output, even if it is current steering DAC. Referencing Ohm's law (V=IR), resistor also has an effect on output voltage. For current steering DAC, output current of it directly connects to output load. But current sources of DAC are non-ideal current source. Then output impedance is not infinite. Therefore, output voltage is affected by not only load of resistor but also impedance of current source.

Current source connected to output is changed by input codes. Non-ideal current source connection changes output impedance. In other words, output resistor varies with input codes. Changes of input codes also decrease performance of DAC.

1.2.3 Dynamic errors.

Nonlinearity is caused by error like current source mismatching and then output is different with ideal output. However, the error that measures through static analysis could be existed. DAC is not only used in simple DC output but also various high-frequency signal generation for communication or audio application. Although DAC has good linearity, actual converter doesn’t operate well in generation of high-frequency signal. As shown in previous, dynamic performance as SFDR is important factors of DAC characteristic. Dynamic performance degenerated by several reasons. Most of case, circuits operate with clock signal and signal transition should be occur for different output values. Signal transition is delivered additional error and the error affect nonlinearity of DAC.

1.2.3.1 Non-exact timing in the data switches.

One of difference between operation of ideal DAC and actual DAC is data switching timing. Jitter and skew in clock signal could be happened. Clock loading is depend on data. Also, mismatch of random component or parasitic component in layout lead to unwanted error signal generation due to switching timing error.

Especially, DACs isn’t switched all of input switch in every cycle. In other world, switching depend on transition of digital input code. The input code also affect the nonlinearity of DAC in each conversion step. If the one bit code is changed, only one current cell, driving circuit and digital control block that relate with changing code turns on and then effect of bias and power could be stable due to small power consumption in a moment. But, if most of code is changing, power dissipation is increased and instantaneous disturbance is occurred in bias parts.

To reduce the effect of code changing, return-to-zero (RZ) technique is generally used. RZ technique. Every switch return to zero after conversion procedure attenuate dependence of input code. However RZ technique has drawbacks like operating speed disadvantage and need for additional post-processing on output values. Current-mode logic is also one way to reduce problem.

- Clock feed-through

DAC is composed of not only analog current cell but also various digital circuit for driving switches. These circuit affect to output terminal because the circuit synchronize with clock signal. Driving signal from switch driver circuit appear to output terminal through capacitance. The error generates spur in output node.

- Rise and fall time difference

Although the circuit designed by CMOS, rise and fall time are not perfectly match. Also, turning on and off of switch doesn't occur perfectly simultaneously because MOSFET current source operate gradually and source voltage bias of MOSFET also changes. This switching asymmetry affect non-ideal output waveform.

- Break-before-make behavior

Conventional differential current steering DAC structure shown in Fig. 21. It commonly use both side MOSFET switches. The case of two of switch is off could be happened. In that state, not only output voltage but also bias voltage such as drain or source voltage of MOSFET on current cell alter. MOSFET of current source should be biased properly to operate in saturation region. When both side of switch turn off, VDD path of current source is eliminate and drain or source voltage of MOS are short to ground. Parasitic capacitors are also discharged. However, if the switch turn on, output current is changed by recovery behavior which consume current instantaneously for re-charging the current source and parasitic capacitor.

Chapter II

Applied Nonlinearity Compensation Method from State-of-the-art

As shown in chapter 1, operation of DAC has many source of error and various reason restrict the performance. Specification of DAC could be improved by reducing the effect mismatching. A technique that improves the performance has been intensively studied since the past.

This thesis apply not only its own proposed method but also some representative nonlinearity compensation method form stage-of-the-art. This chapter introduces and analyses state-of-the-art technique specially applied this research.

2.1 Segmentation.

There are many ways reducing errors and nonlinearity. It means best DAC can be made using all these methods. Most engineers try to apply error-correcting study, but DAC including all methods is rarely found out because of trade-off problem in not only DAC, but most circuit design.

Each method to improve performance needs additional circuits which consume extra power and increases complexity. And circuit such as digital circuit and clock tree has effects such as spur to DAC output. But one of worst drawback for DAC is complexity and size of circuit. For an example in 12bit DAC, it has the number of 2^N-1, 4095 unit current cell. Circuits related to these current cell might increase size and complexity a lot.

Size and Complexity are not only cost problem, but also trade-off problem directly related to performance of DAC. Random mismatch of DAC current cell explained in Chapter 1 is related with device's width and length which is size of each current cell. In other words, increasing area of current cell decrease mismatch error. By using same silicon area, DAC can directly improve matching error with large size current cells. So, it's important issue whether to assign area for digital compensation circuit or for current cell area.

Segmentation is way to assign optimum point of area for each digital and analog area. It assign digital area only for MSB linearity compensation circuits because MSB has more effect on overall linearity specification than LSB.

2.1.1 Binary coded DAC.

This is basic operation method of current steering DAC. All currents have weighted value of binary numeral and use assigned current with its codes. Small required area for digital circuit needed to data transmission makes design compact, because every current source directly matches binary current source one on one.

But in the case of binary code DAC, change of code directly turns on or off entire assigned current cell. Because one of significant error comes from these switches' on-off operation, error would be serious with its code's change. Especially, MSB code causes changes of switches over than half which results in critical issue.

For an example of 3bit DAC, $011_{(2)}$ to $100_{(2)}$ is just one step difference in the point of decimal system while 4 switches turn on and 3 switches turn off. Following equation (6) in chapter 1

$$I_T = \sum_{n=0}^{2} b_n I_n + \varepsilon_n = \sum_{n=0}^{2} 2^{n-1} b_n I_u + \varepsilon_n \tag{10}$$

So,

$$I_T(011_{(2)}) = 3I_u + \varepsilon_1 + \varepsilon_0 \tag{11}$$

$$I_T(100_{(2)}) = 4I_u + \varepsilon_2 \tag{12}$$

Then, difference is

$$I_T(100_{(2)}) - I_T(011_{(2)}) = I_u + \varepsilon_2 - \varepsilon_1 - \varepsilon_0 \tag{13}$$

One step changes in input code has error term of every current cell. Usually random distributed error is accumulated in statically and not related the sign of error. So, this change might cause large error.

2.1.2 Thermometer coded DAC.

Thermometer coded DAC is suggested to complement disadvantages from binary DAC. Thermometer consists of individualized unit current source. Binary input is converted to thermometer code by using thermometer decoder and code is assigned to unit current source. In other words, it arranges input value from binary code as putting 1 from lowest digit and 0 for others. From these generated code, it turns on current cell in order and vice versa. Using this method, minimized amount

of switch turns on and off every clock. Consequently, various noise and glitch from operation binary code DAC is reduced a lot.

Similar with binary cases, current of k^{th} unit current cell $I_u(k)$, with error of each k^{th} unit current cell $\varepsilon(k)$, then

$$I_u(k) = I_u + \varepsilon(k) \tag{14}$$

Total current is

$$I_T(x) = \sum_{k=1}^{x} I_u + \varepsilon(k) = xI_u + \sum_{k=1}^{x} \varepsilon(k) \tag{15}$$

1step difference at input x is

$$I_T(x) - I_T(x-1) = \left(xI_u + \sum_{k=1}^{x} \varepsilon(k) \right) - \left((x-1)I_u + \sum_{k=1}^{x-1} \varepsilon(k) \right) = I_u + \varepsilon(x) \tag{16}$$

For example, 3bit Current DAC. In the case of Binary structure one step transition from $011_{(2)}$ to $100_{(2)}$ need all 7 switches switching operation. But in the case of thermometer structure this one step transition need just one current source switch switching operation. So thermometer structure can reduce any error to minimize switching operation. By equation (16) this one step change is

$$I_T\left(100_{(2)}\right) - I_T\left(011_{(2)}\right) = I_u + \varepsilon(k) \tag{17}$$

There is no accumulative error in thermometer DAC.

Also thermometer structure intrinsically guarantee data monotonicity. Increase of code value means just adding of current in thermometer coded DAC. In other word code and current always have same tendency even though current cell has mismatch. This means intrinsic monotonicity of thermometer coded DAC. In terms of mismatch, $\varepsilon(k)$ is always larger than $-I_u$. Then

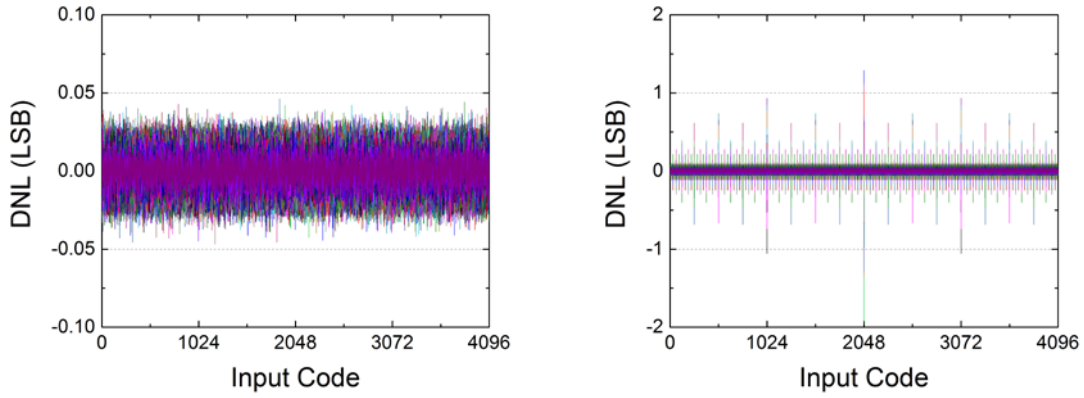
$$I_T(x) - I_T(x-1) = I_u + \varepsilon(x) \geq 0 \tag{18}$$

2.1.3 Segmented DAC.

Thermometer coded DAC has many advantages. There are also many disadvantages like massive digital circuit, poor power efficiency and large layout. Therefore, it's not that much easy to decide to

use which type of DAC. To choose one of these two DAC type, careful analysis is necessary. This thesis refer to analysis method about thermometer coded and binary coded area efficiency in [3].

Very basic performance on DAC operation is linearity. Therefore, INL and DNL analysis is necessary and essential to verify the efficiency of each DAC topologies. Compared basic DAC operation shows each DAC code topology has different linearity specification. Simply in the case of thermometer coded DAC 1step input code transition, just one unit current cell switched on or off irrespective of previous state. Only unit current cell mismatch affect DNL. With an increase in the input code value, unit current cell steadily added. So DNL>-1 because monotonicity is guaranteed. In the other hand in the case of binary coded DAC, number of operation switch affected by previous input state. Especially at the point where the MSB code is changed, the entire switch and majority of unit current cell operates. So majority of unit cell random mismatch error are added up and it affect DNL. Therefore thermometer coded DAC has better DNL performance than binary coded DAC.



(a) (b)

Fig. 13. Overlapped 100times MATLAB DNL simulation result with 0.01LSB standard deviation for (a) Thermometer coded DAC (b) Binary coded DAC

This thesis follows same analyzing method that Lin did in [3] to compare binary and thermometer coded DAC. Two DAC topologies are compared using numerical analysis and MATLAB simulation for obvious performance comparison. Assume unit current cell's current error follows a normal distribution and each unit current cell has 0.01LSB standard deviation. Simulate numerical model 100 times numerical model simulation is done with 12bit resolution DAC model. Fig.13 (a), (b) shows DNL results of thermometer coded DAC model and that of binary coded DAC model. In the case of thermometer coded DAC, DNL is no more than 0.05LSB shown in Fig. 13 (a). But, in the case of binary coded DAC, DNL has very large value at the point where MSB code is changed. Especially near the

midpoint binary coded DAC, DNL is more than 1LSB and it can't guarantee monotonicity. From this result thermometer coded DAC has better DNL than binary coded DAC.

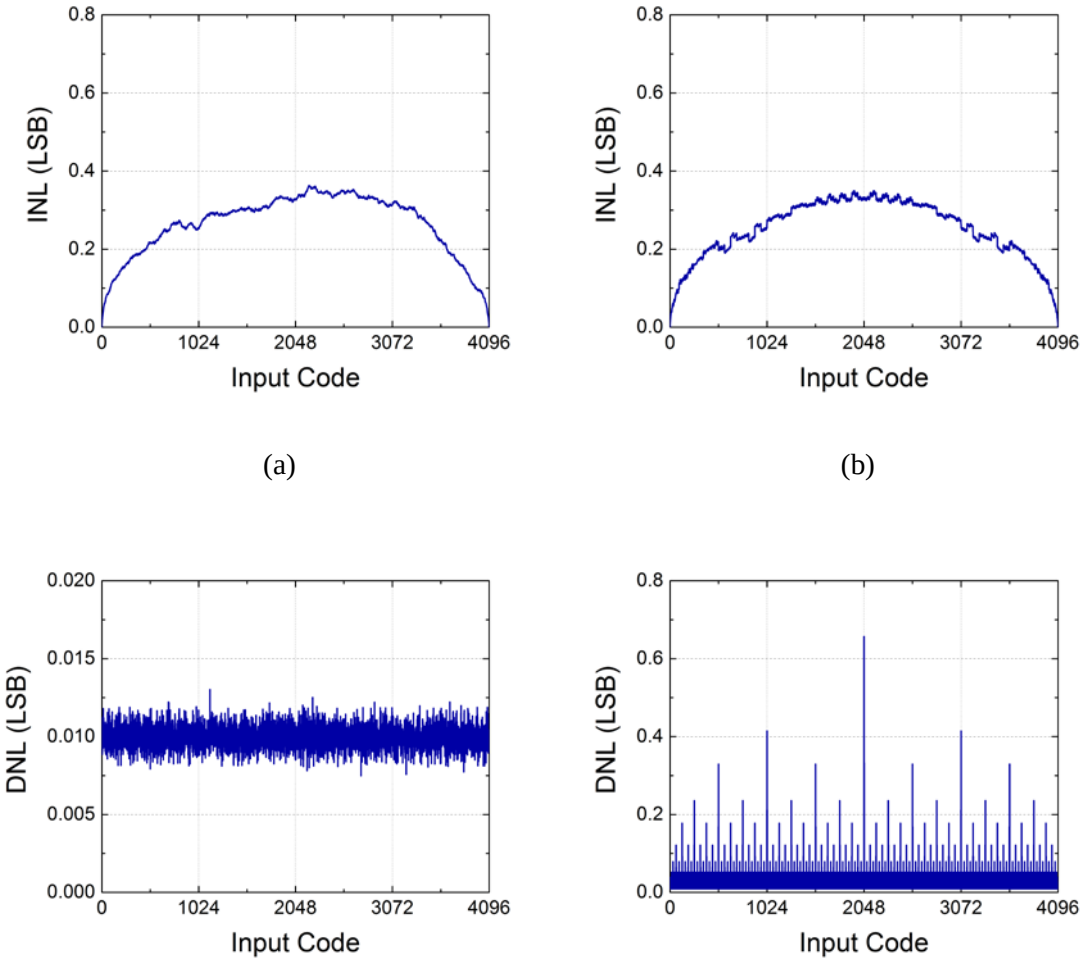


Fig. 14. 100RMS value of (a) INL in thermometer coded DAC, (b) INL in binary coded DAC, (c) DNL in thermometer coded DAC and (d) DNL in binary coded DAC

For clear analysis, each code INL, DNL value convert to 100RMS. This method shows INL and DNL standard deviation. Fig. 13 shows 100times RMS simulation results. Thermometer coded DAC INL and Binary coded DAC INL shown in Fig. 14 (a), (b). INL is increased when many unit cell errors are added. But, because of definition of INL, INL is 0 at each end point. This results are appeared both thermometer coded DAC and binary coded DAC, and both INL distribution is similar.

Fig. 14 shows large DNL difference between thermometer coded DAC and binary coded DAC. Thermometer coded DAC has very small DNL shown in Fig. 14 (c). In the case of thermometer coded DAC, different between adjacent two input code appear as one unit current cell's current. So DNL is same with one unit current cell error. DNL shown in Fig. 14 (c) is 0.01LSB because assume each unit current cell's standard deviation is 0.01LSB. Fig. 14 (d) shows DNL variation of binary coded DAC. In the case of binary coded DAC, number of operating switch is different by previous code. So at the point where near MSB code changed, DNL is increased. DNL shows a similar tendency shown in Fig. 13 (b) and at midpoint DNL has largest variance.

Also numerical analysis show similar result with experimental simulation result. Like the MATLAB simulation, each unit cell's current follow normal distribution and the standard deviation of it is assumed σ.

Whole current cells of N bit resolution DAC are consist of 2^N-1 unit current cells. Let I_o be equal to ideal unit cell's current, $I_u(n)$ is n^{th} unit cell's current, ε is n^{th} unit cell's current error. $I_u(n)$ described as below equation.

$$I_u(n) = I_o + \varepsilon_u(n) \tag{19}$$

But output current description is little bit different as DAC type. When DAC input is k, thermometer coded DAC's total current output $I_T(k)$ is described as below equation.

$$I_T(k) = \sum_{n=1}^{k} I_u(n) = \sum_{n=1}^{k} \left(I_o + \varepsilon_u(n)\right) = kI_o + \sum_{n=1}^{k} \varepsilon_u(n) \tag{20}$$

Using the equation, DNL can be calculated easily.

$$\frac{DNL_T(k)}{LSB} = \frac{I_T(k) - I_T(k-1) - I_o}{I_o} = \frac{\varepsilon_u(k)}{I_o} \tag{21}$$

Like the equation, thermometer coded DAC's DNL is same as each unit cell's current error. Therefore, thermometer coded DAC's DNL is same as normal distribution which unit current's cell's standard deviation σ.

In case of binary coded DAC, there is more difficult calculation process needed. Because DNL is related with number of switching operation, MSB transition point (midpoint input) is most significant point. From (7) and (8), DNL on midpoint input is expressed like below equation.

$$\frac{\mathrm{DNL_B}(2^{N-1})}{\mathrm{LSB}} = \frac{\mathrm{I_T}(2^{N-1}) - \mathrm{I_T}(2^{N-1}-1) - \mathrm{I_o}}{\mathrm{I_o}} = \frac{\varepsilon_{N-1} - \sum_{n=0}^{N-2}\varepsilon_n}{\mathrm{I_o}} = \frac{\sum_{n=2^{N-1}-1}^{2^N-1}\varepsilon_u(n) - \sum_{n=1}^{2^{N-1}-1}\varepsilon_u(n)}{\mathrm{I_o}} \quad (21)$$

Summation of n random variable has n times variance than single random variable. And sign of random variable doesn't relate with summated variance. Therefore standard deviation of binary code DAC DNL is show in (22). Standard deviation of ε_u is σ and standard deviation operator is σ().

$$\sigma\left(\frac{\mathrm{DNL_B}(2^{N-1})}{\mathrm{LSB}}\right) = \sigma\left(\frac{\sum_{n=2^{N-1}-1}^{2^N-1}\varepsilon_u(n) - \sum_{n=1}^{2^{N-1}-1}\varepsilon_u(n)}{\mathrm{I_o}}\right) = \sigma\left(\frac{\sum_{n=1}^{2^N-1}\varepsilon_u(n)}{\mathrm{I_o}}\right) \approx \sqrt{N}\sigma \quad (22)$$

Binary coded DAC has $\sqrt{N}$ times larger standard deviation than thermometer decoded DAC. Binary coded DAC should reduce mismatching variance to fit same DNL requirement with thermometer coded DAC. Relation between area and variance of current cell is described in (9). Variance of current cell is inversely proportional to area of current cell. To fit same DNL requirement, binary coded DAC should increase current cell area.

Table. 1 shows standard deviation of INL and DNL on each DAC structure. Current cell area requirement of 12 bit and N bit DAC also shown in it. Au is unit area which fit the requirement of 0.5LSB in thermometer coded DAC.

		Binary	Thermometer
Standard Deviation	INL	32 σ	32 σ
	DNL	64 σ	1 σ
12 bit	INL=0.5LSB	1024 A_U	1024 A_U
	DNL=0.5LSB	4096 A_U	A_U
N bit	INL=0.5LSB	$0.5\sqrt{N}*A_U$	$0.5\sqrt{N}*A_U$
	DNL=0.5LSB	$\sqrt{N}*A_U$	A_U

Table. 1 Needed current cell area for INL and DNL requirement.

Area requirement for fixed DNL is small for thermometer coded DAC. But actual required area isn't always small for thermometer coded DAC. Area requirement for digital circuits is large to make multi

bit thermometer decoder and massive signal path. Fig. 15 show simple sketch about digital and analog area requirement for thermometer and binary coded DAC.

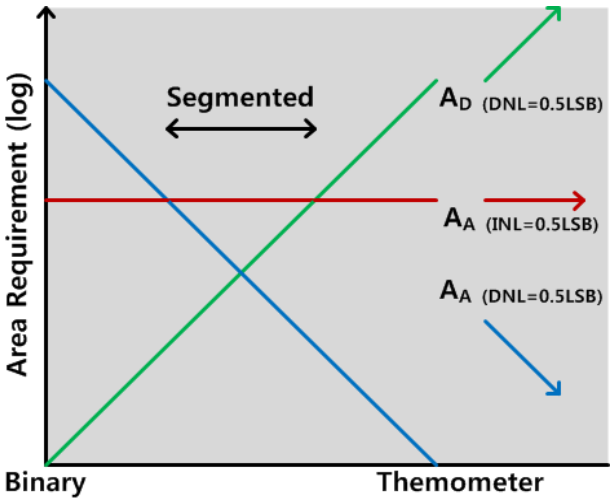


Fig. 15. Digital and analog area requirement for thermometer and binary coded DAC.

Analog area requirement is decreasing as thermometer coded portion is increasing. In contrast, digital area requirement is increasing as thermometer coded portion is increasing. It might be possible to combine both structure to make optimum area requirement DAC. Like this, combining both thermometer and binary coded structure is segmentation. Usually MSB part which dominant for performance is designed as thermometer structure and other LSB part is designed as binary structure. These analysis method from Lin's study [3] easily show the characteristics of segmentation.

2.2 Random Arrangement.

Like above analysis, when using thermometer coded DAC, monotonicity and quite fine DNL are guaranteed. But INL is dominant factor of thermometer coded thermometer coded DAC's performance, because INL is not enhanced. So main objective is INL performance enhancement.

One of the INL's main factors is unit current cell's mismatch error. There are 2 type of mismatch. One is short distance mismatch which is inversely proportional to current cell's area and long distance mismatch which is proportional to distance of each device. In case of short distance mismatch, it can be affordable to improve with larger area of current source, but it isn't effective at limited silicon area. Therefore, gradient (long distance mismatch) error's effect should be decreasing.

Thermometer coded DAC is more vulnerable than binary coded DAC. The reason is using current cell that located in which weighted place, in thermometer coded DAC case. So it is able to degenerate INL because of making overwrapped gradient error which dependent on position.

In case of binary coded DAC, it is affected by gradient error considerably. General binary coded DAC's current cell which assigned to each bit is concentrated on specific location. It becomes degenerated INL vale for a reason to biasing of current cell that using for the characteristic.

2.2.1 Centroid.

Gradient error has more improvement possibility than other random errors, because it has specific direction or regularity. Effect of gradient error can be reduced by using the regularity. INL improvement is purpose of overcoming gradient error. INL is affected by integrated errors. To improve INL, integration sequence which originally accumulate errors change to canceling gradient errors.

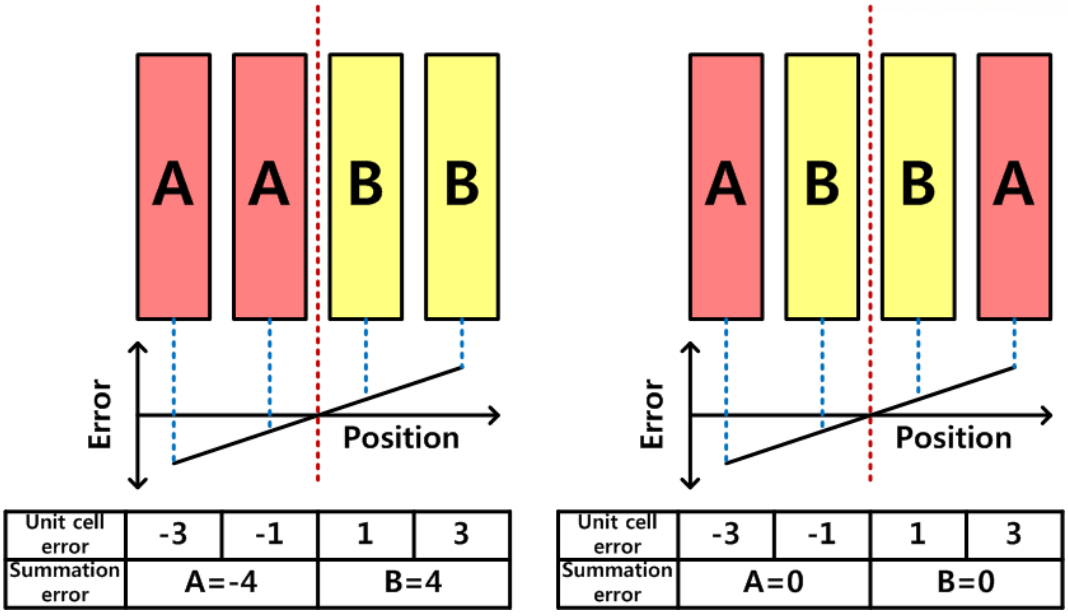
Direction of gradient error means that it has signed value. If unit current cell's errors follow normal distribution has σ value of standard deviation, when add or subtract ε(σ), the errors don't decreasing statistically.

$$\sigma(\varepsilon(\sigma) \pm \varepsilon(\sigma)) = \sigma(\varepsilon(\sqrt{2}\sigma)) \tag{23}$$

But, in case of error which composed of specific sign and value, it can deliver much significant errors by accumulating it. So, it is canceling technique that arrange different signed number gradually to protect increasing error continually.

The centroid arrangement is common skill to decrease gradient error. Foresee cells of midpoint's right and left side have same error value and different sign. Add two cell's offset which located right and left side of Midpoint. It is way that locate cells symmetry in midpoint to decrease gradient error's effect.

Detail explanation about gradient error make show advantage of symmetry layout clearly. Gradient error occur through overall wafer. But single DAC chip using only very small area of wafer. Gradient error through this small local area can be approximated by taylor approximation. First order approximation of it show linear error distribution about x and y axes. This also show perfect symmetry about center point.



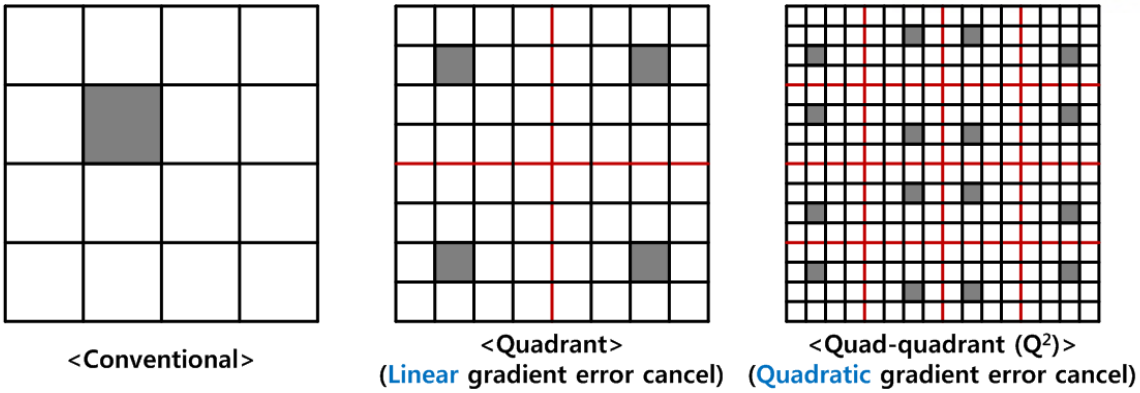
(a) (b)

Fig. 16. Error accumulation of (a) conventional layout and (b) centroid layout

Let's check the difference, giving a one-dimensional example, by sampling one axis as standard. Fig. 16 are conventional arrangement and centroid arrangement respectively. In each cells, error are set from -3 to 3, in proportion to distance from center point. In above case, error of A in common arrangement is -4. On the other hand, error of A in centroid arrangement is zero. As we can know in this example, INL can be improved when cells are arranged symmetrically with origin as the center, by minimizing accumulation of gradient errors.

2.2.2 Quad-quadrant random walk.

In centroid arrangement, first order gradient error can be significantly reduced, cells are located symmetrically. However, when approximate gradient error more accurately, second or higher order error exist. In Taylor approximation, centroid arrangement cannot cancel out error even for Taylor second order approximation. "Quad-quadrant (Q^2) Random Walk" is the technique, from art-of-the-stage [17], to cancel out these high order errors.

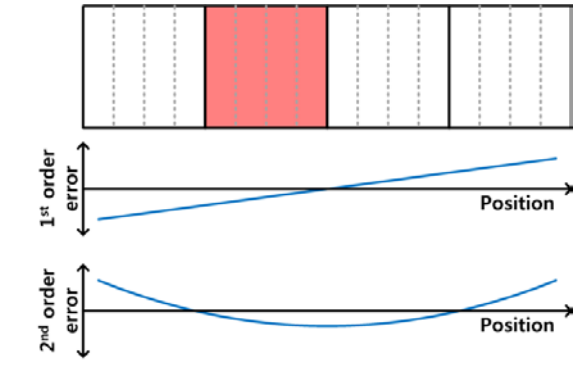


(a) (b) (c)

Fig. 17. Current source layout implementation. (a) Single unary current source. (b) Current source split in to quadrant and connected in parallel. (c) Current source split into quadrant twice and connected in parallel.

Fig. 17 shows different current source splitting layout. Fig. 17 (a) is conventional unary current source arrangement. This shape current cell suffer from gradient error too much. Fig. 17 (b) show current source arrangement with splitting current source by quadrant. This structure can degenerate first order gradient error by adding symmetrically arranged current cell. But higher order gradient error still remain. Fig. 17 (c) show current source split twice into quadrant. This structure degenerate first order gradient error in first quadrant division and higher order gradient error decrease in second quadrant division. This twice division into quadrant is called quad-quadrant.

Fig. 18 show detail example about quad-quadrant current cell arrangement. Example is simplified into one dimension case. 1^{st} and 2^{nd} order errors are linear and quadratic gradient error. It compare accumulated error on red boxed current cell. Fig. 18 (a) show gradient error accumulation for conventional unary current cell. Both first order and second order gradient errors are accumulated without cancelation. First order split current cell in fig. 18 (b) degenerate first order gradient error by symmetric arrangement. But second order error are just accumulated because symmetric current cells still have same sign of second order gradient error. Quad-quadrant structure on fig. 18 (c) degenerate second order gradient error also. At point of second division axis, second order gradient error again can be split by first order term and other higher order term. Degeneration of first order gradient error on second axis also reduce original second order gradient error.

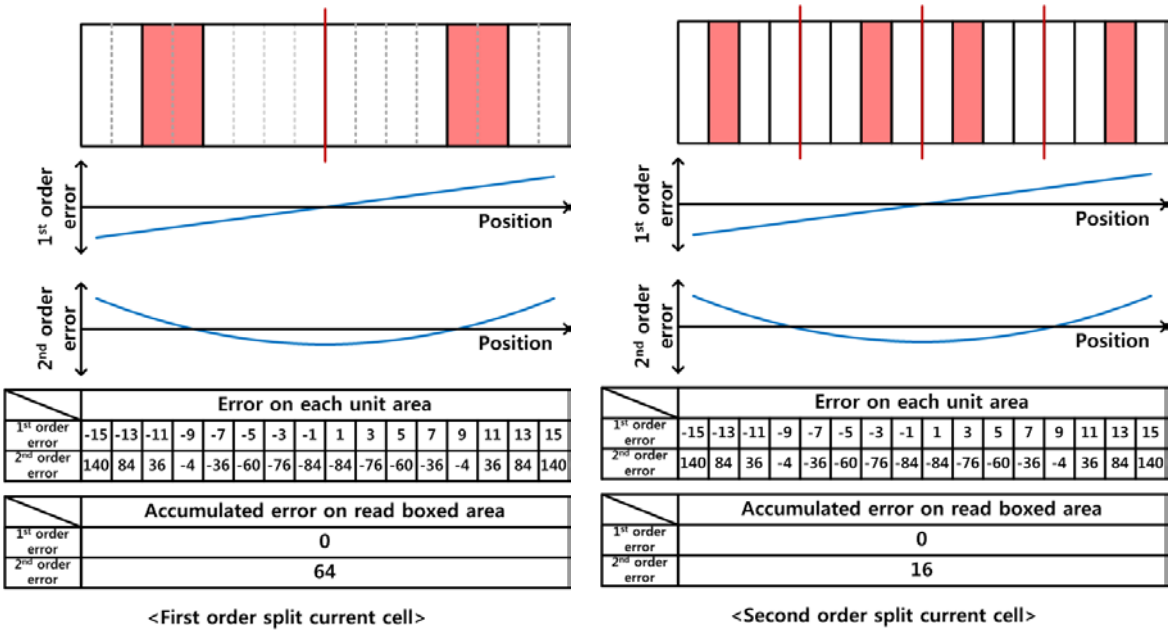


	Error on each unit area															
1st order error	-15	-13	-11	-9	-7	-5	-3	-1	1	3	5	7	9	11	13	15
2nd order error	140	84	36	-4	-36	-60	-76	-84	-84	-76	-60	-36	-4	36	84	140

	Accumulated error on read boxed area
1st order error	-16
2nd order error	-256

<Conventional unary current cell>

(a)



	Error on each unit area															
1st order error	-15	-13	-11	-9	-7	-5	-3	-1	1	3	5	7	9	11	13	15
2nd order error	140	84	36	-4	-36	-60	-76	-84	-84	-76	-60	-36	-4	36	84	140

	Accumulated error on read boxed area
1st order error	0
2nd order error	64

<First order split current cell>

	Error on each unit area															
1st order error	-15	-13	-11	-9	-7	-5	-3	-1	1	3	5	7	9	11	13	15
2nd order error	140	84	36	-4	-36	-60	-76	-84	-84	-76	-60	-36	-4	36	84	140

	Accumulated error on read boxed area
1st order error	0
2nd order error	16

<Second order split current cell>

(b) (c)

Fig. 18. First and second order gradient error accumulation in one dimension example. (a) Conventional unary current cell (b) First order split current cell (c) Second order split current cell

But, even each cell is arranged as above, gradually turned on divided unit current cells also can cause accumulation of gradient error. Therefore, to minimize these accumulations, switching sequence that current cells operate is arranged randomly. This method is called as “Quad-Quadrant Random Walk” in [17].

Considering first order gradient error by 4x4 current cells, if adopt switching sequence minimizing accumulation, INL goes up and down, not getting out of center value. In this way, maximum value of INL is highly reduced.

Random walk switching sequence is also appeared in [17]. These switching sequences are hierarchically constructed twice as fig. 19. “0” cells are operate from A to P in alphabetical order. And next “1” cells are operate from A to P in alphabetical order. All current cell operate A to P and "0" to "15" like this sequence. In this way, accumulation of global gradient error can be reduced and at the same time, detailed gradient error accumulation of 0 to 15 can be also reduced.

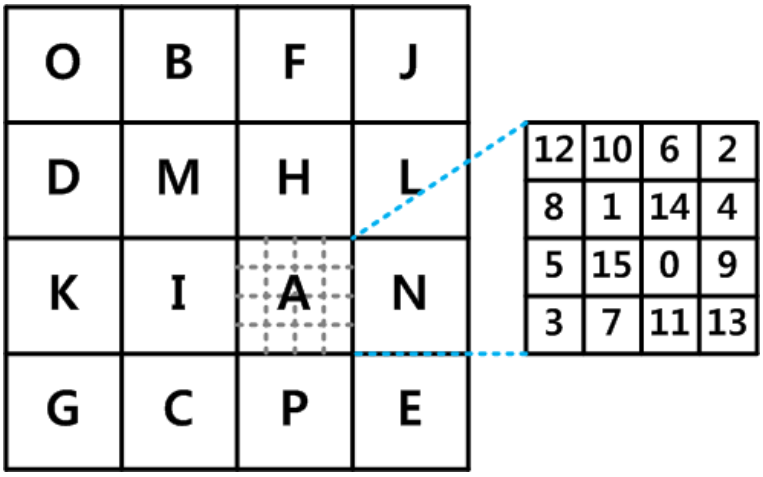


Fig. 19. Random walk arrangement.

2.3 Dynamic Element Matching.

As explained in previous chapter, one of the most important error sources is mismatch of current sources. There are various sources of mismatch like doping concentration, transistor size process variation. So it's almost impossible to compensate or eliminate all source of mismatch. On the other way, performance of DAC can be improve in opposite direction. DAC error can be corrected not only from source of error but also from resulted output.

With many sources of errors, each current cell has their own mismatching errors. To eliminate this matching error, one possible way is averaging as shown in fig. 20. Even if every current cell has mismatch, average current is almost same with ideal current because averaging decrease random variation. It is basic concept of dynamic element matching (DEM).

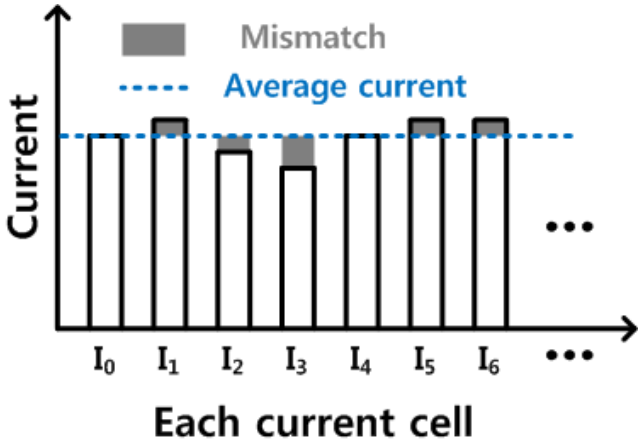


Fig. 20. Mismatch of current cell and average current.

DEM make DAC randomly select current cell at every clock. Then current changes in every cycle. Average this changing current become similar with intended output.

DEM doesn't need additional current cell. It just blend and randomly select current cell among original current cells. In every clock, current cells are selected regardless of position which related with gradient error and other mismatch sources. Then all error are degenerated regardless of source.

When DAC operate in dynamic operation, current cell mismatch appear as spurs which shown in fig. 10. Reason why mismatch appear as spurs is that mismatch are input code dependent. In conventional DAC, output frequency is constructed depend on input data. But resulted output by mismatch also make some frequency because all mismatch associated with input code. DAC need some repeated input to make specific frequency. Then this repeated input also make unwanted spurs associated with mismatch.

DEM remove connection between input code and mismatch. Mismatch independent with input data appear randomly. It means specific frequency signals by mismatch are eliminated.

Chapter III

Proposed High Voltage Protection

3.1 Industrial Application DAC.

Industrial field is one of most common application area for DAC. Use of DAC improve system accuracy, functionality and controllability in the industrial application. DAC provide simple way to apply processed digital signal to industrial applications with analog signal. However, conventional DAC can't be directly applied to industrial applications. There are several requirements for industrial application DAC.

In the industrial area, various supply voltages are accessible like 15V and 5V. Diverse devices and instruments are also used. Most of industrial application devices are required to drive large external load with 10V swing. Requirement of current driving is commonly 20 mA.

	Current requirement	Voltage requirement
Current driver	20mA	-
Voltage driver	-	10V
Current/voltage driver	20mA	10V

Table. 2. Current and voltage driver requirement in the industrial application.

Table. 2 shows common current and voltage driving requirements for industrial applications. Scale of these current and voltage driving requirements are quite larger than current and voltage used in conventional fine process digital or analog CMOS integrated circuit(IC). Most of current steering type DAC satisfy 20mA current driving requirement without difficulty. 10V swing requirement isn't that much easy.

In conventional CMOS process, MOSFET operation voltage is lower than 5V. Some fine process CMOS transistor operation voltages is about 1~2V. It's too much lower than industrial application requirements. Special transistor that operate in high voltage like laterally diffused metal oxide

semiconductor (LDMOS) and drain extended metal oxide semiconductor (DEMOS) is necessary to operate in industrial voltage requirement.

But, these high voltage transistors usually have complex structure that using larger area than conventional MOSFET. Additional processes which consume much cost are also needed to fabricate high voltage transistors. Because of these reasons, designing whole DAC with these high voltage transistor is expensive. High voltage transistors have different properties and shapes to conventional MOSFET. Because of it, whole DAC should be redesigned even though conventional low voltage DAC design is exist.

To overcome these problem, conventional industrial DAC use driving amplifier. Fig. 19 shows simplified structure of it. This structure using driving amplifier which made up with high voltage transistors. It can reuse existing low voltage DAC and using much smaller high voltage transistor than DAC which change whole transistor with high voltage transistors while satisfying industrial high voltage requirements.

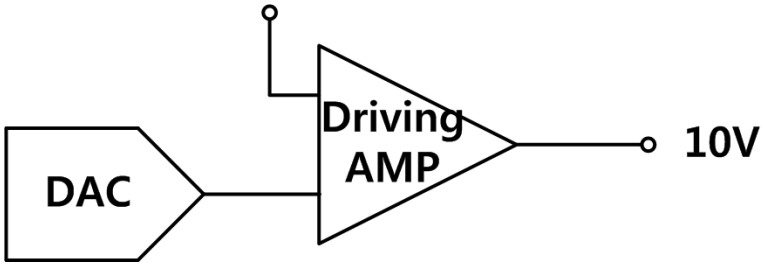


Fig. 21. Conventional industrial high voltage DAC structure.

But, this structure still has disadvantages. It use both DAC and driving amplifier that require area and power consumption. And, driving amplifier still using many high voltage transistors. Additionally, driving amplifier also has their own distortion because it's not ideal amplifier.

3.2 Proposed High Voltage Protection Structure.

High voltage protection structure is proposed to use DAC in high voltage condition that satisfy industrial application requirement while solving other problems in conventional high voltage DAC structure.

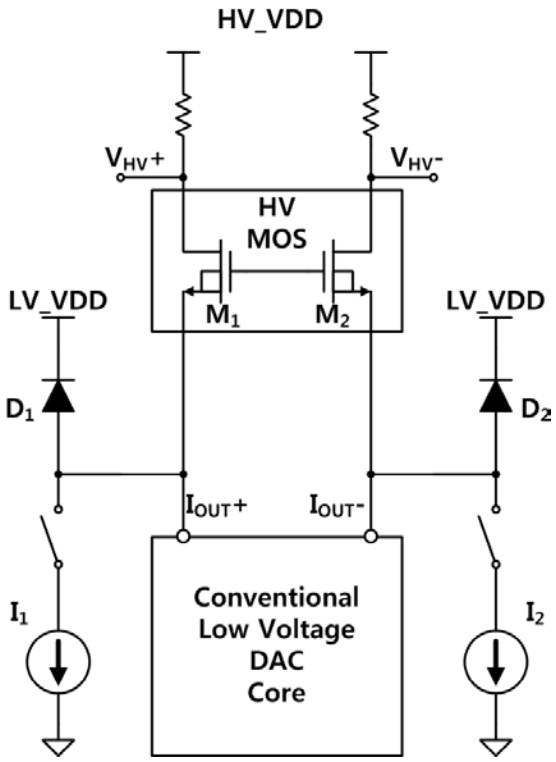


Fig. 22. Proposed high voltage projection structure current steering DAC

Fig. 22 shows brief schematic of proposed high voltage protection DAC. It use conventional low voltage DAC core and simple high voltage protection circuits are added. Fig. 23 is basic structure of conventional low voltage DAC with differential current output used in high voltage protection DAC.

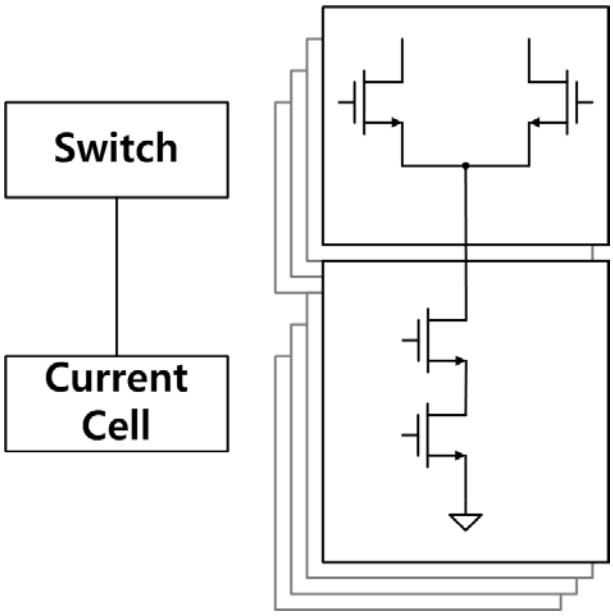


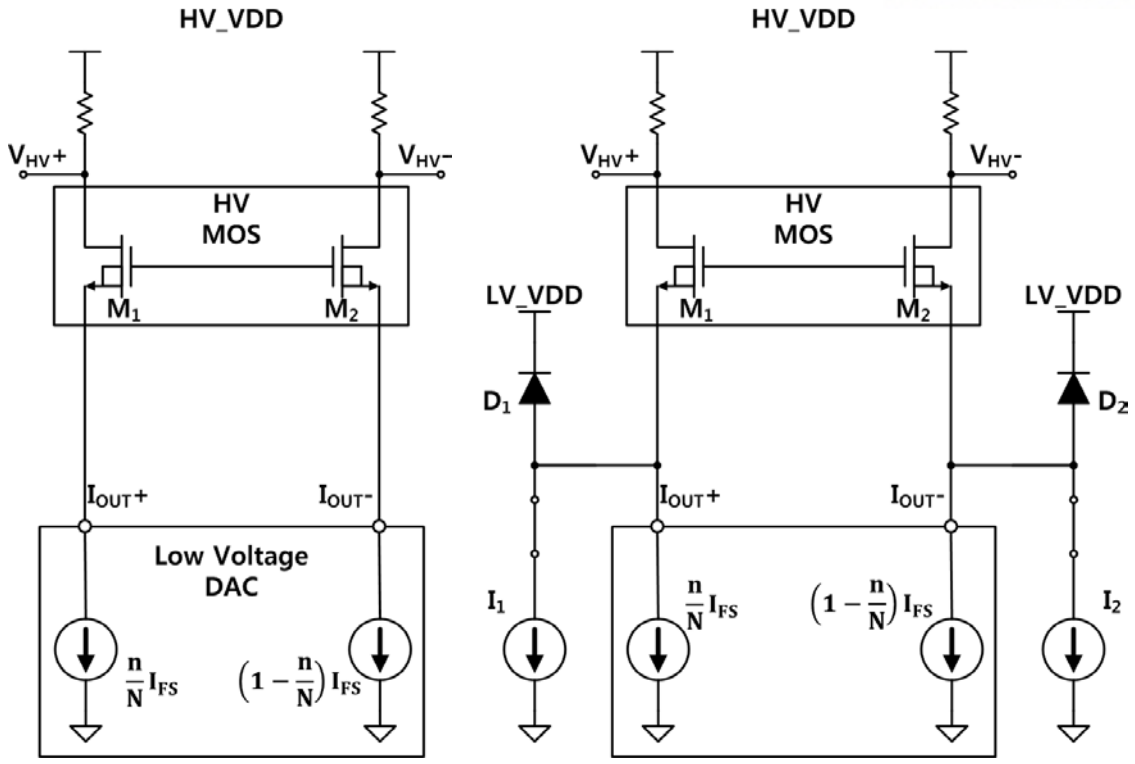
Fig. 23. Simplified structure of differential current steering DAC.

Proposed high voltage protection circuit is composed of high voltage transistors, diodes, switches and bleeding current sources. In fig. 22, two high voltage transistors (M_1 and M_2) are used to prevent that output high voltage flow into low voltage DAC current output node (I_{OUT}+ and I_{OUT}-). If gate of high voltage metal oxide semiconductor transistor (HV MOS) was biased properly, sources of M1 and M2 (which are same as I_{OUT}+ and I_{OUT}- node) is protected from drain voltage of HV MOS (V_{HV}+ and V_{HV}-). V_{HV}+ and V_{HV}- is usually higher voltage than conventional MOSFET's operation voltage. But, most of exceeded voltage is blocked as a drain source voltage of HV MOS which has high drain source breakdown voltage.

Simple high voltage cascading transistors aren't enough to protect conventional low voltage current DAC from output high voltages (V_{HV}+ and V_{HV}-). Fig. 24 (a) show simplified structure with only HV MOS. I_{FS} is full scale output current, N stands for total number of current source and n is input digital code. With n≈N, M_1 flow almost full scale current and it operate in saturation region which means I_{OUT}+ node stay in acceptable low voltage region. If n decreased to almost 0, current of M_1 decrease and gate source also decrease. But size of M_1 is large enough to flow full scale current, leakage current also very large. With very small n, current flow through M_1 is scale of subthreshold leakage current. It means I_{OUT}+ voltage increase to voltage that make M_1 fall into subthreshold region. Increased voltage may damage the low voltage DAC.

Proposed structure is shown in Fig. 24 (b). Additional bleeding current sources I_1 and I_2 are connected to I_{OUT}+ and I_{OUT}- node. These additional current sources are sinking subthreshold leakage current of HV MOS. By sinking leakage current of HV MOS, it prevent voltage increasing at I_{OUT}+ and I_{OUT}- node. With these bleeding current sources and HV MOS, input code independent high voltage protection is guaranteed.

Diode D_1 and D_2 are connected to lower the risk of sudden high voltage spike feedthrough. Feedthrough inside low voltage DAC isn't that much crucial because all signals inside low voltage core is smaller than operation voltage of conventional transistor and feedthrough voltage isn't also that much different with operation voltage of conventional transistor like clock feedthrough. But signal at high voltage node is usually much larger than operation voltage of conventional transistor. Feedthrough voltage from high voltage node also can be much larger than operation voltage of conventional transistor. This large voltage feedthrough might dangerous for low voltage transistor circuits. D_1 and D_2 are placed at the connection between low voltage circuit and high voltage circuit. It absorb spike shape feedthrough voltage. If I_{OUT}+ and I_{OUT}- nodes was connected to the pad of chip, D_1 and D_2 can be replaced with pad diode.



(a) (b)

Fig. 24. Proposed high voltage protection DAC with (a) only HV MOS and (b) additional bleeding current source.

3.3 Advantage of Proposed Structure.

3.3.1 Simplest way to convert low voltage DAC to high voltage DAC.

Proposed high voltage protection structure DAC is the simplest structure that convert low voltage current steering DAC to high voltage current steering DAC. In 3.1, other method that construct industrial high voltage DAC is already mentioned. One is designing whole DAC with high voltage transistor and other is adding additional high voltage driving amplifier. Proposed structure is simpler than others.

Number of high voltage transistor is one big difference of proposed structure. High voltage transistor need more special process than conventional transistor. Cost of high voltage transistor is much expensive because of it. In other words, using high voltage transistor is costly process. Structure that construct whole current steering DAC with high voltage transistor usually need more than thousands high voltage transistor. This structure is scarcely used because of cost. Combined structure of low

voltage DAC and high voltage driving amplifier uses high voltage transistor only on driving amplifier. Usually driving amplifier uses tens of high voltage transistor. Therefore, it's much cheaper than previous structure and easy to convert existing low voltage DAC to high voltage DAC. Because of these advantage, it's most common structure in industrial DAC.

Proposed structure uses only two high voltage transistor. It's smallest number to construct high voltage DAC. In addition to decrease of costly high voltage transistor, proposed structure doesn't need additional power by using both DAC and driving amplifier. It only consume current at the current steering DAC core and some current for bleeding current. Additional HV MOS doesn't affect output current of DAC. Proposed high voltage protection structure has advantage of both cost and power consumption.

3.3.2 Nonlinearity compensation by proposed structure.

Improving linearity is one of most important point when designing DAC. But driving amplifier combined structure has poor linearity performance than original low voltage DAC. Driving amplifier has its own distortion. Signal of combined structure is distorted by both conventional low voltage DAC nonlinearity and driving amplifier distortion.

On the contrary to combined structure, proposed high voltage protection structure even improve nonlinearity of low voltage DAC. As explained in previous chapter, current steering DAC has intrinsic code dependent nonlinearity by finite output impedance of current cell. Most current cell in current steering DAC is composed of transistor. MOSFET current cell has finite output impedance because of channel length modulation.

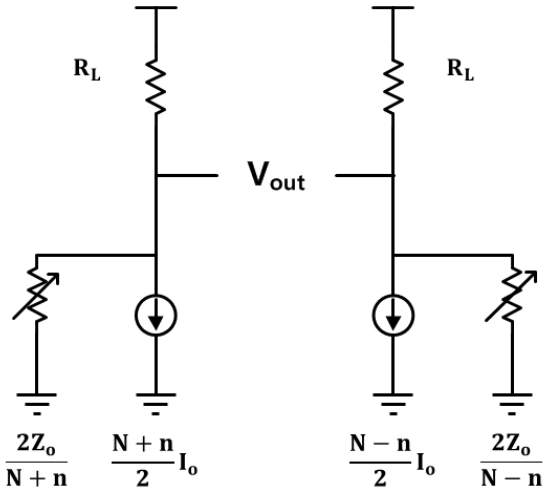


Fig. 25. Code dependent DAC output impedance.

Finite output impedance of transistor brings code dependent output impedance change. Analysis about effect of finite output impedance in this thesis base on [4]. Fig. 25 shows code dependent output impedance. Current of unit current cell is I_o, output impedance of each cell is Z_o, total number of unit current cell is N and data input is n ($-N \leq n \leq N$). Parallel connection of current has total current

$$\frac{N+n}{2} I_o \, , \frac{N-n}{2} I_o \tag{21}$$

and output impedance

$$\frac{2Z_o}{N+n} \, , \frac{2Z_o}{N-n} \tag{22}$$

With output load R_L, differential signal output V_{out} after taylor approximation is expressed as following.

$$V_{out} \fallingdotseq R_L N I_o \left[\left(\frac{n}{N} \right) + \left(\frac{n}{N} \right)^3 \left[\frac{R_L N}{2Z_o} \right]^2 \right] \tag{23}$$

For full swing signal (n=N), third order harmonic distortion (HD3) is following.

$$HD3 \fallingdotseq \left[\frac{R_L N}{4Z_o} \right]^2 \tag{24}$$

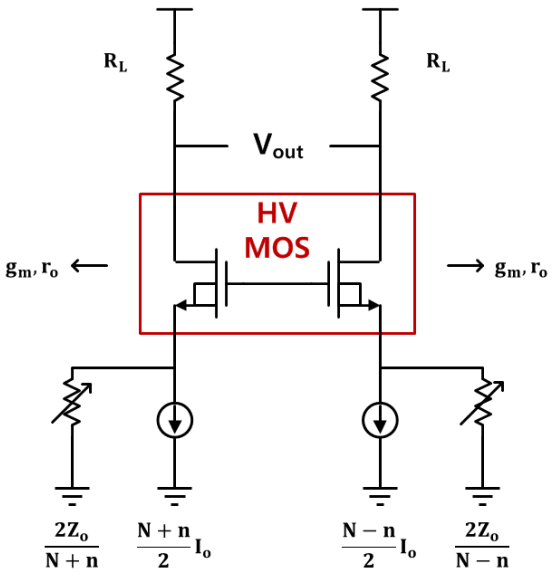


Fig. 26. Code dependent DAC output impedance with high voltage protection.

Fig. 26 show code dependent output impedance of proposed high voltage protection DAC. Transconductance and output impedance of HV MOS are g_m and r_o. HV MOS function as another cascode stage of current source. It increase output impedance of current source seen at the V_{out} node.

This cascode HV MOS reduce effect of code dependent output impedance. If g_m and r_o were similar in both side HV MOS, V_{out} and HD3 are expressed as following.

$$V_{out} \fallingdotseq R_L N I_o \left[\left(\frac{n}{N}\right) + \left(\frac{n}{N}\right)^3 \left[\frac{N}{2g_m Z_o}\right]^2\right] \tag{25}$$

$$HD3 = \left[\frac{N}{4g_m Z_o}\right]^2 \tag{26}$$

In case of $\frac{1}{g_m} < R_L$, distortion by code dependent output impedance dcreases. This condition imply that voltage swing at the output node is larger than voltage swing at the souece of HV MOS. It shown in Fig. 27. For similar swing of current, voltage swing represent difference of effective impedance $\frac{1}{g_m}$ and R_L. Large swing at output node shows $\frac{1}{g_m} < R_L$.

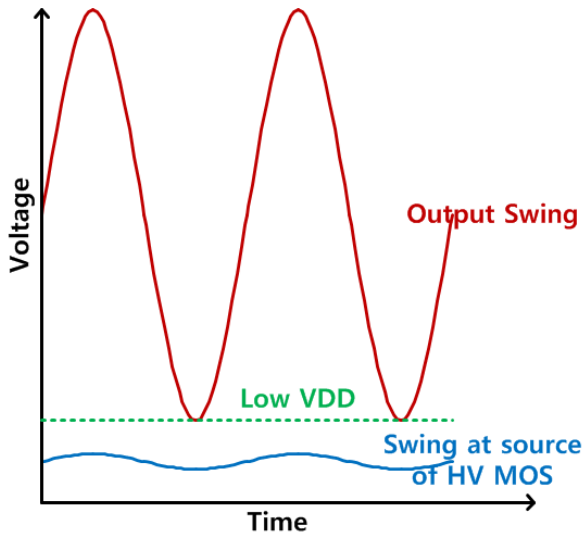


Fig. 27. Voltage swing at output node and source of HV MOS.

However tansconductance g_m maybe change as current flow through HV MOS change. For increasing current, g_m also increase. It means effective impedance seen at source of HV MOS is decreasing as output current increase. In other word, change of transconductance partially compensate code dependent output impedance change.

3.3.3 Power efficiency.

Conventional current steering DAC has cascode MOSFET structure like at output node as shown in Fig. 23. Each of cascode MOSFET need voltage drop to operate properly. This voltage drop make continuous power loss.

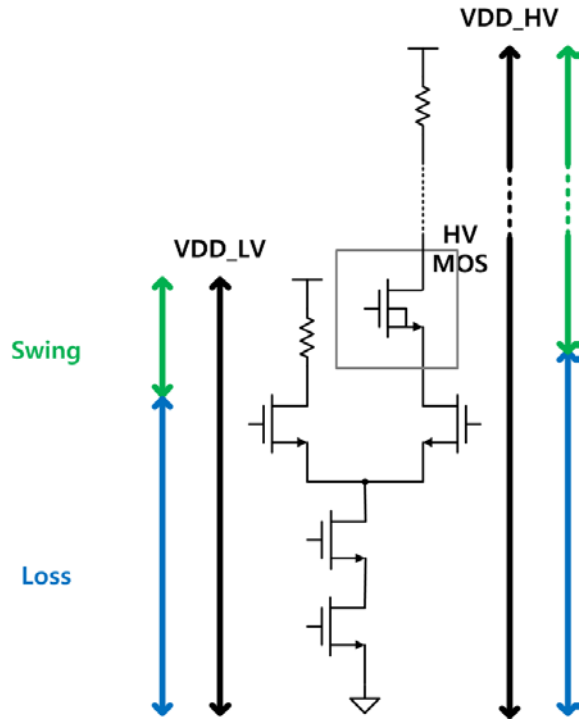


Fig. 28. Output possible swing range for low and high voltage.

Power efficiency is determined by ratio between output power on output load and loss power on DAC current cell. Output power depends on output voltage swing range. Possible output swing range is limited by voltage drop of current cell. DAC which operate in low voltage has small possible output swing range because decreasing voltage drop on current cell is difficult. One possible way to increase output swing range is increasing supply voltage. As shown in fig. 28, increased supply voltage is added to possible output swing range. Proposed high voltage protection structure increase possible output swing range by increasing supply voltage. Even though additional HV MOS need voltage drop, it is much smaller than increased supply voltage. Ratio between possible output swing and supply voltage increase.

Fig. 29 shows how much power efficiency is increasing by increase of output swing range. Power efficiency is power consumed on load by total power and output swing range is possible output swing by supplied voltage. Graph show linearly increasing power efficiency.

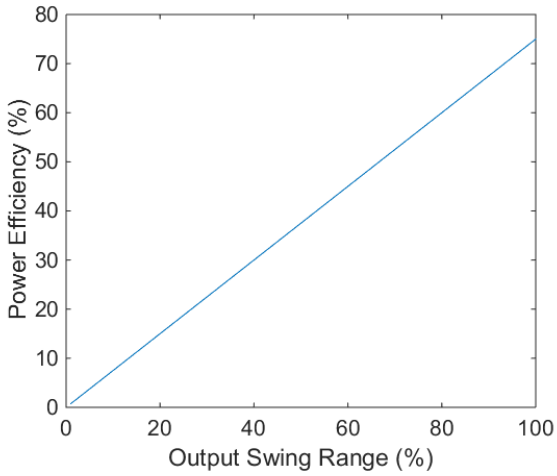
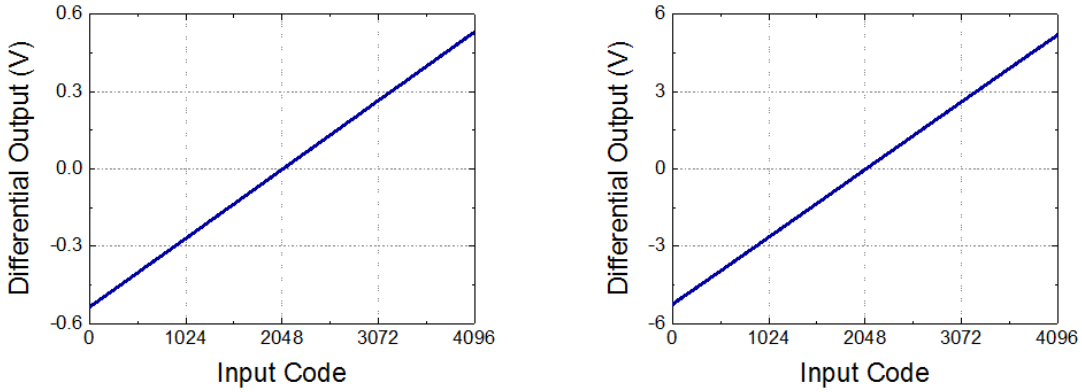


Fig. 29. Power efficiency depend on output swing range

3.4 Test Result.

Prototype of proposed high voltage protection was tested. Prototype tested over 10V condition and operate well.

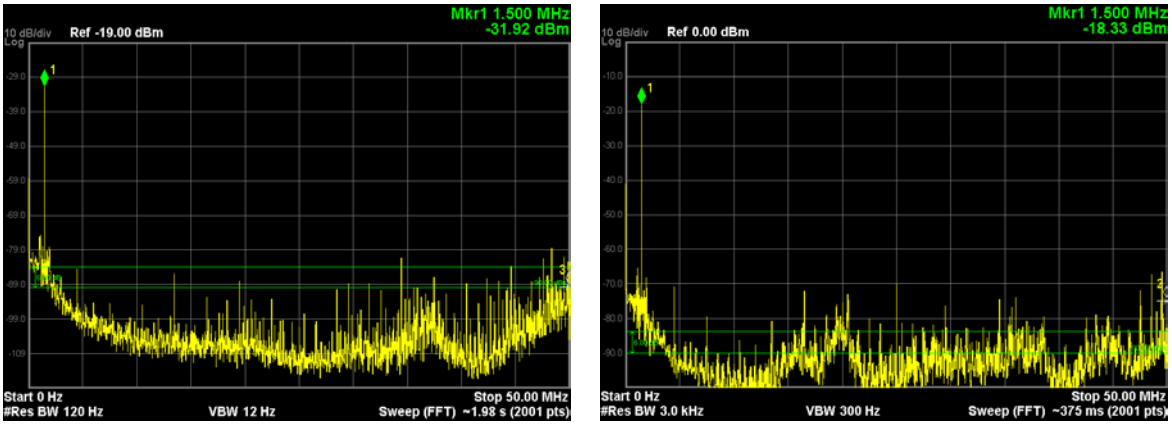


(a) (b)

Fig. 30. Differential output voltages of (a) low voltage mode DAC and (b) proposed high voltage mode DAC.

Fig. 30 show differential output voltage of low voltage mode DAC and proposed high voltage protection mode. Both high voltage mode and low voltage mode DAC has similar shaped differential

output. Low voltage mode DAC has only 1V peak to peak voltage swing. But high voltage protection mode DAC has 10V peak to peak output voltage swing.



(a) (b)

Fig. 31. Output frequency spectrum while desired output frequency is 1.5MHz and sampling speed of 100MS/s. (a) Low voltage mode output spectrum (SFDR = 43dB) (b) Proposed high voltage protection structure output spectrum (SFDR = 47.5dB).

Fig. 31 is output spectrum of both low voltage mode and high voltage mode DAC. Input code of DAC is 1.5MHz sine wave and sampling speed is 100MS/s. Original low voltage mode output spectrum shows 43dB SFDR. Output spectrum of proposed high voltage protection structure shows 47.5dB SFDR. Proposed high voltage protection structure has better SFDR. It represent high voltage protection structure has better performance than conventional low voltage structure.

Chapter IV

Current Steering DAC with Resolution Improving Sigma-delta modulation

4.1 Sigma-delta Modulation Noise Shaping.

4.1.1 Sigma-delta modulation.

Sigma-delta (∑Δ) modulator changes the spectrum of noise. By adding, subtracting or integrating of signal, it can reduce low frequency noise. Then signal to noise ratio (SNR) on the low frequency region increase. Oversampling ∑Δ DAC is designed with this property. ∑Δ DAC is briefly explained on chapter 1.

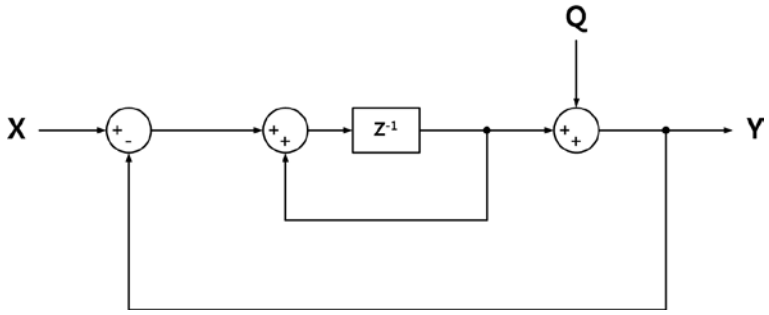


Fig. 32. First order sigma-delta modulator.

Fig. 32 shows first order ∑Δ modulator. Q stands for quantization noise, X represents input and Y represents output. In Z domain,

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z) \quad (27)$$

As shown in (27), ∑Δ modulator has different signal transfer function (STF) and noise transfer function (NTF). STF and NTF are

$$STF = z^{-1} \quad (28)$$

$$NTF = 1 - z^{-1} \quad (29)$$

This first order ∑Δ modulator has delay STF and high pass filter NTF. With this high pass filtering NTF, ∑Δ modulator make high resolution ADC and DAC.

4.1.2 Combining between current steering DAC and sigma-delta modulator.

Contrary to ∑Δ DAC, current steering DAC has fast sampling speed. But it's hard to improve resolution because of matching problem. To increase resolution, current steering DAC should add lots of transistor and need much area. This thesis try to find another way to increase resolution of current steering DAC.

One possible way is combining ∑Δ modulator and current steering DAC. ∑Δ DAC has advantage of high resolution and current steering DAC has speed advantage. Combining both advantage can possible way to increase performance.

In detail, current steering DAC has resolution limitation by current cell mismatch. Current steering DAC usually has 10 bit or slightly higher resolution because of mismatch limitation. Most of DAC structures also has limited resolution by matching property. However ∑Δ DAC is freer from matching limitation than other DAC structure. Usual ∑Δ DAC has more than 20 bit resolution. As a result ∑Δ modulator is good candidate for improving resolution without their own mismatching limitation. It also easy to implement because most components of ∑Δ modulator are digital circuit.

From different point of view, ∑Δ DAC has high resolution but speed is limited by oversampling. To increase speed of ∑Δ DAC, oversampling requirement should be reduced. Using multi-bit current steering DAC can decrease oversampling requirement. In this way, ∑Δ DAC might increase the speed.

4.2 Proposed Current Steering DAC with Resolution Improving Sigma-delta Modulator.

4.2.1 Proposed resolution improving current steering DAC basics.

Fundamental structure of proposed DAC is simply combination of ∑Δ modulator and conventional current steering DAC. N-bit resolution proposed DAC only using M-bit resolution current steering DAC which has lower resolution than intended N-bit (N>M). Resolution difference (N-M) is compensated by ∑Δ modulator which decreasing low frequency quantization noise. Simplified block diagram of proposed DAC is shown in fig. 33.

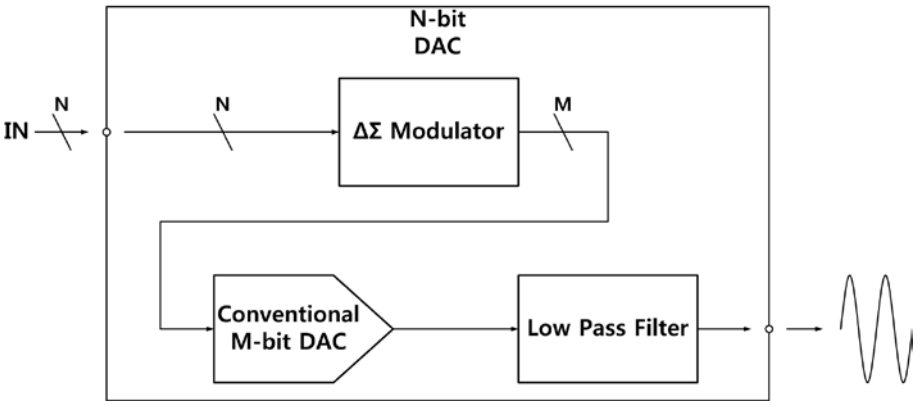
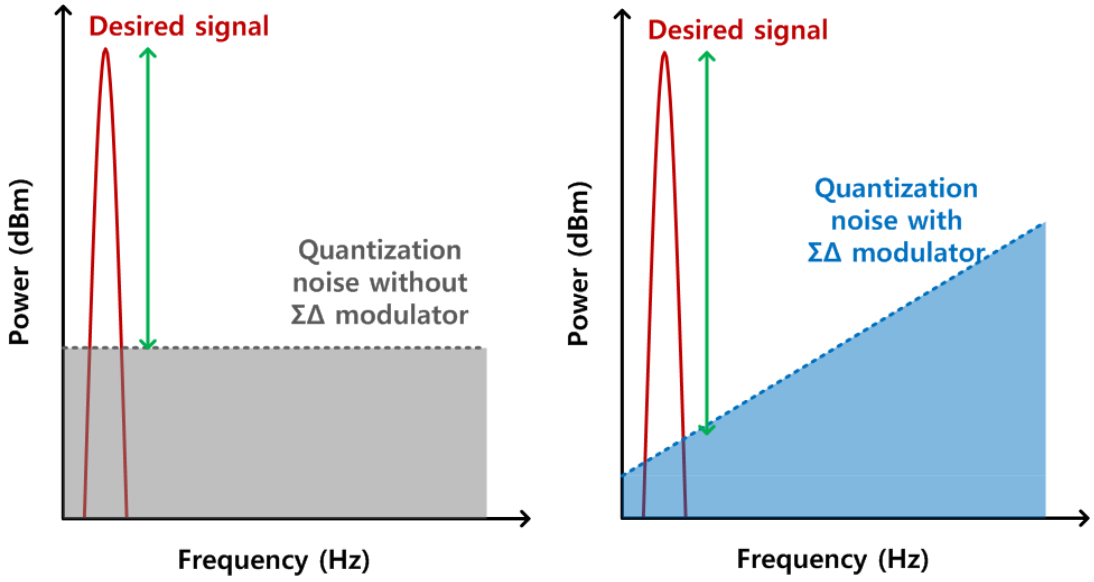


Fig. 33. Block diagram of proposed resolution improved DAC

It looks similar with multi-bit ∑Δ DAC [7]. But multi-bit ∑Δ DAC just use 2~3 bit (low resolution) DAC to improving ∑Δ modulator operation. But proposed structure use conventional current steering DAC with 10 bit or higher resolution DAC. This current steering DAC has enough performance to operate without ∑Δ modulator. And also linearity compensation technique also applied.



(a) (b)

Fig. 34. Output spectrum of DAC (a) without ∑Δ modulator and (b) with ∑Δ modulator.

Sigma delta modulator is used for noise shaping (high pass filtering). This noise shaping make resolution improvement. Fig. 34 shows effect of noise shaping. Original quantization noise exist in overall frequency like fig. 34 (a). ∑Δ modulator moves this unwanted noise to the high frequency

spectrum like fig. 34 (b). Ratio between desired signal power and noise power in low frequency increase after ∑Δ modulation. Resolution of modulated DAC looks improved in low frequency.

4.2.2 Implemented structure of resolution improving sigma-delta modulation current steering DAC.

In real implementation of proposed DAC, not all of input data (N bit) but improved LSB data (N-M bit) need to be modulated. The reason why ∑Δ modulator need is quantization. Therefor M bit data doesn't need ∑Δ modulation because already M bit current cells are assigned. Just improved resolution (N-M bit) data suffer from quantization and should be expressed with upper bit current cell. Therefore small bit sigma delta modulator is enough. ∑Δ modulator need N-M bit + overflowing bit (O bit). Fig. 35 is modified block diagram with overflowing bit O.

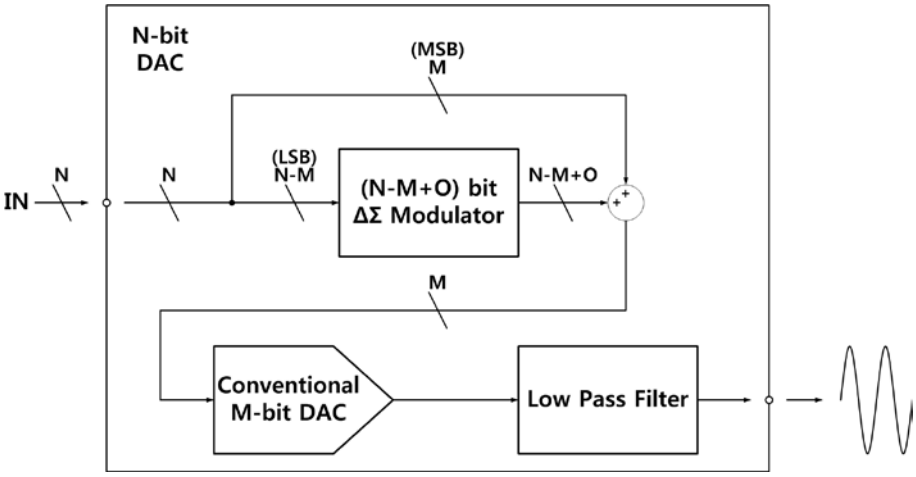


Fig. 35. Block diagram of proposed DAC with smaller ∑Δ modulator.

Core M-bit conventional DAC is also important. If core M-bit DAC has already lots of error, ∑Δ can't compensate that error. ∑Δ modulator changes only few LSB bit on core DAC. Therefore ∑Δ improving LSB related performance by LSB randomized noise shaping. Proposed structure also need MSB related performance improving technique. They are DEM and Q^2 random walk from art-of-the-state [17], [19].

DEM and Q^2 random walk are MSB related randomization and ∑Δ modulation is LSB related randomization for improving performance. By combine both LSB randomization and MSB randomization, overall DAC performance can be increased. Fig. 36 is MSB LSB randomization DAC block diagram.

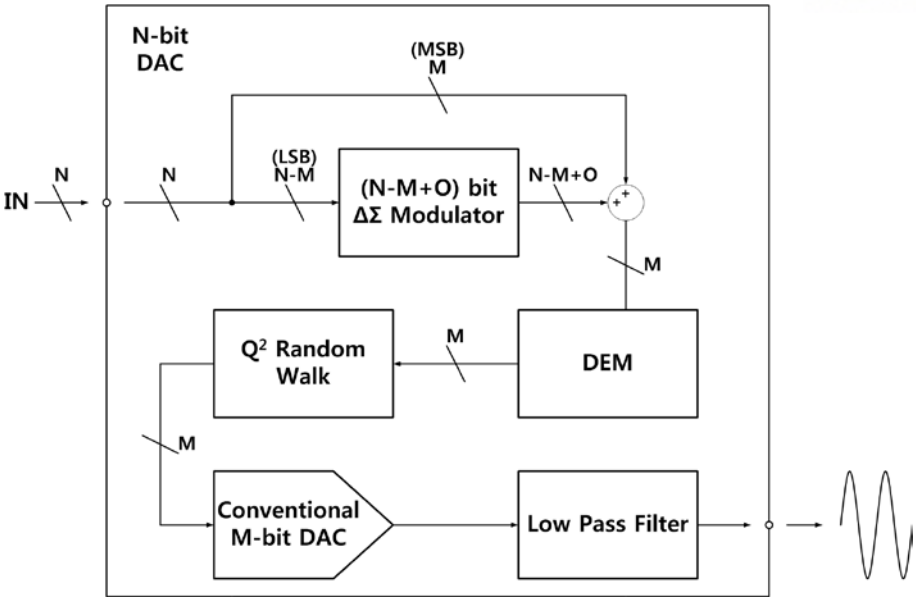


Fig. 36. Block diagram of proposed DAC which combine both MSB and LSB randomization technique.

Sigma-delta modulator that used for testing proposed structure is second order modulator in Fig. 37.

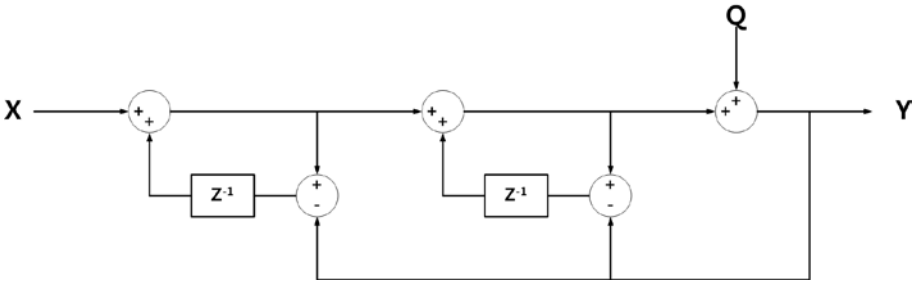


Fig. 37. Second order ∑Δ modulator.

Modulator output and transfer function are following.

$$Y(z) = X(z) + (1 - z^{-1})^2 Q \tag{30}$$

$$STF = 1 \tag{31}$$

$$NTF = (1 - z^{-1})^2 \tag{32}$$

It has no effect on input signal. But quantization noise has second order high pass filtering transfer function. It can reduce low frequency quantization noise directly.

4.3 Advantage of Proposed structure.

4.3.1 Resolution increasing.

Proposed structure easily increase resolution by adding additional ∑Δ modulator. This structure can have both high speed and high resolution. Because of oversampling in ∑Δ modulator speed is slower than conventional current steering DAC. However proposed structure still have fast speed because recent current steering DAC is very fast. Recent high speed current steering DAC which operate over GS/s make proposed DAC fast enough.

Even though proposed structure has lower resolution than ∑Δ DAC, it is faster than them and it's more accurate than conventional current steering DAC.

Increased resolution by ∑Δ modulation can be seen by MATLAB simulation.

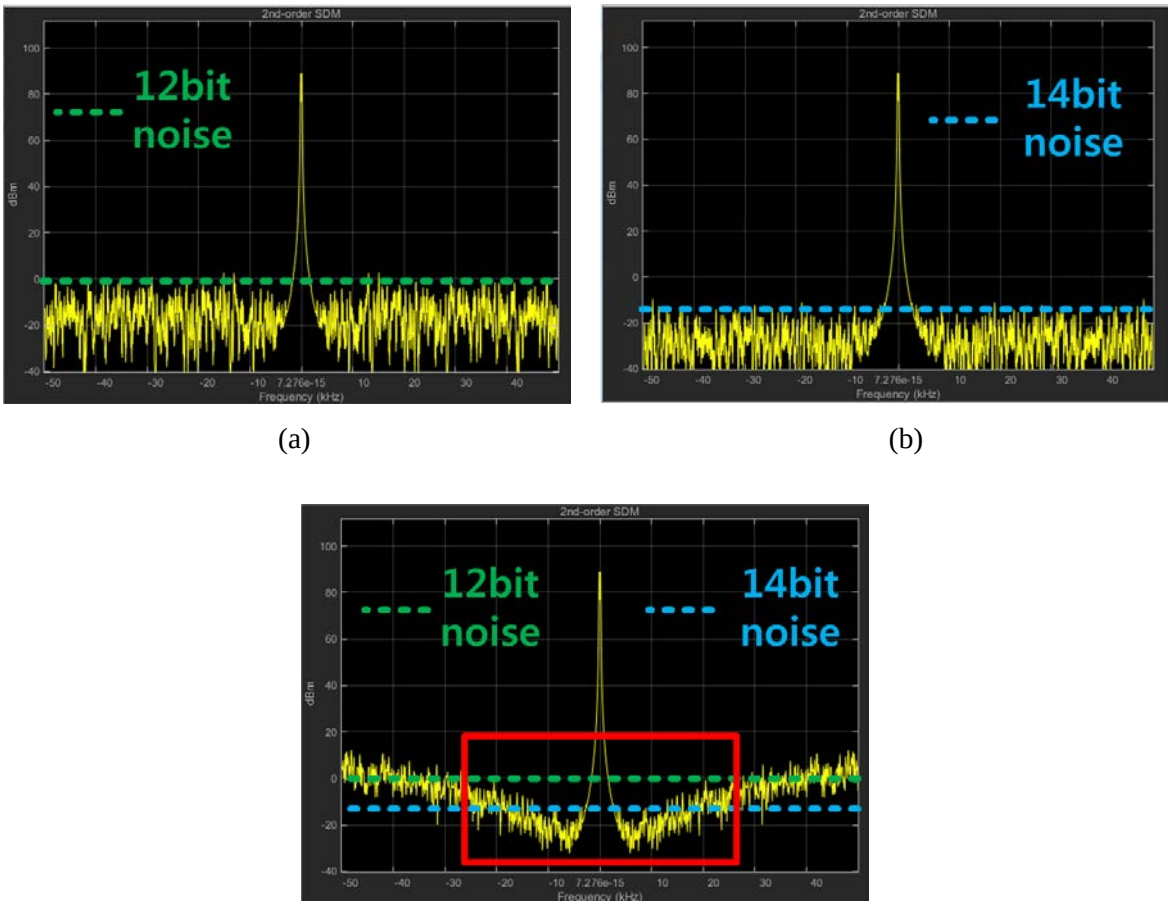


Fig. 38. MATLAB simulation spectrum of (a) 12bit DAC, (b) 14bit DAC and (c) proposed 12bit DAC + 2bit modulation.

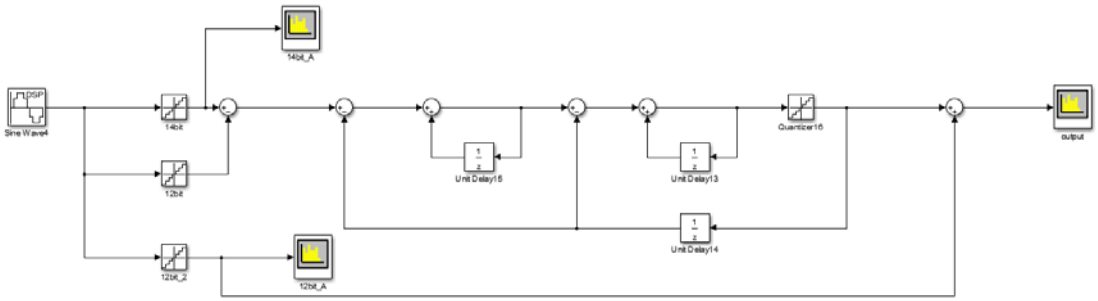


Fig. 39. Proposed structure simulink model for fig. 38 simulation.

Fig. 39 show 12bit DAC + 2bit ∑Δ modulation simulink model and result is Fig. 38. Each 12bit and 14bit DAC has different noise spectrum like fig. 38 (a) and (b). Proposed 12bit DAC + 2bit ∑Δ modulation result is fig. 38 (c). At high frequency, noise is even larger than 12bit DAC. but low frequency part show similar noise spectrum with 14bit DAC. This simulation show resolution of proposed noise shaped DAC is increased in low frequency.

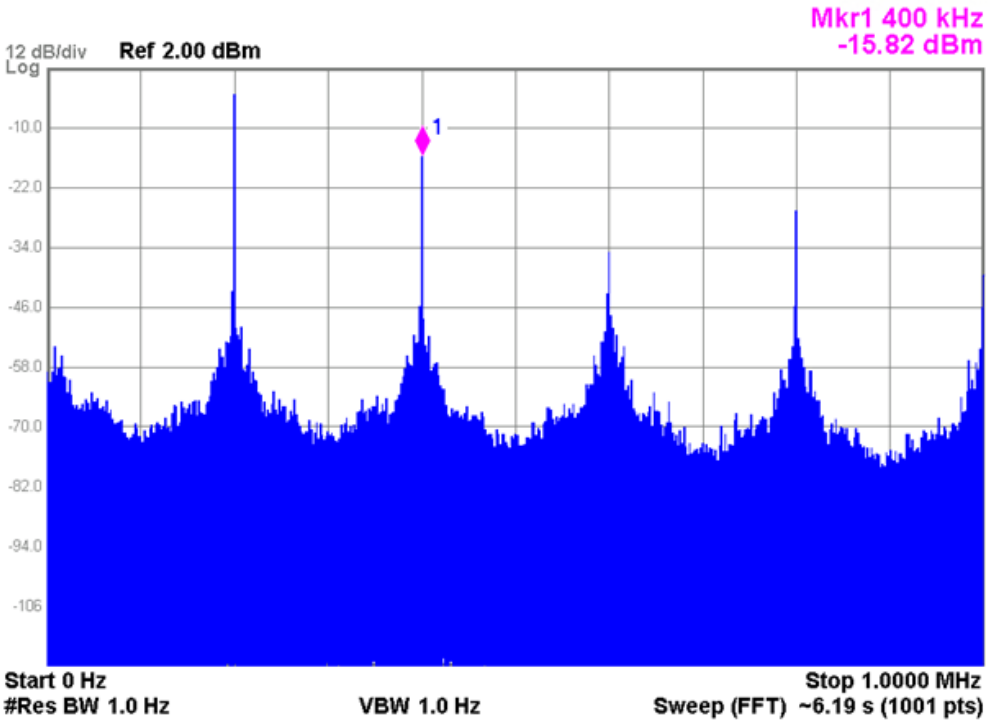
4.3.2 Multi resolution possibility.

Another advantage of proposed structure is resolution controllability. Proposed structure has conventional current steering already. It can still operate as high speed DAC if ∑Δ modulator is turn off because MSB input isn't modulated by ∑Δ modulator. On the other hand, proposed DAC can be used as high resolution DAC with ∑Δ modulator. Like this manner, proposed DAC is easily transformed into high resolution mode and high speed mode

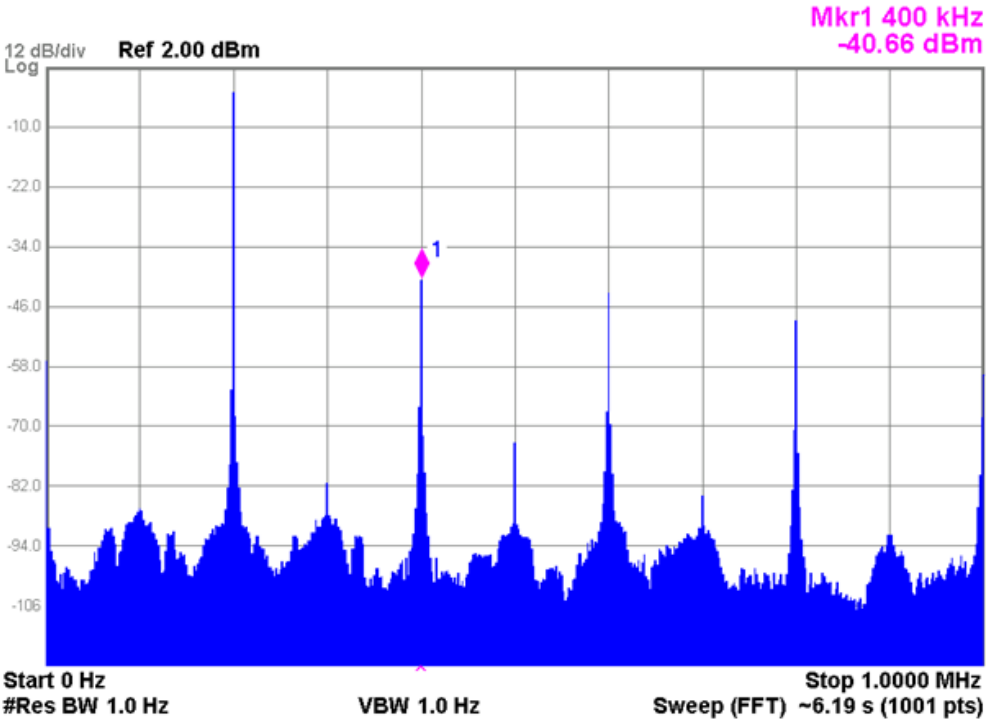
4.4 Test result.

Prototype version of proposed structure DAC is tested to verify the proposed idea. Test chip implemented in 180nm process with 1.8V power supply. Test chip include ∑Δ modulator, Q^2 random walk and DEM.

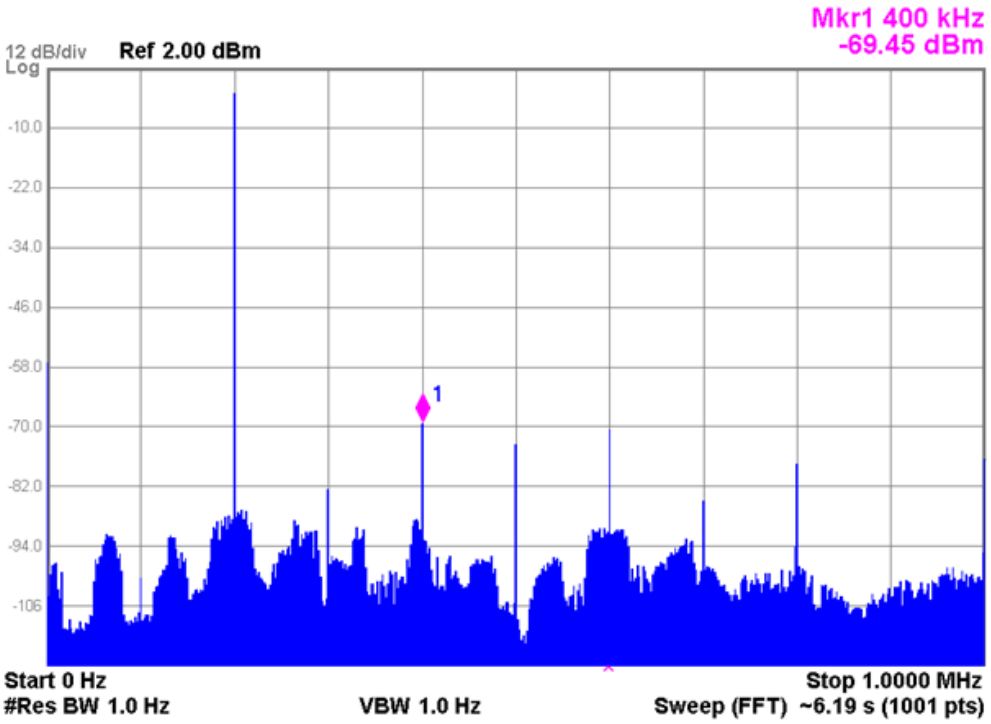
Prototype DAC tested for 200 kHz desired output signal clocked at 2MS/s. Output spectrum measured by spectrum analyzer. Fig. 40 shows spectrum output of prototype DAC.



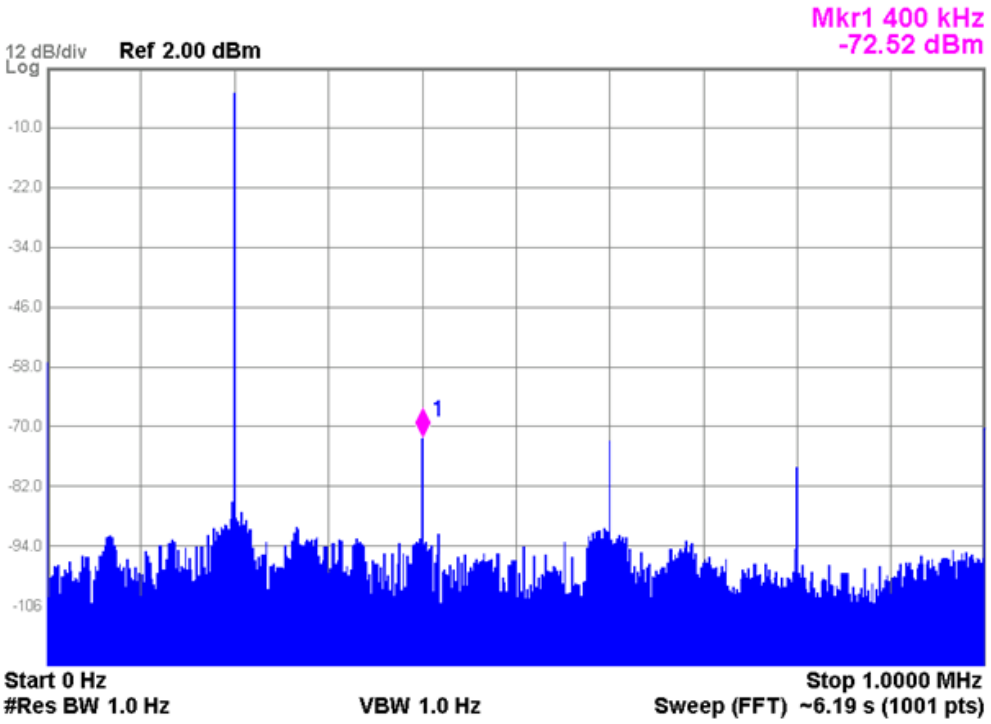
(a)



(b)



(c)



(d)

Fig. 40. Spectrum output for 5MHz desired output signal clocked at 2MS/s. (a) ∑Δ modulator : OFF / Q^2 random walk : OFF / DEM : OFF (b) ∑Δ modulator : ON / Q^2 random walk : OFF / DEM : OFF (c) ∑Δ modulator : ON / Q^2 random walk : ON / DEM : OFF (d) ∑Δ modulator : ON / Q^2 random walk : ON / DEM : ON

Test result show effect of applied technique. Comparison of fig. 40 (a) and (b) shows ∑Δ modulator which related with LSB decrease noise of DAC. Comparison of fig. 40 (b) and (c) shows Q^2 random walk which increase the linearity suppress harmonic distortion occurred by mismatch and nonlinearity. Comparison of fig. 40 (c) and (d) shows DEM suppress spurs which occurred by mismatch.

All of these test result shows that proposed MSB and LSB randomizing resolution improving current steering structure are operation correctly.

Chapter V

Test Chip Implementation

5.1 12bit Resolution RRBS DEM DAC in 130nm CMOS.

5.1.1 Chip implementation.

This test chip apply Random Rotation-based Binary-weighted Selection (RRSB) DEM technique [7] and segmentation. This chip implemented as 12bit current steering DAC in 130nm CMOS process.

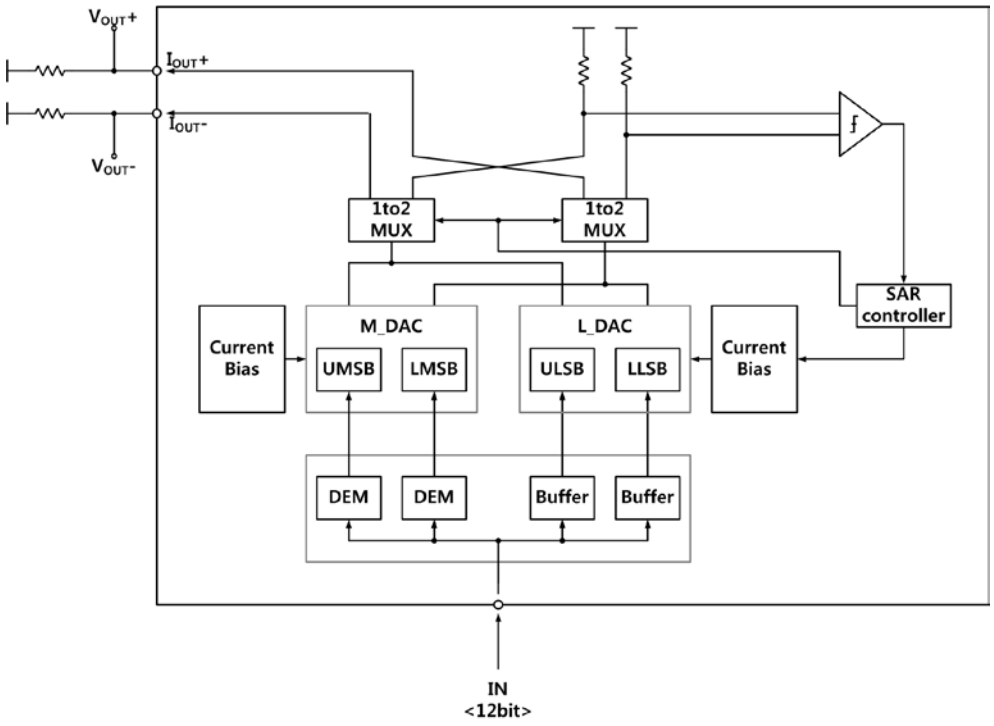


Fig. 41. Block diagram of test chip.

Fig. 41 shows block diagram of test chip. It divided by 4 segment. Each segment composed of 3bit DAC. Because MSB is dominant for DAC performance, RRBS DEM is applied to two MSB side segment. Other two LSB side segment are binary weighted DAC. There are some calibration circuit also added.

Applied RRSB is one type of DEM. Fig. 42 shows operating principle of it. This RRBS is very simple and compact DEM. Unlike other DEM, RRBS doesn't need thermometer decoding. Binary input is

directly applied and shifted by random amount. This RRSB doesn't fully shuffle current cell. It simply shifting input. This method is very simple and compact than other DEM.

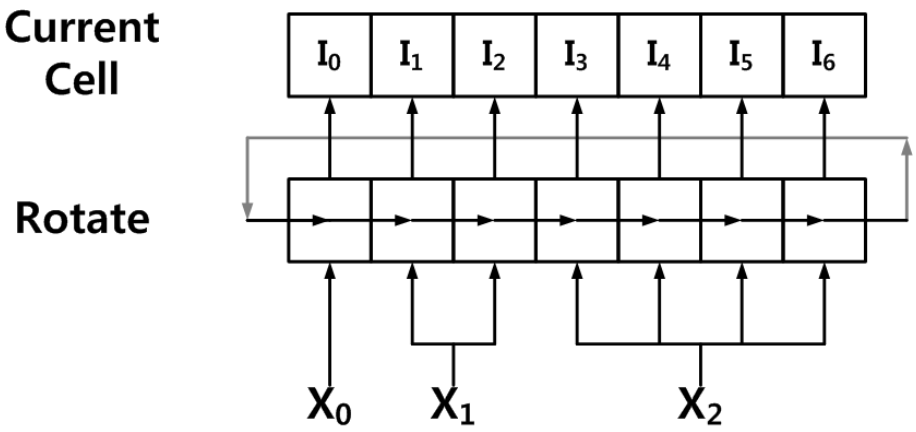
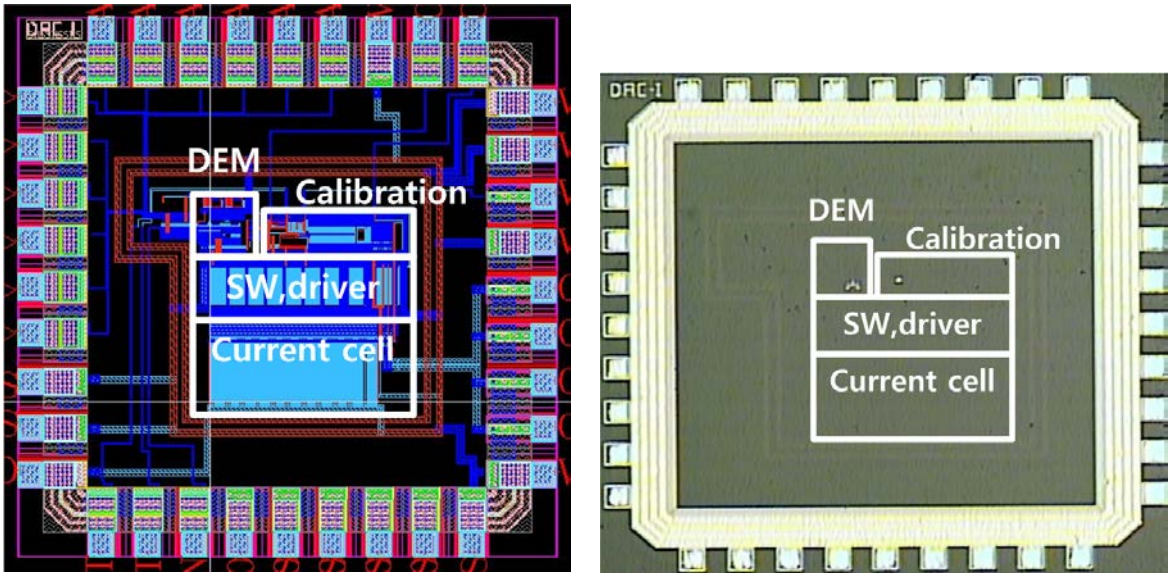


Fig. 42. Operation principle of RRSB.

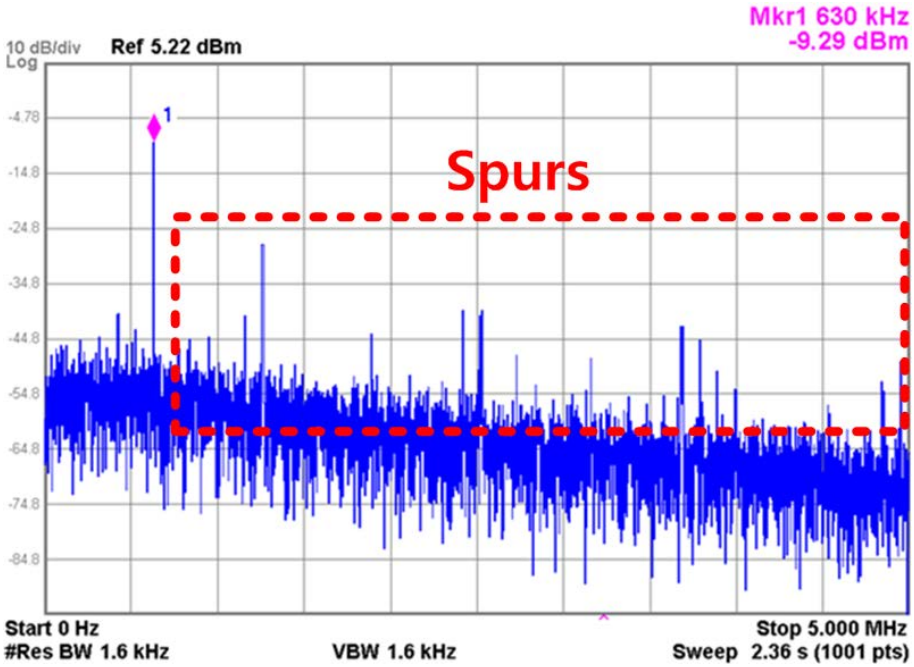
Fig 43 shows test chip layout and chip photograph.



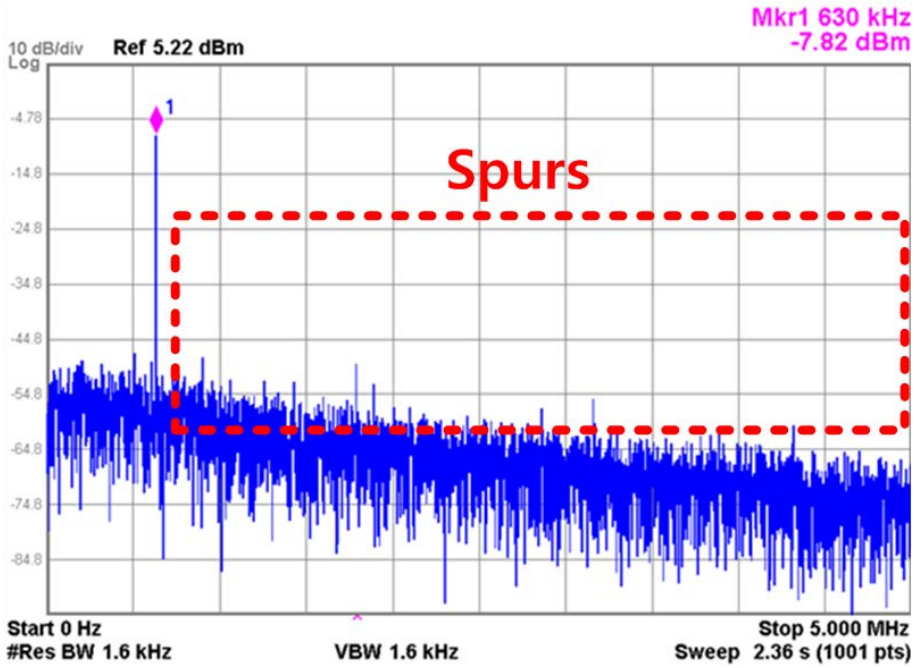
(a) (b)

Fig. 43. (a) Test chip layout (b) Test chip photograph.

5.1.2 Test result.



(a)



(b)

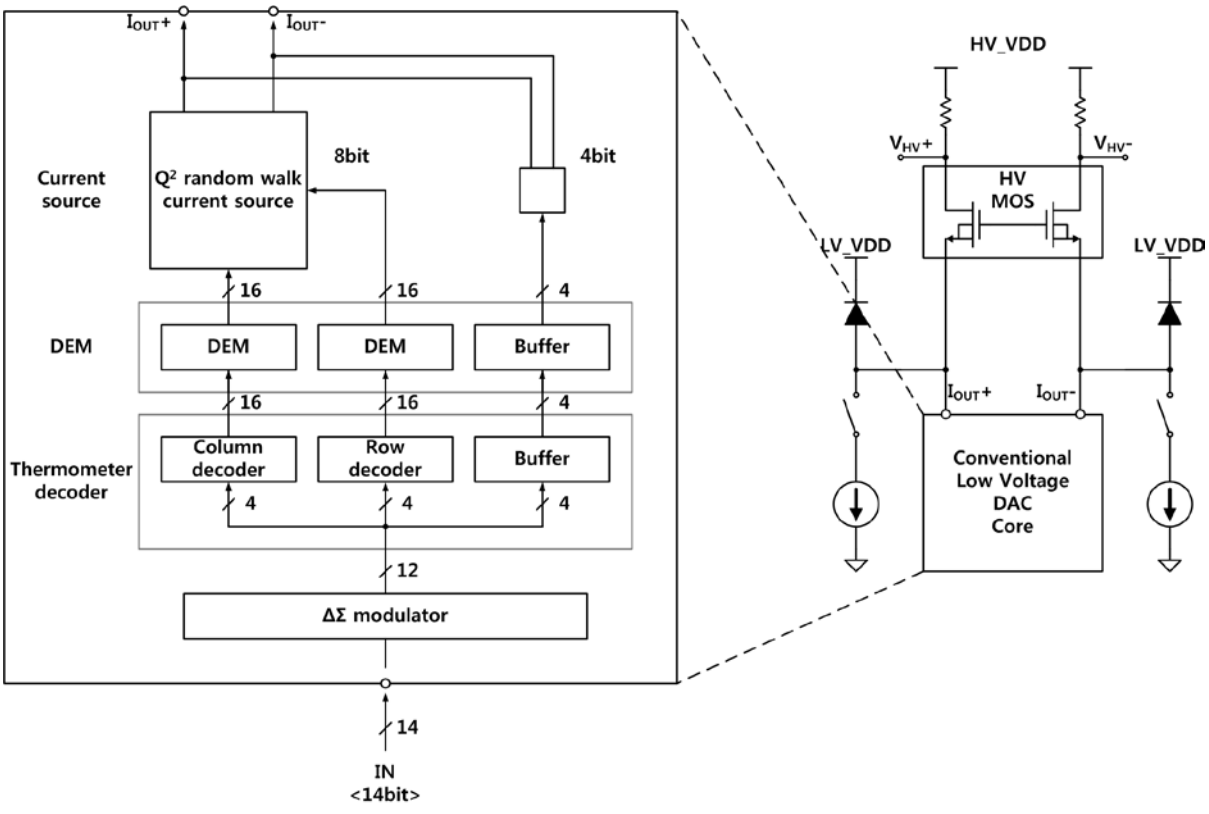
Fig. 44. Output spectrum for 630 kHz desired signal clocked 10MS/s. (a) without RRBS (b) with RRBS

Fig. 44 (a) shows output spectrum without RRBS. Test chip generate many spur because current cells have lots of mismatch. Fig. 44 (b) is output spectrum with RRBS. It generate less spurs than fig. 44 (a). By randomly selecting current cells, effect of mismatch is degenerated and spurs also dcrerese.

5.2 14bit Resolution $\sum\Delta + Q^2$ Random Walk + DEM + HV Protection Current Steering DAC in 180nm BCDMOS.

5.2.1 Chip implementation.

14bit resolution test chip is implemented in 180nm bipolar-CMOS-DMOS metal oxide semiconductor (BCDMOS) process. BCDMOS is the process which can place bipolar, CMOS and double-diffused MOS (DMOS) in single wafer. In this test chip, both of proposed structures are integrated.

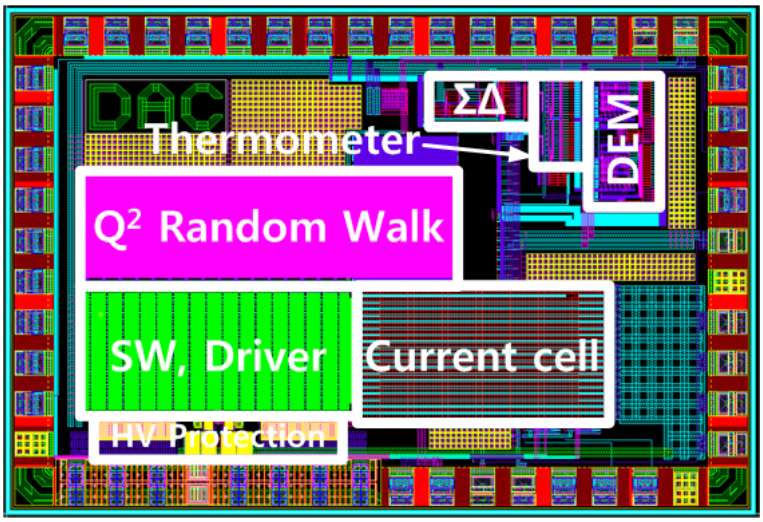


(a) (b)

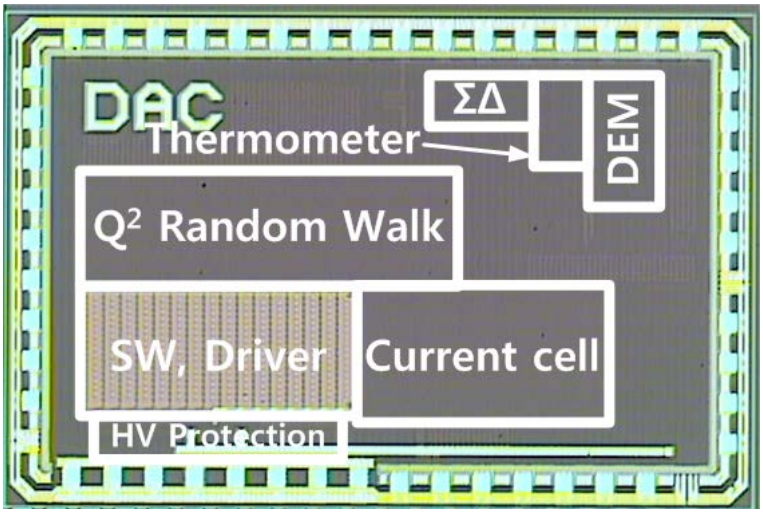
Fig. 45. Block diagram of test chip. (a) Current steering DAC core. (b) High voltage protection.

Test chip composed of low voltage DAC core and high voltage protection circuit like fig. 45. High voltage protection circuit is designed as described in chapter 3. Low voltage DAC core include all function explained in chapter 4. Included functions are ∑Δ modulator, Q^2 random walk, DEM and segmentation.

Test chip has 12bit current DAC and improve resolution by 2bit with ∑Δ modulator noise shaping. Current DAC segmented by 3 Segment. MSB segment is designed as binary coded DAC and other two segment connected to DEM and Q^2 random walk. High voltage protection circuit used LDMOS which has operating drain voltage is 40V.



(a)

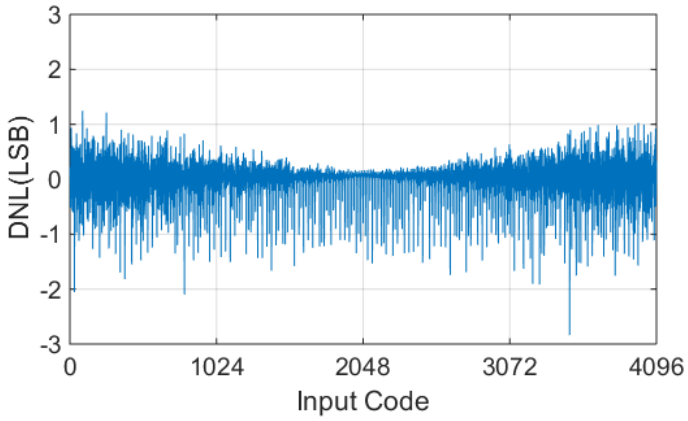


(b)

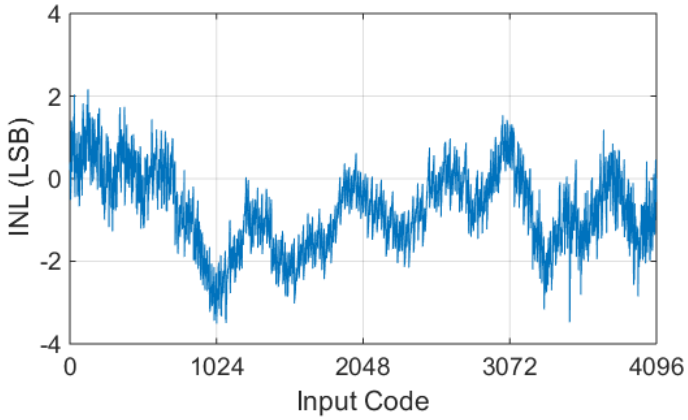
Fig. 46. (a) Test chip layout (b) Test chip photograph.

Layout and photograph of test chip are shown in fig. 46. There are not only analog current block but also performance improving digital block and high voltage protection circuit.

5.2.2 Test result.



(a)



(b)

Fig. 47. Test chip linearity specification. (a) DNL (b) INL

Linearity of tested chip is measured. Fig. 47 shows linearity of test chip without ∑Δ modulator. INL move up and down because of Q^2 random walk.

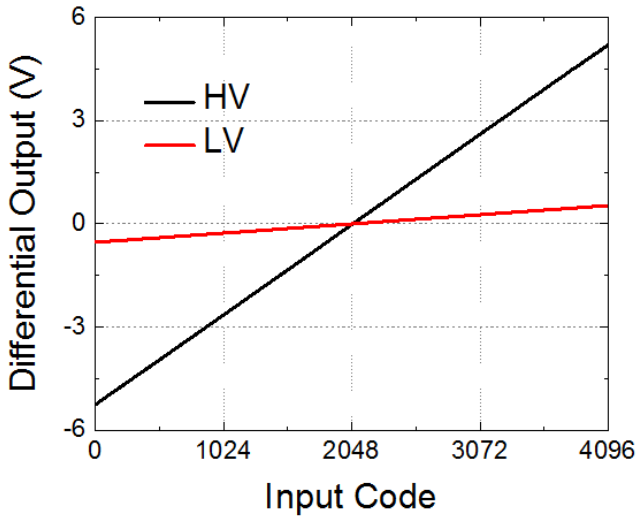


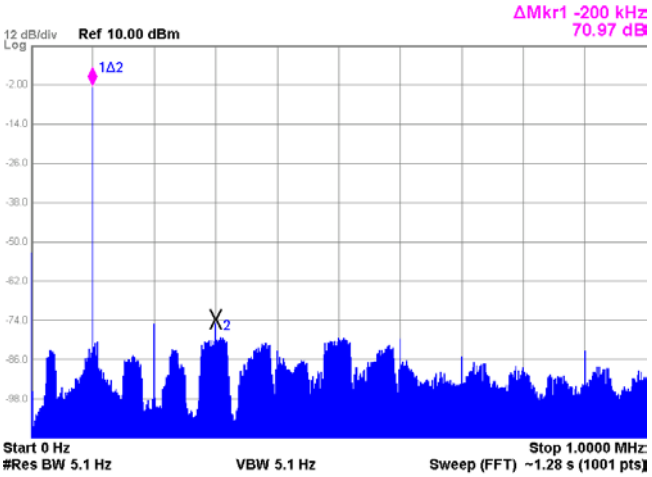
Fig. 48. Differential voltage range of high voltage mode (10Vpp) and low voltage mode (1Vpp)

High voltage protection structure also tested. Fig. 48 shows differential output voltage range of high voltage mode and low voltage mode. Each mode have 10 peak to peak voltage (Vpp) and 1Vpp range. Low voltage mode is tested at 1.8V supply voltage and high voltage mode is tested at 12V supply voltage.

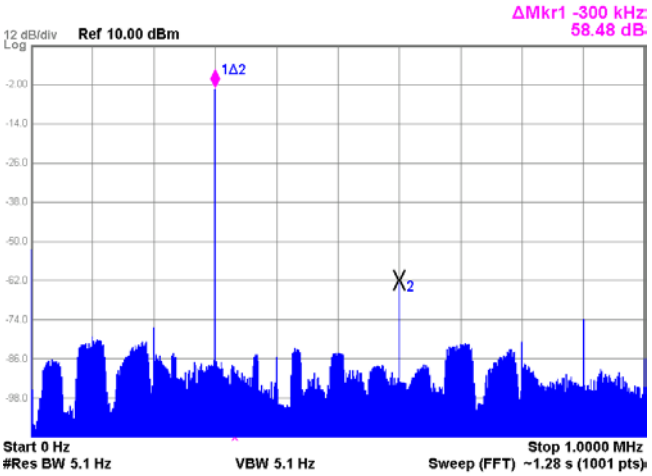
Following table. 3 shows SFDR of test chip. Fig. 49 and Fig. 50 show output spectrum of test chip.

Update frequency (MHz)	Output frequency (MHz)	SFDR (dB)
2	0.1	71
	0.3	58.5
	0.9	60.2
20	1	64
	3	54.3
	9	40.1

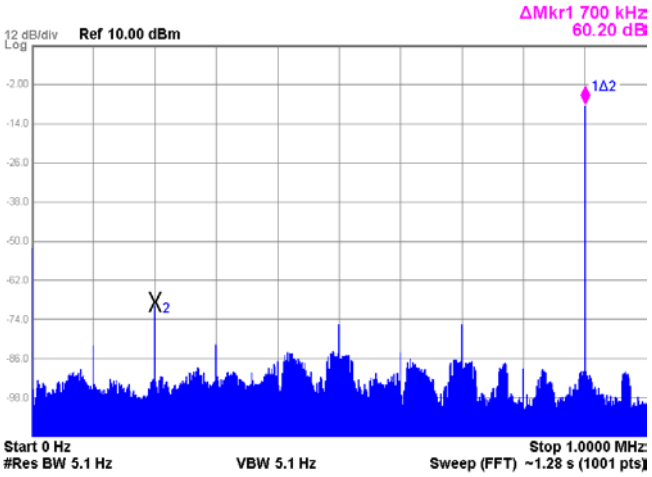
Table. 3. SFDR of test chip.



(a)

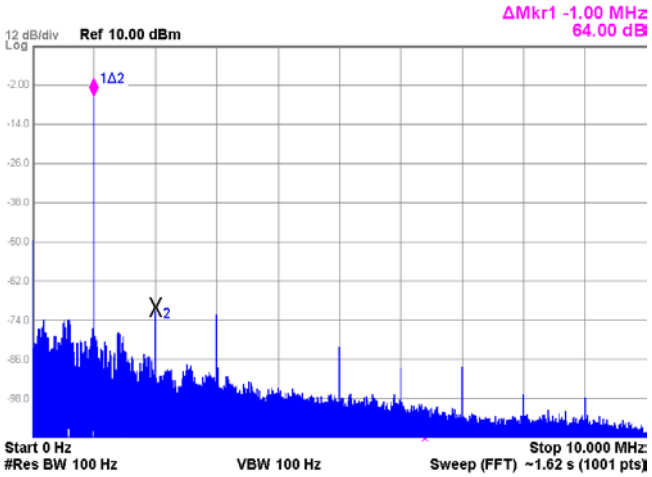


(b)

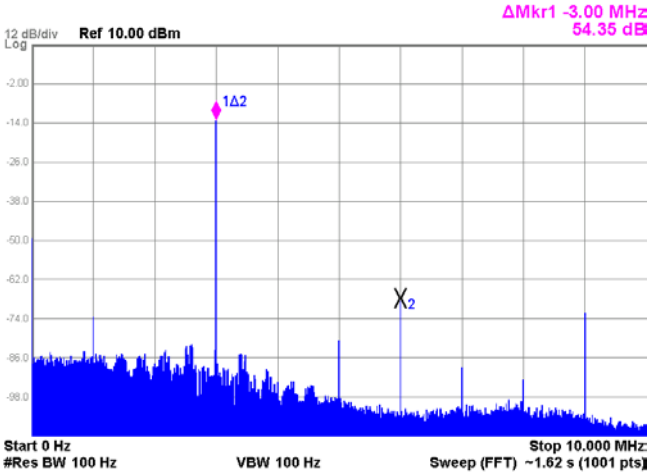


(c)

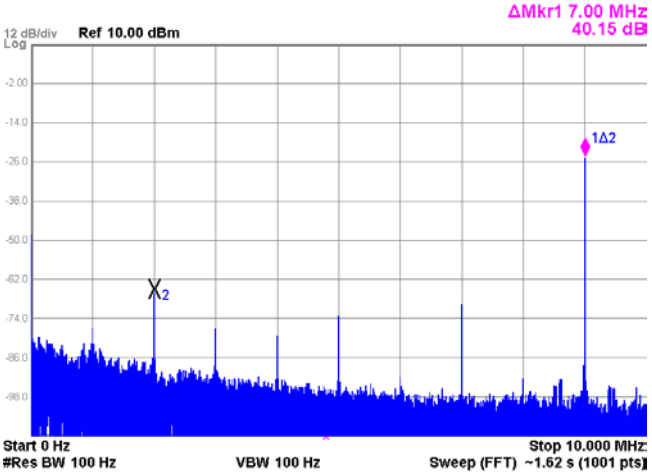
Fig. 49. Output spectrum and SFDR with 2MHz update frequency (a) 100 kHz (SFDR 71dB) (b) 300 kHz (SFDR 58.5dB) (c) 900 kHz (SFDR 60.2dB)



(a)



(b)



(c)

Fig. 50. Output spectrum and SFDR with 20MHz update frequency (a) 1MHz (SFDR 64dB) (b) 3MHz (SFDR 54.3dB) (c) 9MHz (SFDR 40.1dB)

Chapter VI

Conclusion

Targets of this thesis is two things. One is high voltage swing current DAC for industrial application and the other is resolution improving by sigma-delta modulation other linearity compensation method from art-of-the-state.

Each proposed structure start from different motivation. First motivation is industrial application high voltage requirement. DAC can be used in various application. But conventional CMOS process DAC can't handle high voltage (over 5V) because this high voltage exceed the conventional CMOS operation voltage. Common method for high voltage operation is adding high voltage driving amplifier. But additional driving amplifier cause additional distortion by its own distortion and additional power consumption. It also use lots of costly high voltage transistor. Proposed high voltage protection structure decrease use of high voltage transistor by 2 and cost is reduced by it. And proposed structure even improve linearity of DAC by changing effective output impedance. Operation of high voltage protection is verified with prototype chip test.

Second motivation is resolution limitation by matching properties. Recent current steering DAC becomes fast enough to cover over GHz range with developing technologies. But resolution of current steering DAC still limited by matching of devices. There might be matching independent circuits which can improve resolution. It is sigma-delta modulator. Sigma-delta modulator combined structure improve resolution by noise shaping at a cost of speed. Sigma-delta modulator is LSB side randomization. MSB side randomization also needed to compensate original DAC linearity. So Q^2 random walk and DEM also added to proposed structure. Test result of prototype show performance improvement by proposed structure.

Both targets are achieved by proposed circuits and verified by prototype chip test. One method change operation voltage range and the other method change resolution. By applying both method, DAC might be used in various application that require various operation voltage and resolution.

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Acknowledgements

First and foremost, I would like to thank to my supervisor, Prof. Jae Joon Kim, for his encouragement and guidance. His support and inspiration lead me to develop my research. It's great luck for me to study and research with his instruction.

I would like to thank to my committee member, Prof. Jaehyouk Choi. Every his comment help me to improve my research. Also, I would like to thank to another committee member, Prof. Seokhyeong Kang, for his advice. He help me to complement imperfect point of research.

Finally, I appreciate my lab member helping me to overcome difficult. Especially I would like to thank to Kwangmuk Lee for his help on this research.