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Multilayer bipolar field-effect transistors

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Field-effect transistors comprising a layer of regioregular poly(3-hexylthiophene) (rr-P3HT) separated from a parallel layer of the soluble fullerene,[6,6]-phenyl C_{61}-butyric acid methyl ester (PCBM) by a layer of titanium suboxide (TiO_x), are fabricated by solution processing. Because the TiO_x is an electron transporting material and a hole blocking material, this multilayer architecture operates either in the *p*-channel mode with holes in the rr-P3HT layer or in the *n*-channel mode with electrons in the PCBM layer. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2816913]

Organic field-effect transistors (FETs) show promise as components for low-cost, flexible, and portable electronic applications including, for example, smart cards, electronic identification tags, and active matrix displays.[1–3] Bipolar organic FETs, which integrate both *p*-type and *n*-type channels in one device and thereby simplify the design and fabrication processes, are particularly attractive for use in such applications.[4–6] The fabrication of bipolar organic FETs is, however, difficult because organic materials typically show either significantly higher hole mobility or significantly higher electron mobility.[7–10]

In order to realize bipolar organic FETs, bulk heterojunction (BHJ) blend materials comprising both hole and electron transporting materials have used as the active layer.[5,11–13] However, since percolation in two dimensions requires volume fractions >50%, it is difficult to achieve bicontinuous networks for both components in the confined space near the interface with the gate dielectric. Moreover, the tortuous pathways within the phase separated two-component blend cause a significant reduction in apparent mobility compared to that of either component in pure form.

In another approach, bilayer FETs have been suggested, with separate (parallel) hole-transport and electron-transport channels within a multilayered device structure.[14–18] However, interactions between the carriers at the interface between the two layers prevents the realization of true *p*-channel and *n*-channel behavior at low gate bias. Moreover, when fabricating the bilayer using solution processing, the deposition of the second layer tends to damage the first layer underneath. Although this can be minimized by using two materials which are not cosoluble (such as one being hydrophobic and the other being hydrophilic), most attempts at making bipolar FETs with a bilayer structure have utilized thermal deposition of small molecules under high vacuum conditions.

We report here the fabrication and characterization of bipolar FETs using regioregular poly(3-hexylthiophene) (rr-P3HT) and [6,6]-phenyl C_{61}-butyric acid methyl ester (PCBM) by spin casting the various layers from solution. In order to achieve the desired bilayer structure comprising two independent layers made of rr-P3HT and PCBM, respectively, we have introduced an intermediate layer of sol-gel-processed titanium suboxide (TiO_x) between the two semiconductor layers. The bottom of the conduction band and the top of the valence band of TiO_x are at −4.3 and −8.1 eV, respectively (both with respect to the vacuum).[19] As a result, electrons are readily transferred across an interface between TiO_x and the lowest unoccupied molecular orbital (LUMO) of a conjugated polymer semiconductor, whereas holes are blocked by the large energy barrier at such an interface. Therefore, the TiO_x layer acts as a functional separation layer which ensures that holes and electrons are injected only into the specifically desired semiconductor (holes in the rr-P3HT and electrons in the PCBM).

All FET structures were fabricated on a heavily doped *n*-type Si wafer with a 200 nm thick thermally grown SiO_2 layer. The doped *n*-type Si functioned as the gate electrode and the SiO_2 functioned as the gate dielectric insulator. In order to improve the adhesion of gate electrode, 3 nm titanium (Ti) layer was deposited first and then Au gate deposition was made on top of it. Each of the semiconductor layers, rr-P3HT and PCBM, were spin cast at 2500 rpm for 60 s inside a controlled atmosphere glove box filled with N_2. The concentration of the rr-P3HT solution in chloroform was 2 mg/ml, and the concentration of the PCBM solution in chlorobenzene was 10 mg/ml. The thickness of each layer was ~50 nm. The TiO_x layer between the two semiconductor films was prepared using a precursor solution as described in detail elsewhere.[19] The methanol based TiO_x solution was spin cast at 5000 rpm for 60 s in air on top of the first active layer. The thickness of the TiO_x layer is ~20 nm. After deposition of TiO_x layer and prior to the deposition of rr-P3HT layer, source and drain electrodes (Al) with 50 nm thickness were deposited on the TiO_x by thermal evaporation under $<10^{-6}$ torr using a shadow mask. The channel length (L) and the channel width (W) were $L=50\ \mu$m and $W=1500\ \mu$m. Electrical characterization was performed using a Keithley semiconductor parametric analyzer (Keithley 4200) with the FET in the dry box under N_2 atmosphere.

The device architecture is shown in Fig. 1. In order to function independently, the *p*-channel path and *n*-channel path must be electronically separated, i.e., the material used

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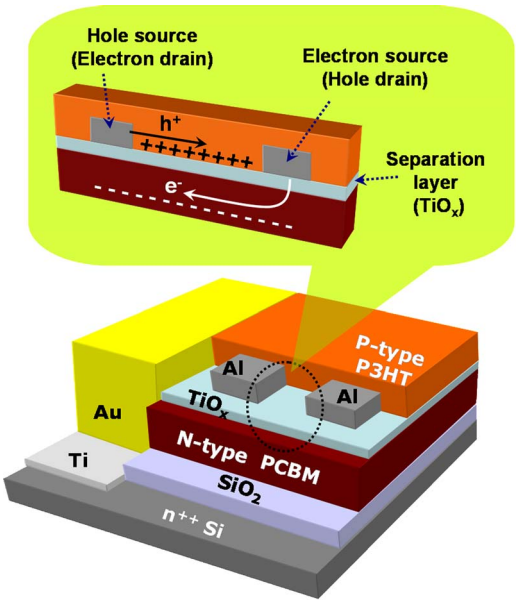

FIG. 1. (Color online) Conceptual diagram of bilayer FETs with completely separated *p* channel and *n* channel by introducing intermediate functional layer.

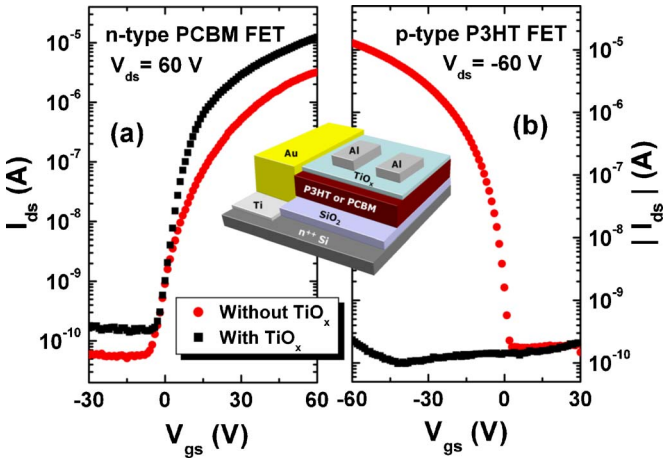

FIG. 2. (Color online) Transfer characteristics of unipolar FETs including a TiO_x layer between the active layer and the source-drain electrodes. (a) *n*-type PCBM FET and (b) *p*-type rr-P3HT FET. For both cases, the data plotted by filled circle (red) represents the devices without TiO_x and the data of filled rectangular (black) is for the devices with the TiO_x layer.

for the separating layer must transport only one species of charge (either holes or electrons), and it must block the other. In addition, there must be no chemical interaction between the material in the separating layer and either of the two semiconducting materials, and carrier traps at the two interfaces should be minimized. Finally, in order to enable fabrication by printing technology, all three layers must be processible from solution without degrading the previously cast layer(s).

We have selected the sol-gel processed titanium suboxide (TiO_x) as the material for the separating layer. TiO_x is a good electron transporting material and a hole blocking material. The bottom of the conduction band (4.4 eV) of TiO_x is close to the work function of Al (4.3 eV), and close to the LUMO energy level of PCBM (4.2 eV).[6,20–22] The top of the valence band of TiO_x (8.1 eV) is sufficiently electronegative to block holes. Thus, we expect that TiO_x will function as an effective separating layer between the hole transport channel and the electron transport channel. Moreover, since the TiO_x precursor is typically prepared in isopropyl alcohol or in methanol, thin films of TiO_x can be formed by spin casting without disturbing the underlying layer cast from an organic solvent.

Based upon our previous studies of bipolar FETs fabricated using a phase separated BHJ blend of rr-P3HT and PCBM,[6,22] Al was chosen to enable approximately equivalent injection of electrons (into PCBM) and holes (into rr-P3HT). The device architecture shown in Fig. 1, with Al electrodes between the TiO_x and the rr-P3HT assures charge injection for holes into the rr-P3HT and for electrons into the PCBM.

In order to clarify the role of the TiO_x layer, unipolar FETs covered with TiO_x on top of the active layer were fabricated. The transfer characteristics of *n*-type FETs using PCBM and *p*-type FETs using rr-P3HT are shown in Figs. 2(a) and 2(b), respectively. For the *n*-type PCBM FET, because of the small barrier at the TiO_x/Al interface and the good electron transport nature of TiO_x, the device with the TiO_x layer exhibits even better performance compared to the device without the TiO_x layer. On the other hand, because of the large energy barrier between the Al electrode and the top of the valance band of TiO_x, hole carriers are blocked by the TiO_x layer. With the TiO_x layer in place, there is no indication of hole injection into the *p*-type rr-P3HT channel as a function of the applied gate bias [see Fig. 2(b)]. We conclude that the TiO_x layer electronically separates the *p*-channel path and *n*-channel path in the multilayer structure.

Figure 3 shows the transfer characteristics of the heterostructured bipolar FET with the TiO_x separating layer. The

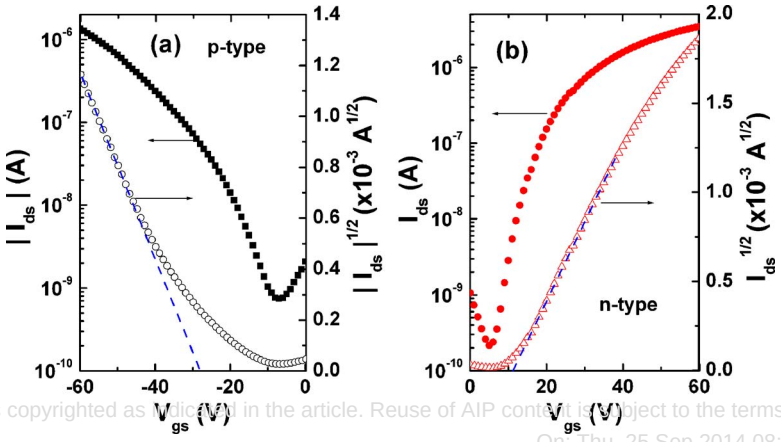

FIG. 3. (Color online) Transfer characteristics of the most optimized bilayer FETs. (a) *p*-type operation and (b) *n*-type operation. The mobilities deduced from the linear plot of $I_{ds}^{1/2}$ (the curve plotted by open symbol) were estimated to be $\mu_e = 8.9 \times 10^{-3}$ cm^2 V^{-1} s^{-1} in the *n*-channel mode and $\mu_h = 5.7 \times 10^{-3}$ cm^2 V^{-1} s^{-1} in the *p*-channel mode.

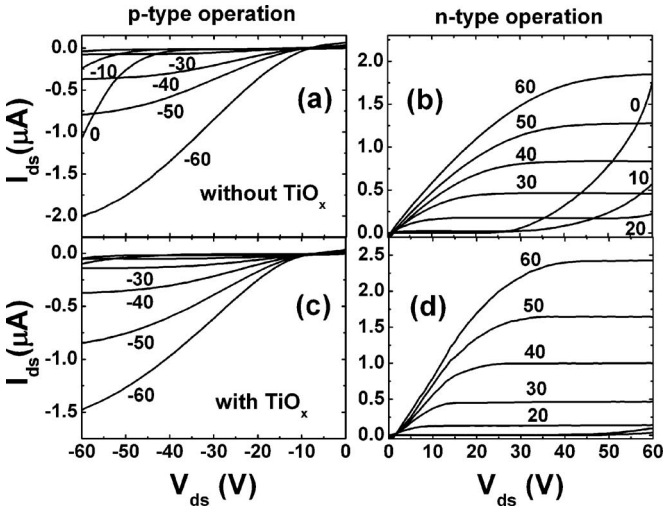

FIG. 4. Output characteristics (I_{ds}-V_{ds} plots) of the bilayer devices with and without the TiO_x separating layer. The data in (a) and (b) were obtained from bilayer FETs without the TiO_x separation layer (fabricated by thermal evaporation of C_{60}). The data in (c) and (d) were obtained with the TiO_x separating layer (see Fig. 1).

data obtained with negative V_{ds}(=−60 V) and negative gate bias yield *p*-type operation [Fig. 3(a)], while positive V_{ds}(=60 V) and positive gate bias yield *n*-type operation [Fig. 3(b)]. The device shows bipolar behavior with both *p*-type and *n*-type characteristics. The mobilities deduced from the slopes of $I_{ds}^{1/2}$ versus V_{gs} were estimated to be $\mu_e = 8.9 \times 10^{-3}$ cm^2 V^{-1} s^{-1} in the *n*-channel mode and $\mu_h = 5.7 \times 10^{-3}$ cm^2 V^{-1} s^{-1} in the *p*-channel mode.

As demonstrated in Fig. 4, the effect of separated hole and electron channels by the TiO_x intermediate layer is clearly shown in the output characteristic measurements. I_{ds}-V_{ds} plots obtained from bilayer devices with and without the TiO_x separating layer. For the bilayer FET without the TiO_x separation layer [Figs. 4(a) and 4(b)], "opposite" carrier currents are observed at low gate biases because of bipolar injection into each of the two semiconductors and because of electron-hole recombination at the interface between the *p*-type and *n*-type material due to the Coulomb attraction.[23] For the bilayer FET with the TiO_x separating layer [Figs. 4(c) and 4(d)], these opposite carrier currents are suppressed at low gate biases, fully consistent with the device operating concept shown in Fig. 1. The I_{ds}-V_{ds} data in Figs. 4(a) and 4(b) are, however, nonlinear at low V_{ds}, suggesting non-Ohmic source and drain contacts.

In conclusion, we have demonstrated bipolar organic FETs using rr-P3HT and PCBM separated by an intermediate layer of TiO_x. All layers were processed from solution. The data confirm the utility of TiO_x as an electron transport and hole blocking material. In the multilayer FET structure, the TiO_x layer enables bipolar properties by electronically separating the *p* channel from the *n* channel. The optimized device shows good hole and electron mobilities, $\mu_e = 8.9 \times 10^{-3}$ cm^2 V^{-1} s^{-1} in the *n*-channel mode and $\mu_h = 5.7 \times 10^{-3}$ cm^2 V^{-1} s^{-1} in the *p*-channel mode.

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