Article

Extension of Zero Voltage Switching Capability for CLLC Resonant Converter

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Abstract: TheCLLC resonant converter has been widely used to obtaina high power conversion efficiency with sinusoidal current waveforms and a soft switching capability. However, it has a limited voltage gain range according to the input voltage variation. The current-fed structure canbe one solution to extend the voltage gain range for the wide input voltage variation, butit has a limited zero voltage switching (ZVS) range. In this paper, the current-fed CLLC resonant converter with additional inductance is proposed to extend the ZVS range. The operational principle is analyzed to design the additional inductance for obtaining the extended ZVS range. The design methodology of the additional inductance is proposed to maximize the ZVS capability for the entire load range. The performance of the proposed method is verified with a 20 W prototype converter.

1. Introduction

Recently, the small sized power converterhas become significant in various industries, such as lightings, TVs, computers, and other home appliances [1,2]. A power converter operating at a high switching frequency is one effective method to improve power density [3–7]. However, the high switching frequency operation induces a large switching loss for the turn-on and turn-off states. Therefore, a soft switching capability is important to obtain a high power conversion efficiency in a high switching frequency operation [8–10]. Resonant power converters, such as LC resonance, LLC resonance, CLLC resonance, and CLL resonance, can implement the soft switching capability by the resonance, which can be a good candidate to implement the high switching frequency operation [11–15]. In addition, the wide band-gap device (WBD), such as gallium nitride (GaN) and silicon carbide (SiC), can increase the switching frequency up to several MHz compared with conventional silicon (Si)-based switching devices [16–19].

The CLLC resonant converter operating at the inductive region can obtaina zero voltage switching (ZVS) capability [20–23]. However, the large input voltage variation by the batteryinduces large switching frequency variation. In addition, the voltage gain fluctuation makes a non-ZVS operation withthe capacitive operation of the converter [24]. Therefore, the CLLC resonant converter has poor voltage gain characteristics according to the wide input voltage variation. The current-fed CLLC resonant converter can overcome the input voltage variation by the battery, since the current-fed structure compensates the input voltage variation [25,26]. However, the current-fed structure makes a limited ZVS capability of the low side switch, since the low side switch operates as the boost converter and resonant converter simultaneously. Therefore, the increase of the ZVS capability is significant to obtain a high power conversion efficiency for the entire load condition.

In this paper, the current-fed CLLC resonant converter employing the additional inductance is proposed to improve the ZVS capability. The operational principle of the proposed additional inductance is analyzed with the theoretical waveforms. From the operational principle, the design methodology of the additional inductance is analyzed to obtain the ZVS capability for the entire input voltage range and load conditions. The experimental results with a 20 W prototype converter verify the validity of the proposed additional inductance.

2. Operational Principle

Figure 1 shows the scheme of the proposed current-fed CLLC resonant converter. The current-fed structure regulates the wide input voltage variation with the asymmetric pulse width modulation (APWM), because it operates as the synchronous boost converter. The CLLC resonant tank provides the galvanic isolation using the transformer and resonance. The voltage doubler structure of the secondary side can reduce the turn ratio of the transformer.
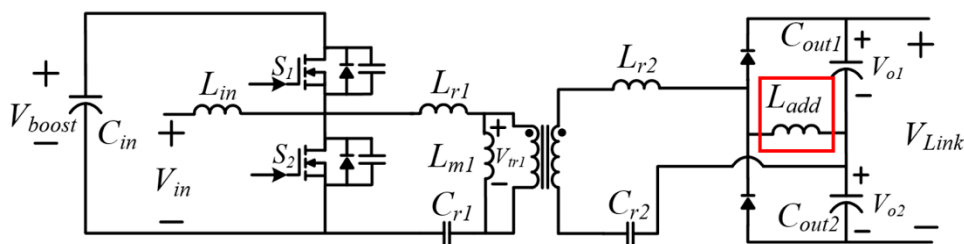

Figure 1. Schematic of the proposed CLLC resonant converter employing additional inductance.

Figure 2 shows the operational waveform of the conventional and the proposed current-fed CLLC resonant converter where S_1 and S_2 are the primary switches, $V_{ds,S1}$ and $V_{ds,S2}$ is the drain-source voltage of S_1 and S_2, respectively, I_{Lin} is the current passing through the input inductor, $I_{r,p}$ is the resonant current in the primary side, I_{Lm} is the magnetizing current, I_{S1} and I_{S2} are the currents passing through S_1 and S_2, respectively, and I_{Ladd} is the current in the additional inductance. The current-fed structure operates as the conventional boost converter by the switching operation of S_1 and S_2. The CLLC resonant tank employing the APWM has zero offset current on the magnetizing inductance which reduces the core and conduction losses of the transformer.

The current-fed structure is proper to compensate the wide input voltage variation. However, it limits the ZVS range according to the increase of the output load. The switch current of conventional voltage-fed CLLC resonant converter for the ZVS capability can be derived as follows:

$$ZVS_{S1} = I_r\left(t_{S2,off}\right) \tag{1}$$

$$ZVS_{S2} = -I_r\left(t_{S1,off}\right) \tag{2}$$

where $I_r(t_{s2,off})$ and $I_r(t_{s1,off})$ are the resonant current at the turn off state of power switches, respectively. The negative current of each switch is required to obtain the ZVS condition. In the voltage-fed CLLC resonant converter, the resonant current onlydetermines the ZVS condition of each switch. In the case of the current-fed CLLC resonant converter, the input inductor and resonant currents determine the ZVS current.The switch current of the current-fed CLLC resonant converter for the ZVS capability can be derived as follows:

$$ZVS_{S1,c} = I_r\left(t_{S2,off}\right) - I_{Lin}\left(t_{s2,off}\right) \tag{3}$$

$$ZVS_{S2,c} = -I_r\left(t_{S1,off}\right) + I_{Lin}\left(t_{s1,off}\right) \tag{4}$$

where $I_{Lin}(t_{s2,off})$ and $I_{Lin}(t_{s2,off})$ are the input inductor current at the turn off state of power switches, respectively. The high side switch (S_1) has a larger ZVS condition compared with Equation (1).

However, the low side switch (S_2) has a poor ZVS condition compared with Equation (2). Figure 2a shows the theoretical waveforms of the conventional current-fed CLLC resonant converter, whichhas a hard switching operation on the S_2. The ZVS capability of the proposed CLLC resonant converter can be derived as follows:

$$ZVS_{S1,p} = I_r\left(t_{S2,off}\right) - I_{Lin}\left(t_{s2,off}\right) - nI_{Ladd}\left(t_{s2,off}\right) \tag{5}$$

$$ZVS_{S2,p} = -I_r\left(t_{S1,off}\right) + I_{Lin}\left(t_{s1,off}\right) - nI_{Ladd}\left(t_{s1,off}\right) \tag{6}$$

where $I_{Ladd}(t_{s2,off})$ and $I_{Ladd}(t_{s2,off})$ are the additional inductor currents at the turn off state of power switches, respectively, and n is the transformer turn ratio. Figure 2b shows the theoretical waveforms of the proposed CLLC resonant converter. The additional inductance extends the ZVS range compared with the conventional current-fed CLLC resonant converter.
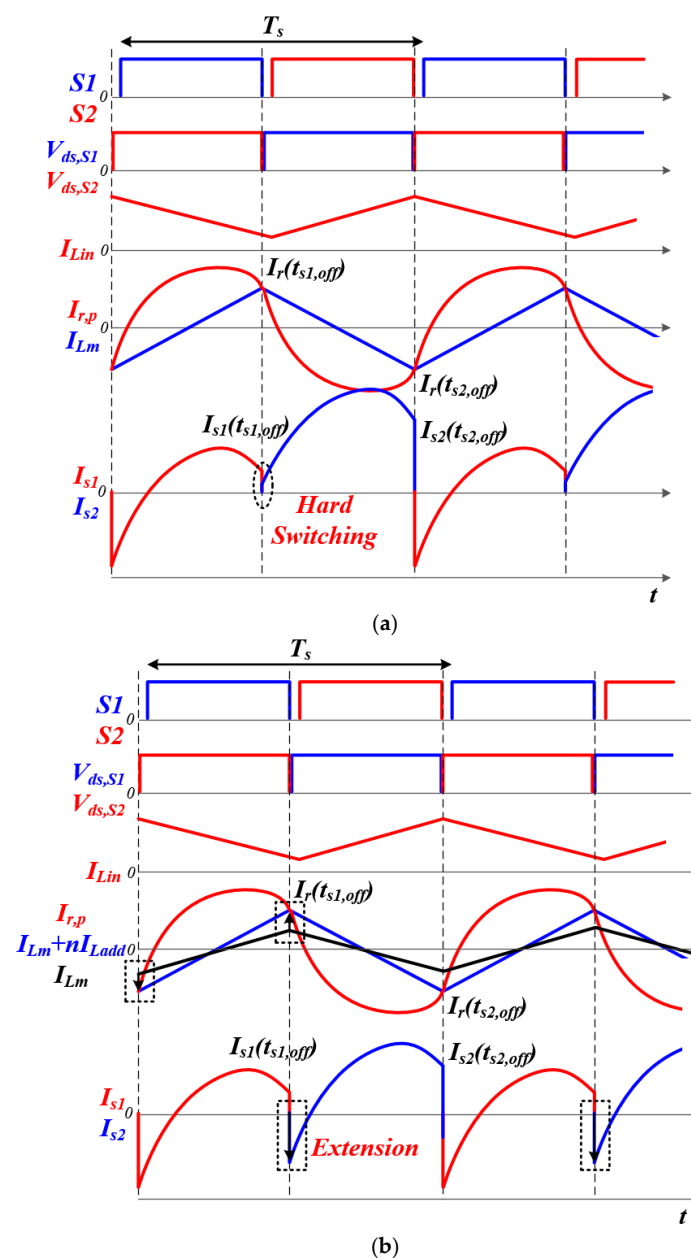

Figure 2. Theoretical operating waveforms: (**a**) Conventional current-fed CLLC resonant converter, (**b**) Proposed current-fed CLLC resonant converter employing additional inductance.

The turnon current for the ZVS condition of the current-fed CLLC resonant converter can be calculated with the input inductor current and resonant current. The ZVS condition on the low side switch can be derived as follows:

$$I_{zvs,s2} = \frac{1}{1 - D_{s2}} \frac{V_{boost}}{R} + \frac{(V_{in} - V_{boost})}{2L}(1 - D_{s2})T_s - \frac{V_{tr1}}{L_m}\frac{1 - D_{s2}}{2}T_s \tag{7}$$

where D_{s2} is the duty ratio of S_2, V_{boost} is the voltage of the current-fed structure, V_{in} is the input voltage of the battery, R is the load resistance, L is the input inductance, T_s is the switching time, L_m is the magnetizing inductance, and V_{tr1} is the transformer voltage. The negative value of $I_{zvs,S2}$ guarantees the ZVS capability of S_2. The decrease of the load resistance makes no ZVS condition of S_2. In addition, the large duty ratio of S_2 makes the worst ZVS condition, which means that the low input voltage condition is the worst ZVS condition.

The turn on current for ZVS condition of the low side switch with the proposed converter can be derived as follows:

$$I_{zvs,s2,p} = \frac{1}{1 - D_{s2}} \frac{V_{boost}}{R} + \frac{(V_{in} - V_{boost})}{2L}(1 - D_{s2})T_s - \frac{V_{tr1}}{L_m}\frac{1 - D_{s2}}{2}T_s - \frac{V_{o1}}{nL_{add}}\frac{1 - D_{s2}}{2}T_s \tag{8}$$

where V_{o1} is the voltage on the output capacitor as shown in Figure 1. The proposed converter extends the ZVS condition with the additional inductor on the secondary side as shown in Figure 2b. Figure 3 shows the ZVS capability according to the additional inductance. The ZVS current is the turn on current of S_2, which is required to have a negative value in order to obtain the ZVS capability. The small additional inductance is proper to extend the ZVS range. However, the small additional inductance increases the conduction loss on the primary side. Therefore, the design methodology of the additional inductance is required to obtain the ZVS capability for the entire load range.
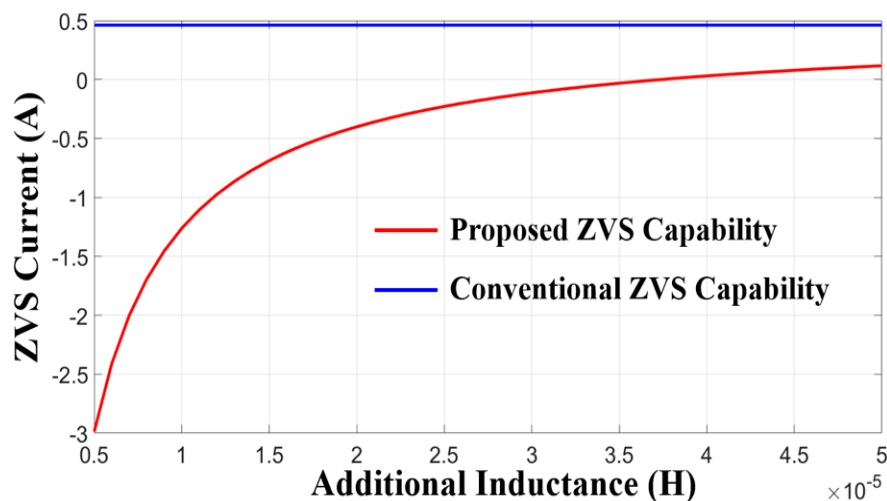

Figure 3. ZVS capability comparison between the conventional current-fed CLLC resonant converter and the proposed current-fed CLLC resonant converter.

The voltage gain according to the duty ratio can be described in Figure 4. The proposed converter has similar voltage gain to that of the conventional boost converter, which shows wide duty ratio variations to regulate the output voltage. The additional inductance can be designed at the worst duty ratio case, which is the maximum duty ratio of S_2.
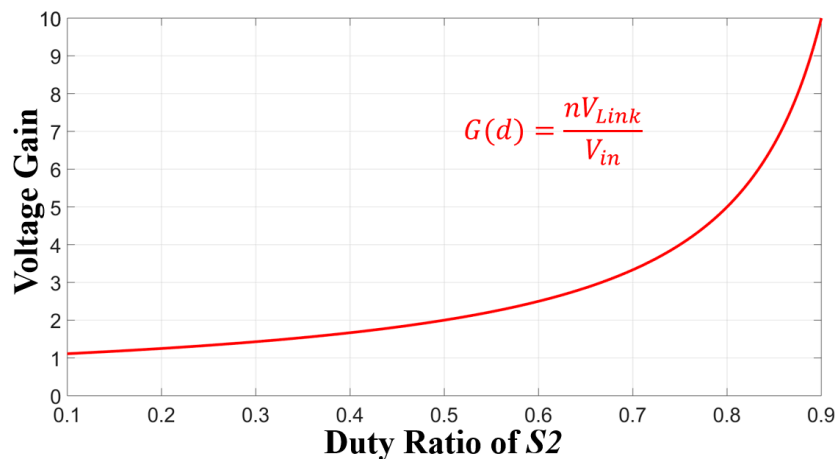
Figure 4. Gain according to duty ratio.

3. Design Methodology of Additional Inductance

The small additional inductance induces the conduction loss with large circulating current. The large additional inductance cannot obtain the ZVS capability of primary switches. Therefore, the maximum additional inductance is required to obtain the ZVS capability and the minimum conduction loss on the additional inductance, which can be derived with Equation (8) as follows:

$$L_{add} = \frac{V_{o1}}{nA} \frac{1-D_{s2}}{2} T_s$$
$$A = \frac{1}{1-D_{s2}} \frac{V_{boost}}{R} + \frac{(V_{in}-V_{boost})}{2L}(1-D_{s2})T_s - \frac{V_{tr1}}{L_m} \frac{1-D_{s2}}{2} T_s \qquad (9)$$

The proper additional inductance can be designed from Equation (9). Figure 5 shows the additional inductance according to the output load condition. The increment of output load requires smaller additional inductance. The design specification is shown in Table 1. The input voltage has a large variation by the state of charge (SOC) of the battery. The load voltage is fixed, and rated load is 20 W. The resonant frequency(f_r) is 200 kHz. The APWM requires the small resonant inductance to obtain the linear voltage gain according to the duty variation.The turn ratio is determined with the input voltage and output voltage ratio. The additional inductance is determined by (9).
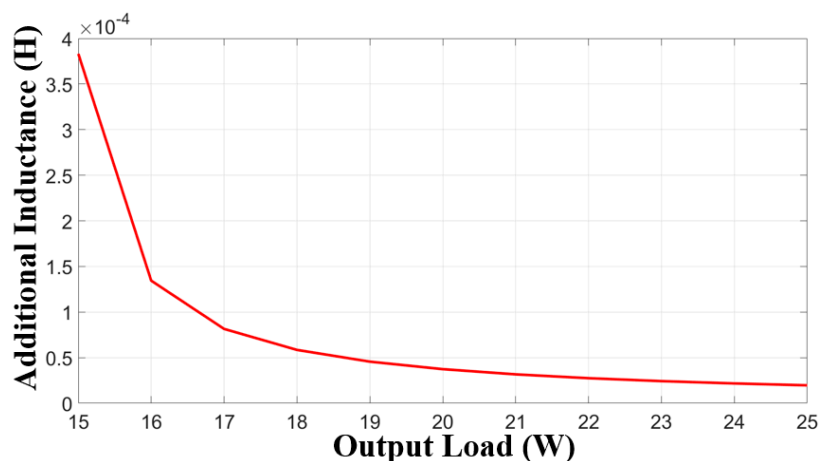

Figure 5. Desired additional inductance to obtain ZVS capability and minimum conduction loss according to output load condition.

Table 1. Design specification.

Parameter	Value
V_{in}	12 V–17 V
Load	32 V, 20 W
f_r	200 kHz
L_r	1 μH
L_m	30 μH
C_r	633 nF
Turn ratio	1:1
L_{add}	25 μH

4. Simulation and Experimental Results

The simulation results show the ZVS capability according to the additional inductance, as shown in Figure 6. The conventional current-fed CLLC resonant converter has no ZVS capability on the bottom side switch. However, the proposed CLLC resonant converter employing the additional inductance can achieve the ZVS condition for both the power switches.
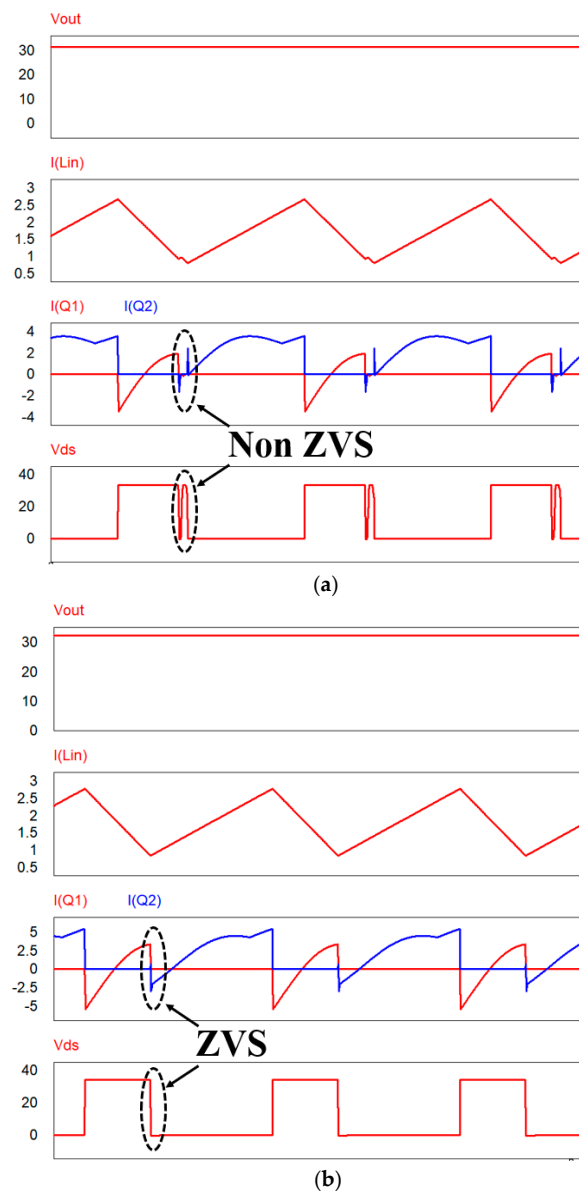
Figure 6. Simulation waveforms to verify ZVS capability: (**a**) Conventional current-fed CLLC resonant converter; (**b**) proposed current-fed CLLC resonant converter.

Figures 7–9 show the steady state waveforms of the conventional CLLC resonant converter according to the input voltage variation and load condition. The duty ratio regulates the output voltage according to the load conditions and input voltages. At the light load condition, it shows the ZVS operation. However, the CLLC resonant converter has a partial and no ZVS operation for the middle load and full load conditions, respectively. For all the input voltage range, the ZVS can be achieved at only the light load condition.
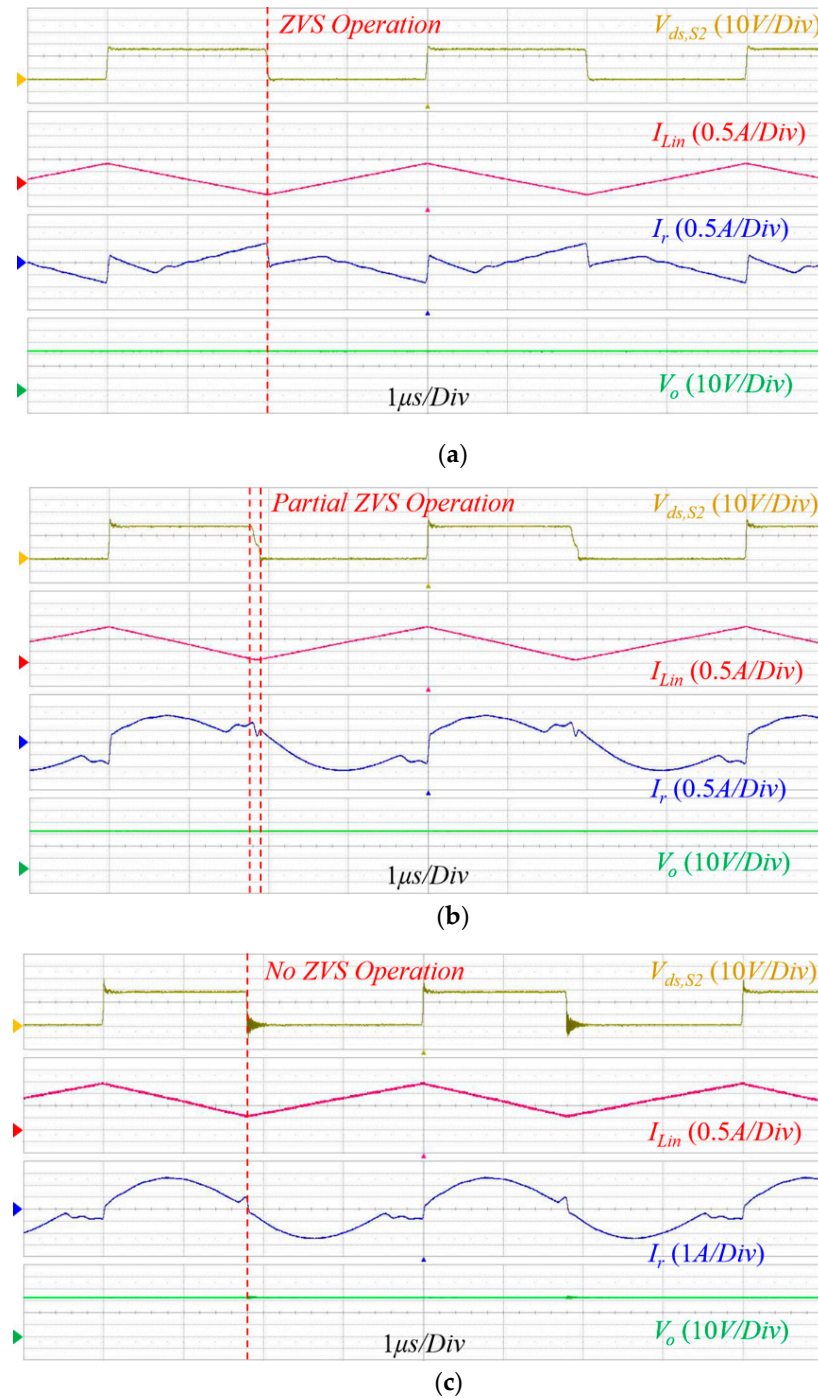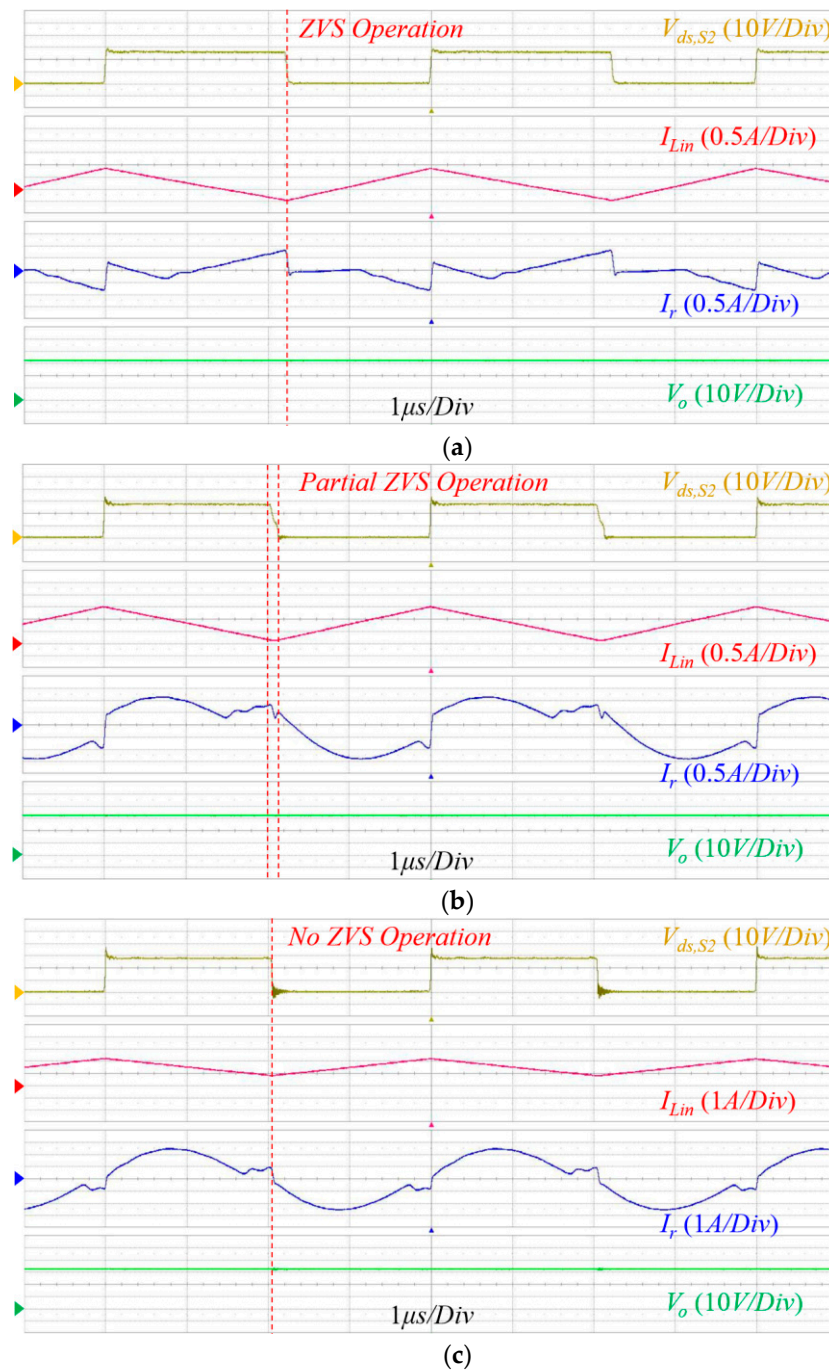

(a)

(b)

(c)

Figure 7. Experimental waveforms of the conventional CLLC resonant converter at 12 V condition: (**a**) 2 W light load condition; (**b**) 10 W middle load condition; (**c**) 20 W full load condition.

Figure 8. Experimental waveforms of the conventional CLLC resonant converter at 14 V condition: (**a**) 2 W light load condition; (**b**) 10 W middle load condition; (**c**) 20 W full load condition.

Figures 10–12 show the steady state waveforms of the proposed CLLC resonant converter according to the input voltages and load conditions. The proposed converter shows the ZVS operation for the entire load and input voltage conditions. The extended soft switching capability improves the power conversion efficiency compared with the partial or no ZVS cases. The power loss of the partial and no ZVS cases can be calculated as follows:

$$P_{noZVS} \cong \frac{1}{2} V_{ds,c} I_{on} t_{on} f_{sw} \tag{10}$$

where P_{noZVS} is the power loss according to the partial or no ZVS conditions, $V_{ds,c}$ is the drain-source voltage at the turn on state, I_{on} is the switch current at the turn on state, t_{on} is the turn on time duration, and f_{sw} is the switching frequency. Figure 13 shows the comparison of the power conversion efficiency between the conventional current-fed CLLC resonant converter and the proposed converter. For the light load condition, the proposed and conventional methods can obtain ZVS capability at the light load condition, which makes no difference in terms of the efficiency. However, the proposed converter has a higher power conversion efficiency for the middle to full load conditions. The maximum improvement of power conversion efficiency is 1% at the middle load condition.
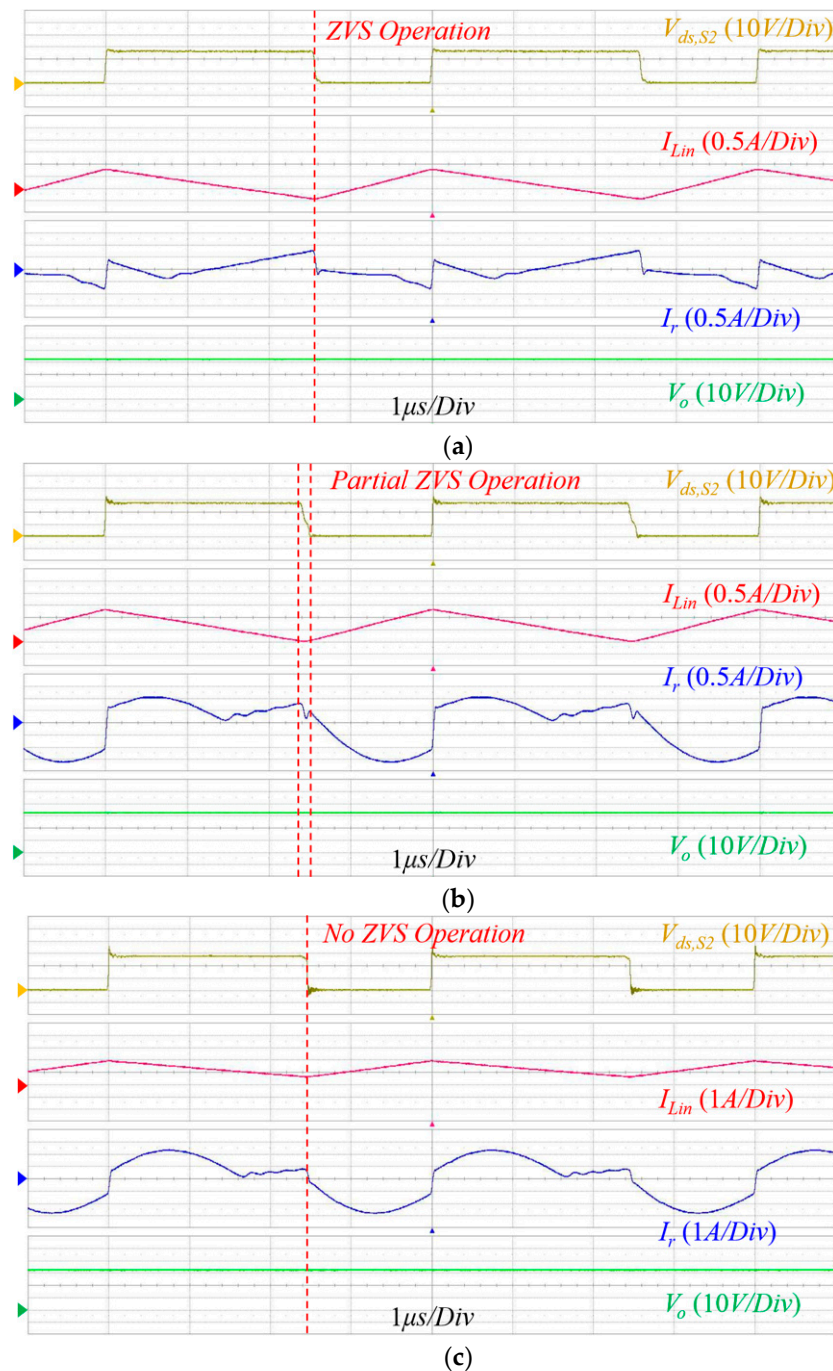

(a)

(b)

(c)

Figure 9. Experimental waveforms of the conventional CLLC resonant converter at 17 V condition: (**a**) 2 W light load condition; (**b**) 10 W middle load condition; (**c**) 20 W full load condition.
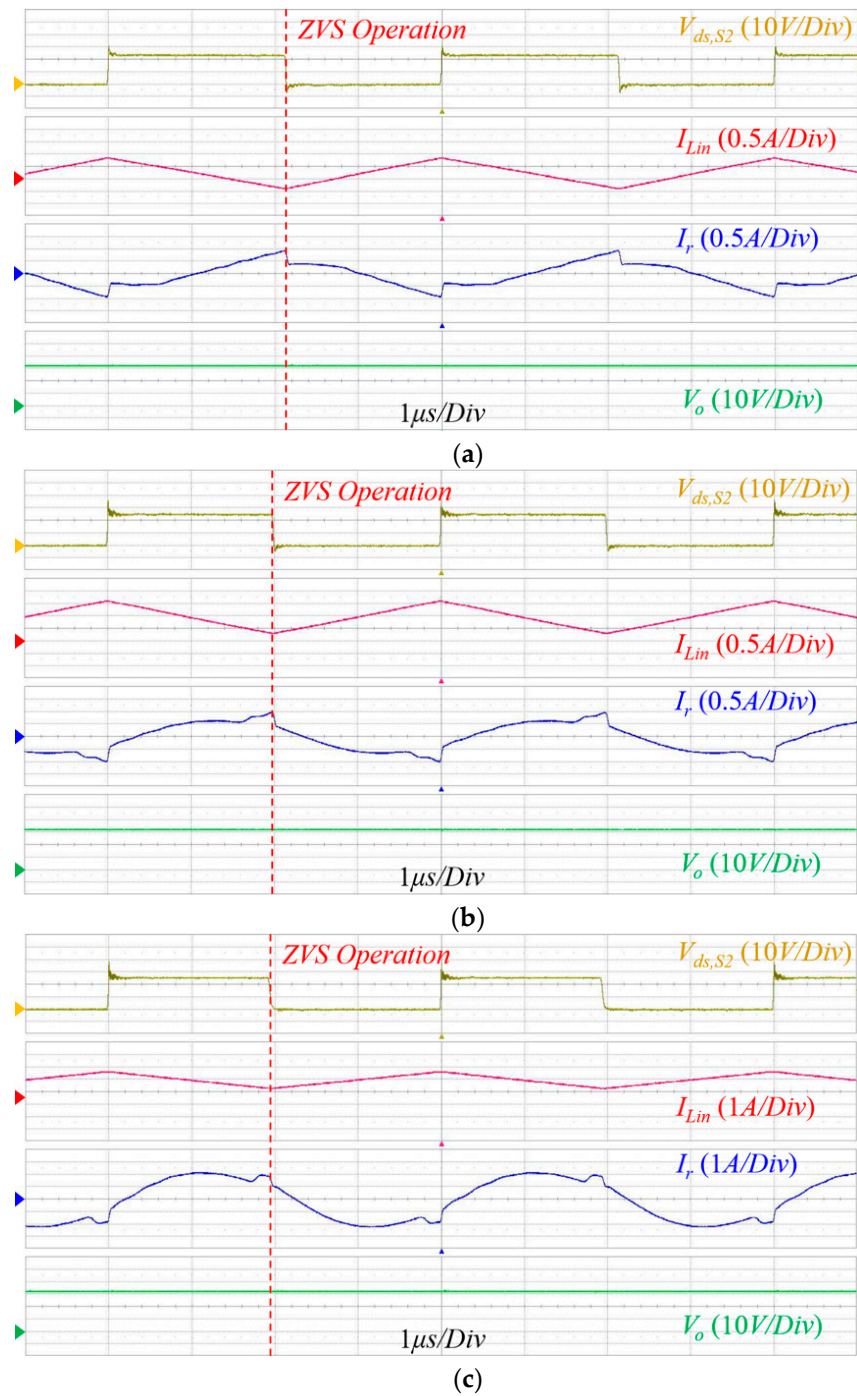
Figure 10. Experimental waveforms of the proposed CLLC resonant converter at 12 V condition:
(**a**) 2 W light load condition; (**b**) 10 W middle load condition; (**c**) 20 W full load condition.
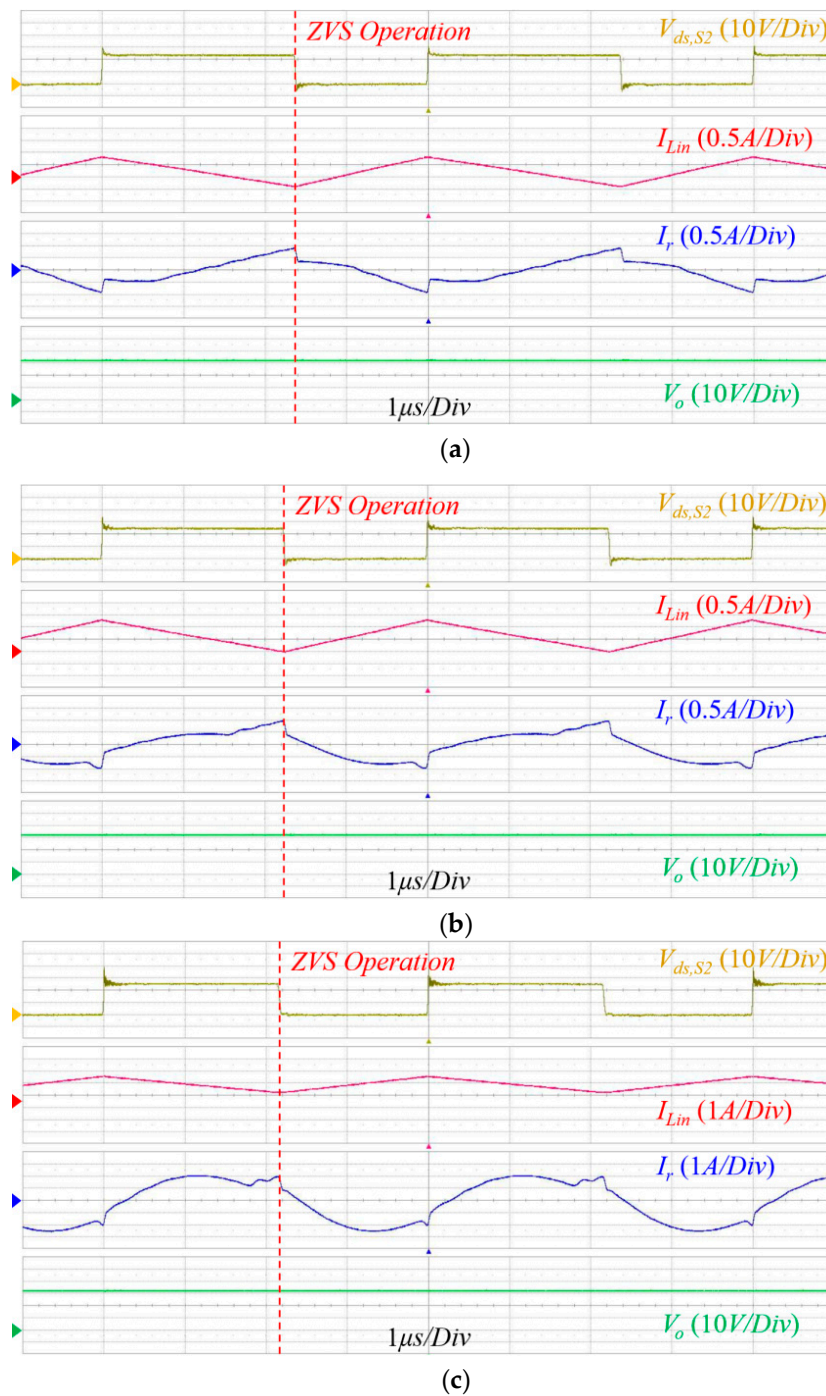
Figure 11. Experimental waveforms of the proposed CLLC resonant converter at 14 V condition: (**a**) 2 W light load condition; (**b**) 10 W middle load condition; (**c**) 20 W full load condition.
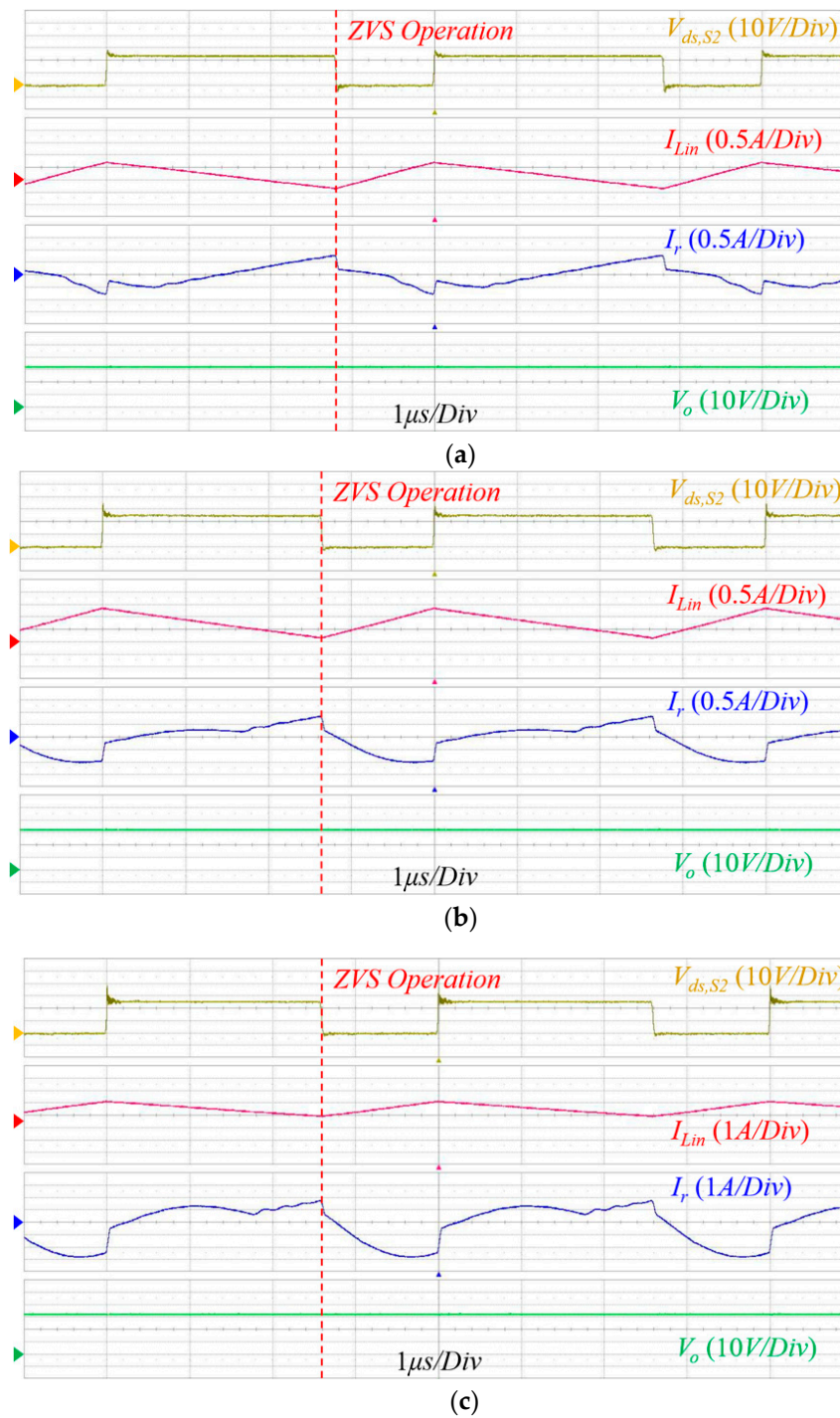
Figure 12. Experimental waveforms of the proposed CLLC resonant converter at 17 V condition: (**a**) 2 W light load condition; (**b**) 10 W middle load condition; (**c**) 20 W full load condition.
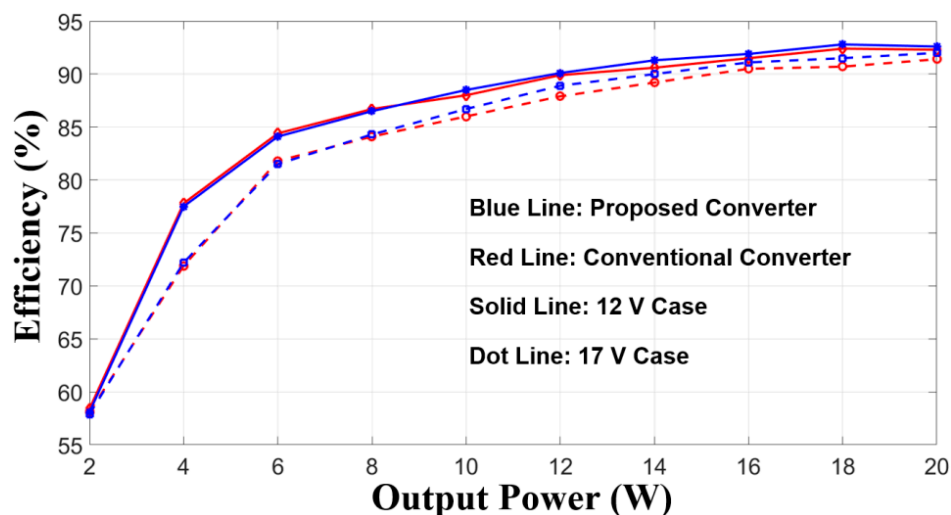
Figure 13. Power conversion efficiency curves.

5. Conclusions

A soft switching capability can improve the power conversion efficiency of the power converter. In this paper, the current-fed CLLC resonant converter employing the additional inductance is proposed to extend the ZVS capability. The operational principle and the design methodology of the additional inductance are analyzed to obtain the soft switching capability for the entire load and input voltage conditions. The simulation and experimental results verify the soft switching performance of the proposed CLLC resonant converter compared with the conventional converter. The maximum efficiency improvement using the proposed converter is 1% at the middle load condition.

Author Contributions: Conceptualization, H.P., J.J.; Methodology, H.P.; Software, H.P.; Validation, H.P.; Resources, D.K., S.B., J.J.; Writing-Original Draft Preparation, H.P.; Writing-Review & Editing, J.J.; Supervision, D.K, J.J.; Project Administration, D.K., S.B.; Funding Acquisition, J.J.

Conflicts of Interest: The authors declare no conflict of interest.

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