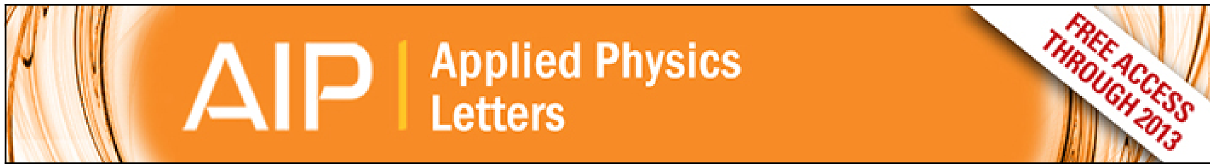

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Citation: Applied Physics Letters **103**, 222102 (2013); doi: 10.1063/1.4833295
View online: http://dx.doi.org/10.1063/1.4833295
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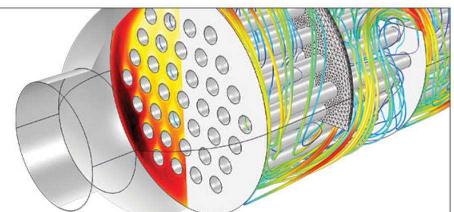

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Silicon-compatible high-hole-mobility transistor with an undoped germanium channel for low-power application

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(Received 11 October 2013; accepted 8 November 2013; published online 25 November 2013)

In this work, Ge-based high-hole-mobility transistor with Si compatibility is designed, and its performance is evaluated. A 2-dimensional hole gas is effectively constructed by a AlGaAs/Ge/Si heterojunction with a sufficiently large valence band offset. Moreover, an intrinsic Ge channel is exploited so that high hole mobility is preserved without dopant scattering. Effects of design parameters such as gate length, Ge channel thickness, and aluminum fraction in the barrier material on device characteristics are thoroughly investigated through device simulations. A high on-current above 30 μA/μm along with a low subthreshold swing was obtained from an optimized planar device for low-power applications. © *2013 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License.*
[http://dx.doi.org/10.1063/1.4833295]

Germanium (Ge) is a material with versatility in both electronics and photonics due to its relatively high electron mobility ($\leq$3900 cm^2/V·s) compared with that of silicon (Si) ($\leq$1500 cm^2/V·s) and its peculiar energy-band structure in that a local conduction band (E_C) minimum exists at the Γ valley ($\mathbf{k} = 0$ in the momentum space).[1] Because of these virtues, Ge has been adopted for a wide range of applications in high-speed electronic devices and group-IV-based optical components.[2–6] Another merit of Ge is found in its prominently high hole mobility among the most prevalent semiconductors used for functional devices as shown in Table I.[1,7–9] Although the smaller energy bandgap ($E_g = 0.8$ eV at the Γ valley and 0.66 eV at the L valley) of Ge offers the opportunity for fabricating photonic components in the infrared regime, it has a drawback in that it makes it more difficult to realize higher electrical reliability and endurance in metal-oxide-semiconductor field-effect transistors (MOSFETs).[10–12] Also, efforts are required prior to gate oxide deposition to passivate the surface to suppress the interface leakage induced by the instability of Ge dangling bonds.[13–15]

In the present study, a high-hole-mobility transistor (HHMT) with an undoped Ge channel is designed and characterized by device simulation.[16] By using an intrinsic Ge channel, there is no loss in hole mobility owing to dopant scattering, and the leakage current by band-to-band tunneling between the channel and drain is significantly reduced. Following the configuration of conventional metal-semiconductor FETs (MESFETs), the high-κ dielectric used as the gate oxide in Ge MOSFETs is replaced by an AlGaAs epitaxial layer due to its small lattice mismatch with Ge, which greatly simplifies the fabrication by eliminating complicated steps for gate oxidation which substantially reduces the mobility degradation owing to surface scattering.[17] Moreover, the AlGaAs/Ge heterojunction is an ideal structure for the effective quantum confinement of holes to form 2-dimensional hole gas (2DHG) due to its large valence band offset ($\Delta E_V = 0.834 + 0.147x$, where x is Al fraction in AlGaAs for $x < 0.45$).[18] At the same time, Ge has higher graftability to Si, which realizes monolithic integration on a Si platform with advanced electronic devices and optical components.[6,19,20]

Figure 1(a) shows the schematic a real view of the simulated Ge HHMT. Gate length (L_G), Ge channel thickness (T_{Ge}), and aluminum (Al) fraction have been treated as the device variables. Al (work function = 4.06 eV) was used for the gate metal. The p-type Si substrate had a doping concentration of 10^{15} cm^{-3} and p^+ source and drain were doped at 10^{19} cm^{-3}. The p^+ AlGaAs barrier had a thickness of 30 nm, and its doping concentration was 10^{18} cm^{-3}. For higher accuracy in the simulation, multiple models including field- and concentration-dependent models, a Shockley–Read–Hall recombination model, and a quantum model were activated in cooperation. Figures 1(b) and 1(c) demonstrate the simulated energy-band diagrams in the vertical (at the device center) and lateral (across the Ge channel) directions, respectively. In each figure, the upper and lower parts show

TABLE I. Comparison of hole mobilities of intrinsic semiconductors (units in cm^2/V·s).

Si	GaAs	InAs	InP	GaN	SiC	Ge
450	400	500	200	300	100	1900

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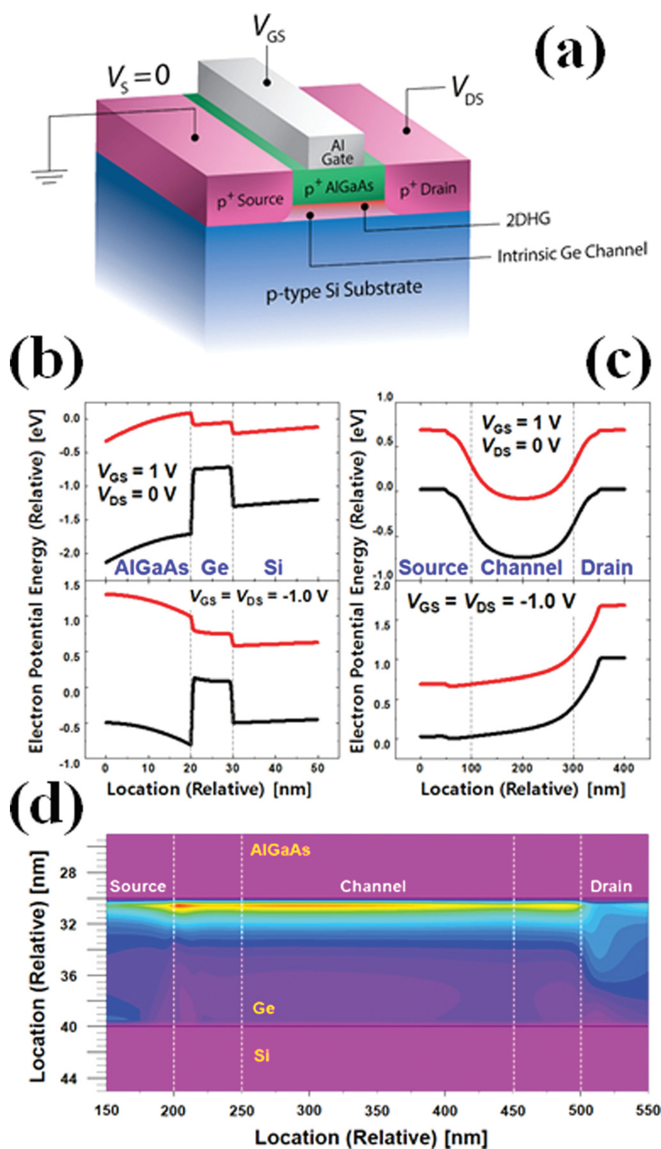

FIG. 1. Device configurations. (a) Areal view of the simulated device. (b) Energy-band diagrams at the device center in the vertical direction (upper: off-state, lower: on-state). (c) Energy-band diagrams along the channel beneath the AlGaAs/Ge interface (upper: off-state, lower: on-state). (d) Formation of 2DHG at the on-state, $V_{GS} = V_{DS} = -1.0$ V.

diagrams in the off- and on-states (off-state: $V_{GS} = 1.0$ V, $V_{DS} = 0$ V; on-state: $V_{GS} = V_{DS} = -1.0$ V). It is assured from the figures that the band arrangement for effective hole confinement is not interrupted in any circumstance, and that the energy barrier seen by the free holes is completely lowered by an operation voltage as small (in magnitude) as -1.0 V. Figure 1(d) illustrates the hole current density obtained by simulation in a magnified view of the intrinsic Ge channel, by which the formation of 2DHG is more tangibly confirmed. From a fabrication point of view, it might be a tricky task to achieve seamless interfacing of the heterojunctions in the HHMT and Ge/Si interface should be more challenging than AlGaAs/Ge site since the lattice mismatch between Ge and Si (4%) is much larger than that between AlGaAs and Ge (within 0.08%). However, it is a relieving feature that the conduction carriers of the HHMT are drifted along the AlGaAs/Ge interface away from Ge/Si interface in its drive mode, and further, a permissibly smooth relaxed Ge/Si interface can be also obtained by a cyclic epitaxy technique combining low-temperature growth and flash annealing.[21]

Figures 2(a)–2(c) show the electrical performances of a Ge HHMT with varying L_G from 500 nm down to 20 nm with other design variables fixed at $T_{Ge} = 10$ nm and Al fraction = 0.3. Figures 2(a) and 2(b) depict the transfer and output characteristics of a device with $L_G = 200$ nm. In the transfer curves, it is observed that gate-induced drain leakage (GIDL) by band-to-band tunneling is effectively suppressed, and a steep subthreshold slope (SS) is obtained. Subthreshold swing (S) is defined as the reciprocal of the maximum instantaneous SS (in absolute value), $S = |[\mathrm{d}(\log_{10}|I_D|)/\mathrm{d}V_{GS}|_{max}]^{-1}|$, as illustrated in the inset. The extracted S under the given condition was less than 80 mV/dec. The output curves are similar to typical curves of p-type MOSFETs (PMOSFETs) and evenly spaced by V_{GS}. Figure 2(c) illustrates collectively the direct-current (DC) parameters as functions of L_G. The on-state current (I_{on}) shows a monotonic increase, while S is degraded as L_G is scaled down, where S values are checked only at the high drain voltage (V_{DS}) = -1.0 V. Threshold voltage (V_{th}) becomes positively higher, and drain-induced barrier lowering (DIBL) increases as L_G shrinks. V_{th} was defined by the constant-current method at a reference I_D of $I_{Ref} = 10^{-7}$ A/μm, and DIBL was extracted mathematically from the amount of V_{th} shift normalized by the V_{DS} change (in

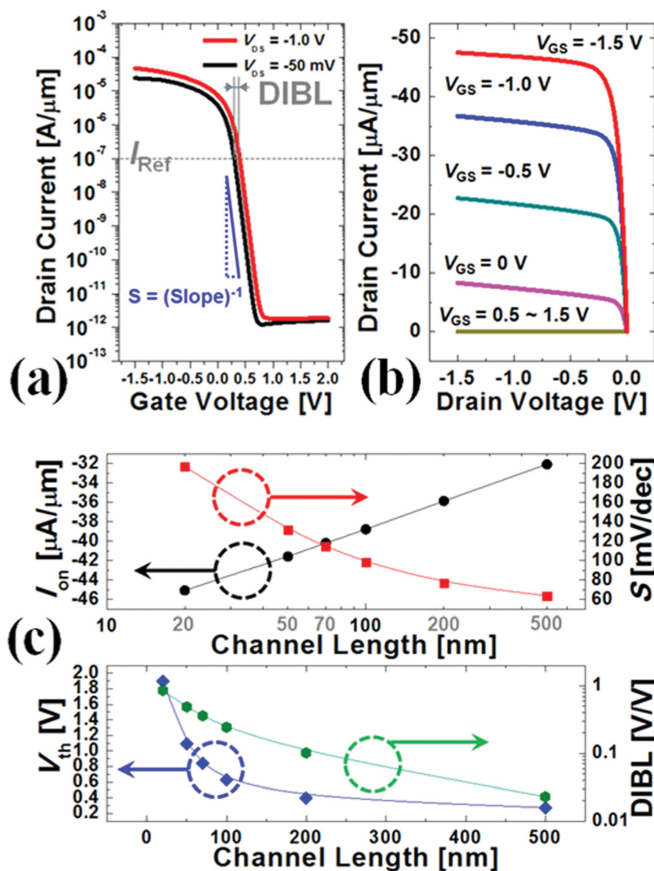

FIG. 2. Electrical characteristics as a function of L_G. Validation of Ge HHMT by (a) transfer and (b) output characteristics from a device with $L_G = 200$ nm, $T_{Ge} = 10$ nm, and Al fraction = 0.3. (c) DC parameters as a function of L_G: I_{on} and S (upper); V_{th} and DIBL (lower) ($T_{Ge} = 10$ nm, Al fraction = 0.3).

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absolute value), $\text{DIBL} = |\Delta V_{th}/\Delta V_{DS}| = |(V_{th}|_{VDS} = -1.0\,\text{V} - V_{th}|_{VDS} = -50\,\text{mV})/[-1.0\,\text{V} - (-50\,\text{mV})]|$ (unit in V/V), as indicated in Fig. 2(a). Although further device optimization by geometrical rendering into a fin-shaped-channel FET (FinFET), double-gate (DG) or multiple-gate (MuG) FET, a nanowire FET would produce improvements in S and DIBL,[22–29] and it is an encouraging fact that high current drivability reaching some tens of amperes per unit width has been obtained from an unaltered in-plane Ge HHMT.

Figures 3(a)–3(c) illustrate the DC parameters for varying T_{Ge} from 5 nm to 100 nm keeping the other variables constant at $L_G = 200$ nm and Al fraction = 0.3. Figure 3(a) depicts I_{on} and current ratio (I_{on}/I_{off}, I_{off}: off-state current) as a function of T_{Ge}. I_{on} shows a monotonic increase with T_{Ge} but the extremely thin channel below 10 nm needs to be avoided to secure sufficient current drivability. It is noticeable that the change in I_{on} by modulating T_{Ge} over 100 nm is much larger than that by L_G scaling over 500-nm range, which implies that controlling T_{Ge} is more steering factor in determining the current drivability of Ge HHMT. However, the current ratio decreases with increasing T_{Ge}, and T_{Ge} should be kept thin below the upper limit to obtain a high current ratio. The trade-off relation between I_{on} and current ratio implies that a large portion of optimal design should be placed on T_{Ge}. S is plotted as a function of T_{Ge} in Fig. 3(b). To obtain a small swing (tentatively, with a reference of 100 mV/dec), T_{Ge} needs to be kept thin below 40 nm. This supports that the swing characteristics of Ge HHMT would be superior to those of Ge PMOSFETs fabricated on Ge bulk substrate. Along with S, I_{off} can also play a role as an index of gate controllability in a thin-body electron device. Figure 3(c) depicts I_{off} as a function of T_{Ge}. I_{off} is linearly scaled with T_{Ge} since I_{off} would be proportional to the area (device width (constant = 1 μm) $\times$ T_{Ge}) normal to hole flux assuming that the gate has complete controllability over the thin Ge channel, which leads to a plot of I_{off} as a linear function of T_{Ge}. I_{off} increases with T_{Ge} linearly up to $T_{Ge} = 30$ nm; however, the plot shows a hyperlinear trend above that thickness, as indicated by the linear and actual lines in Figure 3(c). It is implied that T_{Ge} needs to be falling into the permissible range (green box in the figure) in order to have a strong gate controllability over the channel. Considering the overall

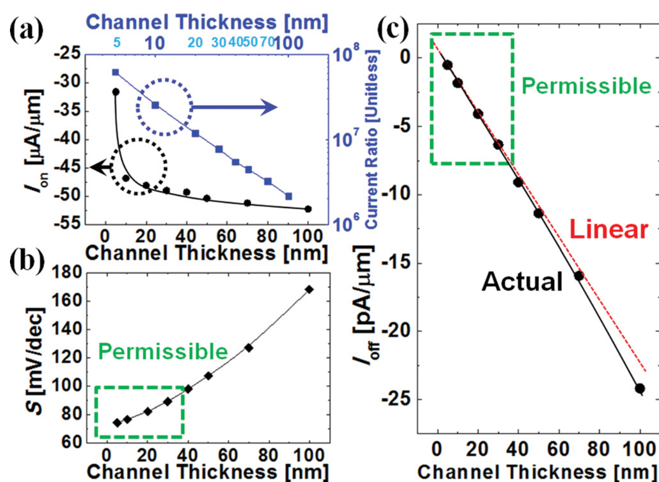

FIG. 3. Electrical characteristics as a function of T_{Ge} ($L_G = 200$ nm, Al fraction = 0.3). (a) I_{on} and current ratio (I_{on}/I_{off}). (b) S. (c) I_{off}.

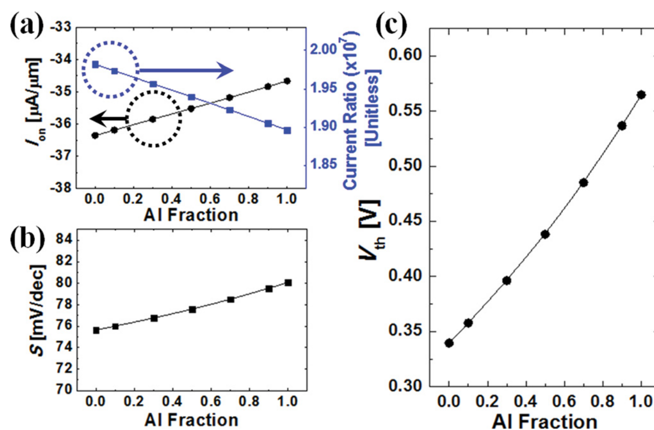

FIG. 4. Electrical characteristics as a function of Al fraction ($L_G = 200$ nm, $T_{Ge} = 10$ nm). (a) I_{on} and current ratio (I_{on}/I_{off}). (b) S. (c) V_{th}.

results, T_{Ge} is a crucial design variable that should be optimally determined, possibly with a permissible range of $T_{Ge} = 10$ nm to 30 nm, for higher current drivability and strong gate controllability.

Figures 4(a)–4(c) demonstrate the effects of the Al fraction in the AlGaAs barrier material on the current characteristics of the Ge HHMT. The other variables were kept constant at $L_G = 200$ nm and $T_{Ge} = 10$ nm. Compared with the previous two design variables, the Al fraction has a relatively small effect on the device performance. The change in I_{on} was as small as 2 μA/μm, and the current ratio also showed a small change of 10^5, which is below a percent order change compared with the base value of 10^7 over the full sweep of the Al fraction from 0 to 1, as shown in Figure 4(a). S is also almost invariable with the Al fraction, as shown in Figure 4(b), where the change in S is found to be only 3 mV/dec by the full scaling of the Al fraction. A relatively more distinguishable change is observed by modulating the Al fraction in the V_{th} shift, as plotted in Figure 4(c). However, its effect on V_{th} is still smaller than that of another variable, L_G. These results ensure that the electrical performance of the Ge HHMT has a strong tolerance against deviation in the Al fraction that might occur during the epitaxy process; this is another advantage of the device, even from a more practical point of view.

We optimally designed a silicon-compatible AlGaAs/Ge/Si heterojunction HHMT considering the channel length, channel thickness, and Al fraction of the barrier. It has been confirmed that an effective quantum confinement of holes forming a 2DHG was achieved by the material system, which confirms the feasibility of the device for low-power applications. Improved reliability, simpler fabrication, higher current drivability that eliminates both dopant and surface scattering, and stronger process tolerance make the Ge HHMT favorable and highly competitive with conventional Si CMOS and Ge PMOSFETs.

This work was supported by the Center for Integrated Smart Sensors funded by the Korean Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186) and by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (Grant No. 2012-0009594).

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[1]S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (John Wiley & Sons, Inc., New York, 1981), pp. 13, 849.
[2]C. R. Selvakumar and B. Hecht, IEEE Electron Device Lett. **12**, 444 (1991).
[3]Y. Kamata, Mater. Today **11**, 30 (2008).
[4]Y.-H. Kuo, Y. K. Lee, Y. Ge, S. Ren, J. E. Roth, T. I. Kamins, D. A. B. Miller, and J. S. Harris, Nature **437**, 1334 (2005).
[5]O. Fidaner, A. K. Okyay, J. E. Roth, R. K. Schaevitz, Y.-H. Kuo, K. C. Saraswat, J. S. Harris, Jr., and D. A. B. Miller, IEEE Photonics Technol. Lett. **19**, 1631 (2007).
[6]S. Cho, B.-G. Park, C. Yang, S. Cheung, E. Yoon, T. I. Kamins, S. J. B. Yoo, and J. S. Harris, Jr., Opt. Express **20**, 14921 (2012).
[7]C. Claeys and E. Simoen, *Germanium-Based Technologies: From Materials to Devices* (Elsevier, Oxford, 2007), p. 368.
[8]D. J. As, D. Schikora, A. Greiner, M. Lubbers, J. Mimkes, and K. Lischka, Phys. Rev. B **54**, R11118 (1996).
[9]W. J. Schaffer, H. S. Kong, G. H. Negley, and J. W. Palmour, *Proceedings of the 5th Conference on Silicon Carbide and Related Materials,* Institute of Physics Conference Series Vol. 137, edited by M. G. Spencer (Institute of Physics Publishing, London, 1994), pp. 155–159.
[10]M. K. Husain, X. V. Li, and C. H. de Groot, IEEE Trans. Electron Devices **56**, 499 (2009).
[11]C.-W. Chen, C.-T. Chung, J.-Y. Tzeng, P.-H. Li, P.-S. Chang, C.-H. Chien, and G.-L. Luo, IEEE Trans. Electron Devices **60**, 1334 (2013).
[12]W. Rindner, Appl. Phys. Lett. **6**, 225 (1965).
[13]S. J. Whang, S. J. Lee, F. Gao, N. Wu, C. X. Zhu, J. S. Pan, L. J. Tang, and D. L. Kwong, Tech. Dig.-Int. Electron Devices Meet. **2004**, 307–310.
[14]W.-S. Jung, J. H. Nam, J.-Y. J. Lin, S. Ryu, A. Nainani, and K. C. Saraswat, in *Proceedings of 2012 International Silicon-Germanium Technology and Device Meeting (ISTDM), Berkeley, USA, 4–6 June 2012* (The Institute of Electrical and Electronics Engineers, 2012), pp. 1–2.
[15]M. Zhao, R. Liang, J. Wang, and J. Xu, Appl. Phys. Lett. **102**, 142906 (2013).
[16]Atlas User's Manual: Device Simulation Software (Silvaco, Inc., Santa Clara, USA, 2013).
[17]W. Liu, *Fundamentals of III-V Devices: HBTs, MESFETs, and HFETs/HEMTs* (John Wiley & Sons, Inc., New York, 1999), pp. 330–345.
[18]J. S. Harris, Jr., *Class Notes from EE327 Properties of Semiconductor Materials* (Stanford University, 2013).
[19]S. Cho, S. H. Park, B.-G. Park, and J. S. Harris, Jr., in *Proceedings of 2011 International Semiconductor Device Research Symposium (ISDRS), College Park, USA, 7–9 December 2011* (The Institute of Electrical and Electronics Engineers, 2011), pp. 1–2.
[20]S. Cho, I. M. Kang, T. I. Kamins, B.-G. Park, and J. S. Harris, Jr., Appl. Phys. Lett. **99**, 243505 (2011).
[21]A. Nayfeh, "Heteroepitaxial Growth of Relaxed Germanium on Silicon," Ph.D. dissertation (Stanford University, 2006).
[22]International Technology Roadmap for Semiconductors (ITRS), 2011 ed., Process Integration, Devices & Structures (PIDS) Chapter (2011).
[23]B.-G. Park, S. W. Hwang, and Y. J. Park, *Nanoelectronic Devices* (Pan Stanford Publishing Pte. Ltd., Singapore, 2012), pp. 228–239, 274–283.
[24]B.-G. Park, J. Y. Song, J. P. Kim, H. Jeong, J. H. Lee, and S. Cho, Microelectron. J. **40**, 769 (2009).
[25]Y. Taur, IEEE Electron Device Lett. **21**, 245 (2000).
[26]J. S. Lee, S. Cho, B.-G. Park, J. S. Harris, and I. M. Kang, J. Semicond. Technol. Sci. **12**, 230 (2012).
[27]M.-S. Lee, S.-M. Joe, J.-G. Yun, H. Shin, B.-G. Park, S.-S. Park, and J.-H. Lee, J. Semicond. Technol. Sci. **12**, 360 (2012).
[28]C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, Appl. Phys. Lett. **94**, 053511 (2009).
[29]P. Razavi and G. Fagas, Appl. Phys. Lett. **103**, 063506 (2013).

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