

Practical Design of Dual Active Bridge Converter as Isolated Bi-directional Power Interface for Solid State Transformer Applications

Hyun-Jun Choi* and Jee-Hoon Jung[†]

Abstract – As a bi-directional isolated interface for solid state transformer applications, practical design considerations of a dual active bridge (DAB) converter are proposed by means of a detailed mathematical model based on the converter’s steady state operations. The DAB converter is useful in isolated bi-directional power conversion applications due to high performance, high efficiency, and bi-directional control manner. However, design considerations should be taken into account to overcome the disadvantages of DAB converter, such as low efficiency caused by restricted soft switching capability at light load conditions and high circulating current at heavy load conditions. The practical design considerations of the converter’s power stage will be discussed to maximize soft switching capability and to minimize the conduction losses. In addition, to reduce the current stress of the power devices during a cold start sequence, an effective soft start algorithm will be proposed. Experimental results with a 3.3 kW prototype DAB converter will be given in order to validate the effectiveness of the proposed design considerations.

Keywords: Solid State Transformer (SST), Dual Active Bridge (DAB) Converter, Bi-directional power conversion, Soft start algorithm, Zero Voltage Switching (ZVS)

1. Introduction

Recently, over-dependency on the fossil fuels has created pollution, environmental damage, and, eventually, resource depletion problems. In addition, global warming is becoming a larger concern, and the electricity energy shortage problem can cause blackouts [1-3]. To address these problems, the demand for green energy continues to increase. Since green energy does not negatively influence the environment and uses renewable power sources, its application has become a significant research topic. Further, the smart-grid, micro/nano-grids and DC distribution systems are also critical issues in today’s world market.

In particular, the solid state transformer (SST) has been actively studied, which is one of the key technologies for the smart-grid, micro/nano-grid, and DC distribution systems. As shown in Fig. 1, the SST is a bi-directional power conversion component that is used to interface a conventional AC grid with an AC/DC microgrid. Besides, the SST can be an alternative to substitute the old-fashioned line-frequency (50 Hz/60 Hz) transformer [1, 4-5]. The weight and volume of the conventional transformers are heavy and bulky. Moreover, it is also a totally passive, causing reactive power. For these reasons, the applications of traditional transformers are very restrictive [6-8]. The

SST can solve the problems of the line-frequency transformer by using a high frequency transformer with reactive power control. Furthermore, the SST has other advantages such as instantaneous voltage regulation, power factor correction, higher power density and systems protection capability. Fig. 2 shows that the SST consists of three parts: a bi-directional AC-DC rectifier, an isolated bi-directional DC-DC converter (IBDC), and a bi-directional DC-AC inverter.

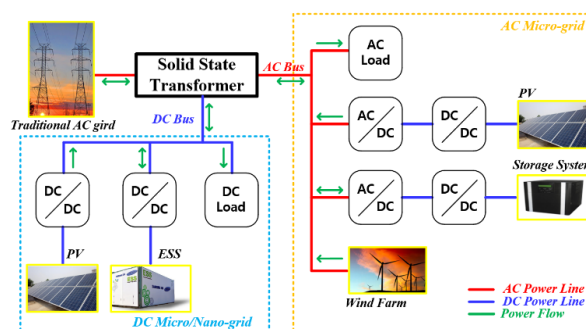


Fig. 1. Structure of AC/DC microgrid system based on SST.

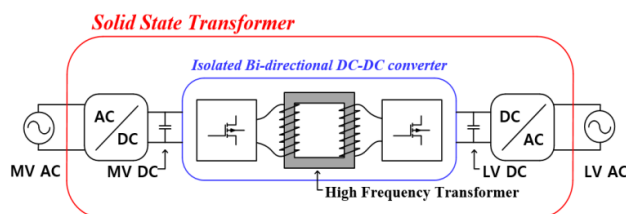


Fig. 2. Structure of SST with three power stages.

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The IBDC is one of the critical parts in the SST that is necessary to control the power flows and regulate the DC bus voltage. As one of based on isolated bi-directional bridge type topologies, the dual active bridge (DAB) converter has advantages, such as wide output voltage ranges and high efficiency. Particularly, based on a phase-shift modulation (PSM), the DAB converter can smoothly control the bi-directional power flows under a seamless voltage regulation manner. In addition, the DAB topology can reduce the switching losses by the inherent zero voltage switching (ZVS) capability. However, the DAB converter has disadvantage, such as high switching losses due to ZVS inadequacy at light load conditions and high conduction losses caused by high circulating current under heavy load conditions.

In this paper, to improve the performance of the DAB converter, a well-organized design methodology will be proposed. In Section II, operation principles of the DAB converter will be introduced briefly. In addition, practical design considerations of proper coupling inductance will be proposed to improve overall efficiency using RMS current analysis. To guarantee the maximum ZVS capability, effective dead time criterion will be determined based on a mathematical model. In Section III, a soft start algorithm will be proposed to suppress overcurrent stress of the power switches during the start-up sequence. Finally, in Section IV, the proposed DAB converter design methodology will be verified by experimental data using a 3.3 kW prototype converter.

2. Design Methodology

Fig. 3 shows the schematic of the DAB converter. The DAB converter need to eliminate this parts, which is unnecessary consists of two single-phase symmetrical H-bridges with a coupling inductor. For the SST applications, a high frequency transformer with 1:1 turn-ratio is applied in the converter. For a simplicity in the converter analysis, the magnetizing current is ignored by assuming a perfect transformer.

2.1 Operation principles of the DAB converter

The operational principle of the DAB converter is

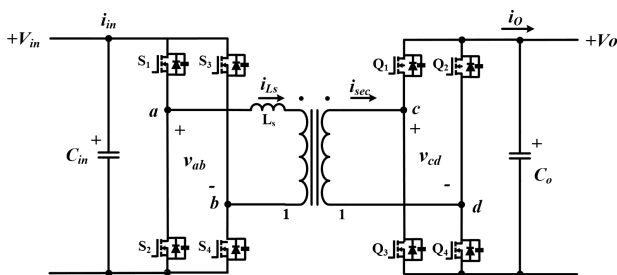


Fig. 3. Schematic of the DAB converter.

simple and similar to the case of the phase-shift full bridge converter. As shown in Fig. 4, the DAB converter can achieve the ZVS when switches are turning on with sufficient negative primary current [9-11]. The steady state operation of the DAB converter is divided into two modes: forward and backward according to the current directions. Power is transferred from the leading bridge to the lagging bridge, and the two square waves are properly phase shifted to control the power flows. Output voltage can be regulated from the difference between the two H-bridge voltages, which is applied over the coupling inductance (L_S) in the Fig. 3. The coupling inductance which is sum of the leakage inductance in the transformer and the external inductance acts as an energy transfer device [10-14].

2.2 Coupling inductance current analysis

Since the coupling inductance is a dominant parameter as the energy transfer component in the DAB converter, the analysis of the coupling inductor current becomes important in the operational principle of the DAB converter [10-12, 15]. Fig. 5 indicates the detail waveforms of the coupling inductor current, i_{LS} , in Fig. 4. From Fig. 5, each corner current i_1 and i_2 are derived as follows in (1) and (2):

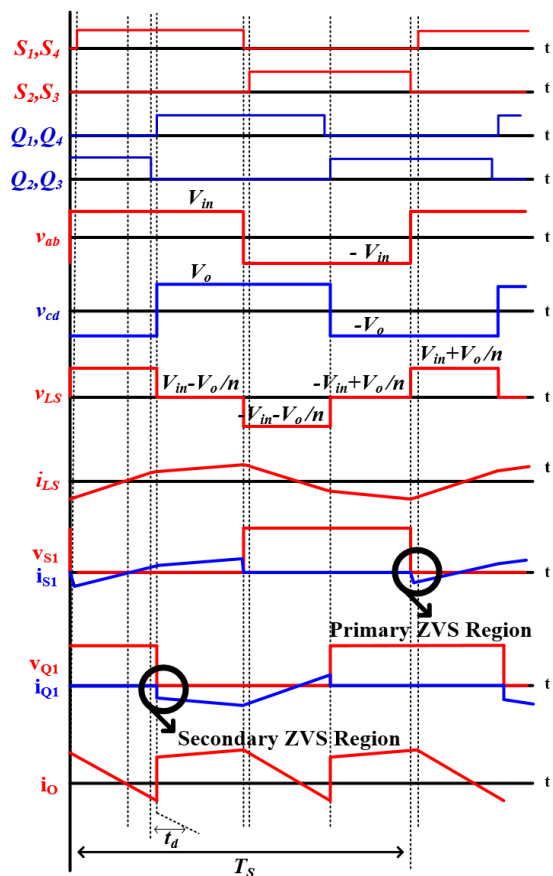


Fig. 4. Theoretical waveforms of the DAB converter in the forward power flow.

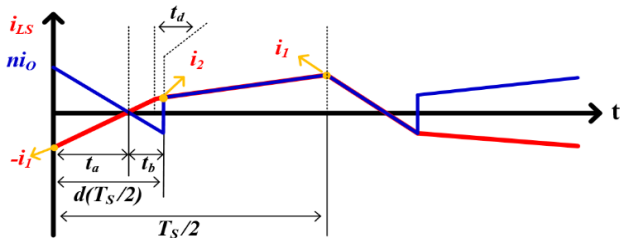


Fig. 5. Theoretical waveforms of the coupling inductor current and the average output current

$$i_1 = \frac{T_S}{4L_S} \left[(2d-1) \frac{v_o}{n} + v_{in} \right] \quad (1)$$

$$i_2 = \frac{T_S}{4L_S} \left[(2d-1) v_{in} + \frac{v_o}{n} \right] \quad (2)$$

where T_S is the switching period, d is the amount of phase-shift radian/ π , n is the turn ratio and L_S is the coupling inductance. By using the corner values of the coupling inductor current, as shown in Fig. 5, the average input current, $I_{in,a}$, and the average output current referred to the transformer primary side, $I_{o,a}$, can be derived as (3) and (4), respectively [12].

$$I_{in,a}(t) = \int_{\frac{T_S}{2}} i_{in}(t) dt = \frac{2}{T_S} \left[-\frac{1}{2} i_1 t_a + \frac{1}{2} i_2 t_b + \frac{1}{2} (i_1 + i_2) (1-d) \frac{2}{T_S} \right] \\ = \frac{V_o d (1-d) T_S}{2nL_S} \quad (3)$$

$$I_{o,a}(t) = \int_{\frac{T_S}{2}} n i_o(t) dt = \frac{2}{T_S} \left[\frac{1}{2} i_1 t_a - \frac{1}{2} i_2 t_b + \frac{1}{2} (i_1 + i_2) (1-d) \frac{2}{T_S} \right] \\ = \frac{V_{in} d (1-d) T_S}{2nL_S} \quad (4)$$

Theoretically, from (3) and (4), the maximum output power of the DAB converter can be obtained at 50% phase-shift between the two H-bridges; however, proper dead time should be considered for the ZVS conditions of the power switches and preventing the shoot-through faults. From (1) to (4), the optimal value of the coupling inductance, L_S , and the proper value of the dead time duration, t_d , can be derived.

2.3 Proper design of coupling inductance

The output power should be considered to design the proper coupling inductance. From (3) and (4), the gain formula and the output power of the DAB converter can be expressed as (5) and (6), respectively:

$$M = \frac{V_o}{nV_{in}} = \frac{I_{o,a} R}{nV_{in}} = \frac{T_S R d (1-d)}{2n^2 L_S} = k(1-d)d \quad (5)$$

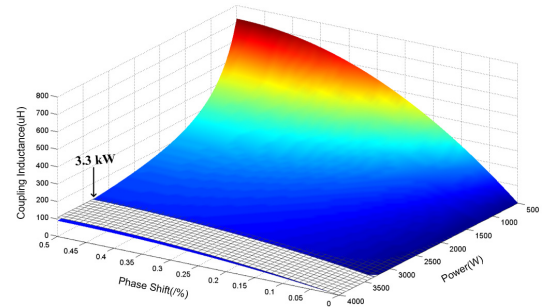


Fig. 6. Coupling inductance graph between the transfer power and the phase-shift

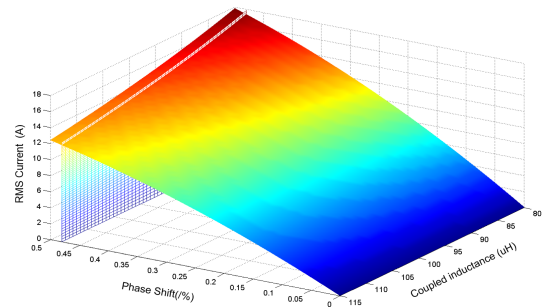


Fig. 7. RMS current graph between the coupling inductance and the phase-shift

$$P_{out} = k V_{in} V_o (1-d) d \frac{n}{R} \quad (6)$$

where R is the load resistance and k is defined in (7).

$$k = \frac{T_S R}{2n^2 L_S} = \frac{P_{out}}{v_o v_{in} (1-d) d \frac{n}{R}} \quad (7)$$

Using (5), (6), and (7), a proper design criterion of the coupling inductance can be derived as follows:

$$L_S \leq \frac{V_{in} d_{max} (1-d_{max}) T_S R_{min}}{2nV_o} \quad (8)$$

where the d_{max} is the maximum phase gap between primary and secondary legs and R_{min} is the minimum load resistance.

Fig. 6 illustrates coupling inductance variations according to the maximum power transfer and the amount of the phase-shift. It shows that smaller coupling inductance can transfer the higher power in the DAB converter. However, the smaller coupling inductance also can induce the higher conduction losses due to the higher RMS current expressed as shown in (9).

$$I_{RMS} = \frac{T_S}{8L_S} \left(v_{in} - \frac{v_o}{n} \right) \left[\left(v_{in} - \frac{v_o}{n} \right)^2 + \frac{4v_{in} v_o d (2-d)}{n} \right] \quad (9)$$

Fig. 7 shows RMS current variation according to the coupling inductance and the amount of the phase-shift. The RMS current is inversely proportional to the coupling inductance. Therefore, considering (8) and (9), a proper coupling inductance value should be determined.

2.4 Dead time duration for soft switching

One of design difficulties of the DAB converter is low efficiency under light load conditions caused by limited ZVS capability. This induces hard switching of the power switches, which reduces the overall power conversion efficiency. To ensure the maximum ZVS region, sufficient time for charge and discharge process of the power MOSFETs' output capacitance should be guaranteed, which requires an optimal dead time duration. In previous research, traditional dead time duration has already been derived as a necessary condition; however, they did not consider charging and discharging speed of the output capacitance [13-15].

Since the dead time should be longer than the charging and discharging duration of the MOSFETs' output capacitance, the dead time condition can be derived as follows [16]:

$$4C_p v_{max} \leq i_c t_d \cong \min(i_1, i_2) t_d \tag{10}$$

where v_{max} is the maximum voltage applied to the switches, C_p is the output capacitance, i_c is the current passing through the output capacitors, and i_1 and i_2 are the corner values of the coupling inductor current in Fig. 5. It is assumed that i_c is constant during the dead time duration which is short enough. Consequently, the ZVS of the power MOSFETs can be guaranteed by the accurate dead time duration described as follows:

$$t_d \geq 16C_p L_s \frac{f_s}{M(1-d_{max})+1} \tag{11}$$

where f_s is the switching frequency.

3. Soft Start Algorithm

A conventional control method of the DAB converter uses the fixed duty ratio with the consideration of dead time which is applied to each power switch. The phase of the pulse width modulated (PWM) signal is shifted between the primary and secondary sides to regulate the output voltage. This control manner is so-called the PSM [10-11, 14]. However, this output voltage control strategy is limited to only the steady-state operation of the converter. During a cold start sequence, the PSM directly transfers electric power from the primary side to the output capacitors. It causes inrush current due to rapidly charging

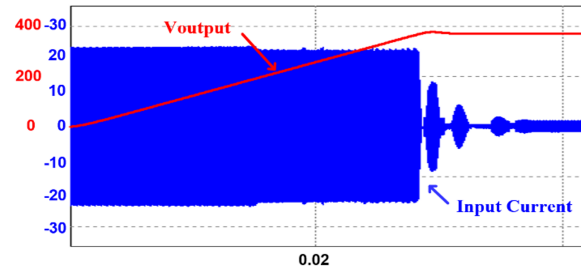


Fig. 8. Simulated inrush current of the DAB converter at the cold start duration

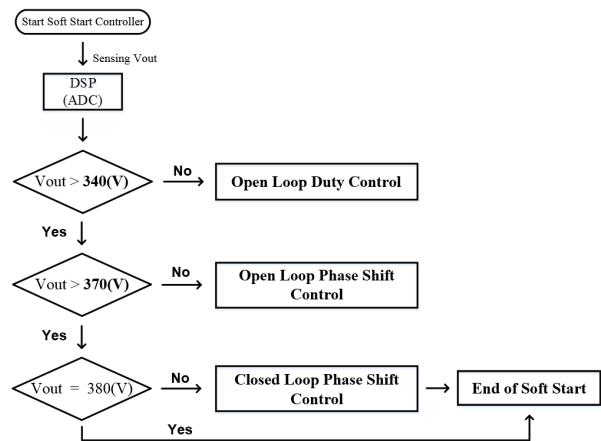


Fig. 9. The control diagram of the proposed three sequences soft start algorithm

the output capacitor regardless of the phase-shift condition in the DAB converter. It can be one of the reasons why the inrush current induces stress and heat, causing the power switches to breakdown in the DAB converter. Fig. 8 shows the simulation results using the PSIM software. It shows output voltage and input current waveforms at the cold-start state with only normal feedback control. When the output voltage rises quickly, the high inrush current fugitively flows through the switches. To reduce the stress from the inrush current, a soft start algorithm is required.

3.1 Concepts of soft start algorithm

To address the problems of the high inrush current during cold-start state, a soft start algorithm is proposed. As shown in Fig. 9, the algorithm is divided into the three sequence in terms of output voltage levels: an open loop duty control (OPDC), an open loop phase-shift control (OLPSC), and a closed loop phase-shift control (CLPSC). According to the output voltage level, proper control algorithms are selected to suppress the inrush current under the cold start sequence.

3.2 Open loop phase control

At the initial state, the OLDC is applied to the DAB

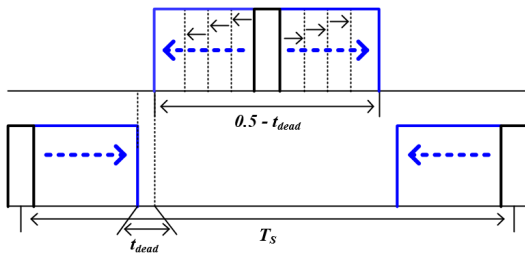


Fig. 10. Operational principle of the proposed open loop duty (OLD) algorithm

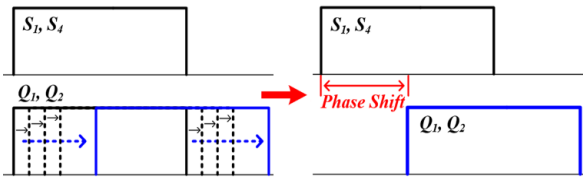


Fig. 11. Operational principle of the proposed open loop phase-shift (OLPS) algorithm

converter. Fig. 10 shows the process of the OLDC. At the beginning state, the duty ratio is not fixed as 0.5 but linearly increased from zero to 0.5. This control is the same as the full-bridge converter PWM control manner, used to regulate the output voltage. The OLDC makes input current increase softly and reduces the peak value of the inrush current. Using the OLDC in the ideal case, the output voltage can effectively reach the reference voltage. However, due to parasitics, the target output voltage may not be reached. Therefore, to obtain the expected output voltage, the control mechanism should be improved.

The most suitable method is feedback control to regulate the output voltage to the reference. However, if the feedback control is achieved immediately after the OLDC, it can also cause high primary currents. This is because the phase of the gate signal, as a result of the OLDC, will be shifted in an instant. To prevent fast variations of the phase gap between the primary and secondary legs, the OLPS is proposed. As shown in Fig. 11, the OLPS algorithm makes the linear increase of the phase gap degree proportional to time duration. The OLPS leads to reach the output voltage to the reference smoothly, and decreases peak inrush current simultaneously.

3.3 Closed loop phase control

After the overall open loop soft start controls are finished, the feedback controller starts to regulate the exact output voltage. The CLPSC is the normal feedback control algorithm of the DAB converter, which uses the difference between output and reference voltage. The key of the CLPSC in the proposed soft start algorithm is when the feedback controller starts in steady state operation. Fig. 12 shows the comparison of two CLPSC starting point cases.

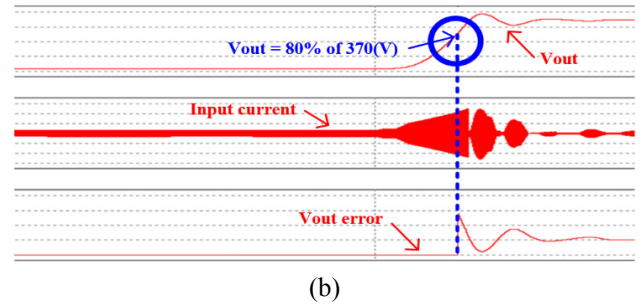
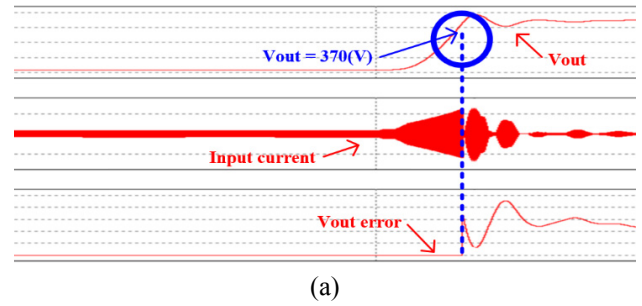


Fig. 12. Comparison of feedback control starting points: (a) After open loop control; (b) Before open loop control

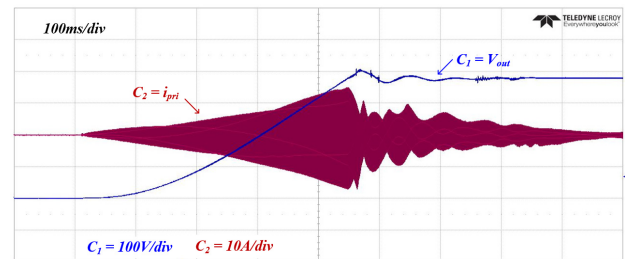
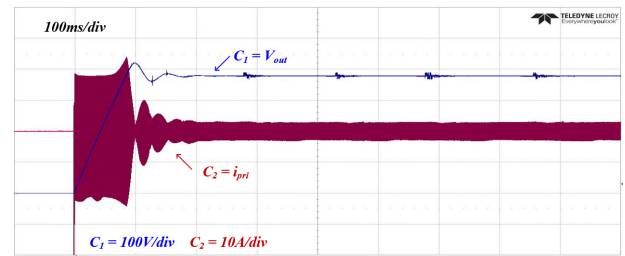


Fig. 13. Comparison of cold start waveforms: (a) Without the soft start algorithm; (b) With the soft start algorithm

Fig. 12 (a) indicates the waveform when the feedback control begins immediately after the overall open loop controls are ended. Fig. 12 (b) presents that the feedback control starts when the output voltage comes to 80% of the expected reference voltage. In case of Fig. 12 (b), the feedback controller accumulates and updates the errors before finishing the OLPS. Although the latter has higher complexity and computational burden than the case of the

former, the peak current in latter is reduced about 3%.

Fig. 13 shows the comparison of the overall DAB converter cold start waveforms which are with/without the proposed soft start algorithm. Even though the settling time is extended, the RMS inrush current decreases from 14.45 A to 8.39 A when the soft start algorithm is implemented. In other words, the proposed soft start algorithm makes almost 41 % reduction of RMS current. Also, the peak value of the inrush current decreases almost 8 A during the cold start.

Table 1. Design specification of the DAB converter

Power	3.3 kW
Input Voltage	380 V
Output Voltage & Current	380 V, 8.7 A
Frequency	50 kHz
$d(\text{degree})/180^\circ$	$-0.48 < \phi < 0.48$
Coupling Inductance	102 μH
Dead time duration	$t_{\min} = 0.52 \mu\text{s}$
Length of air-gap	1.53 mm
Magnetizing inductance	567.66 μH
Turn Ratio	1:1
The Number of turns	26 turns
B_{\max}	0.39 T
Core	EE656S

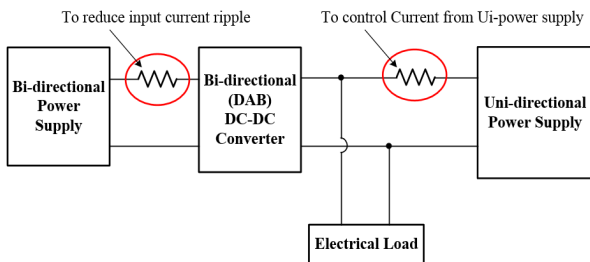


Fig. 14. Schematic of test condition in bi-directional power flows

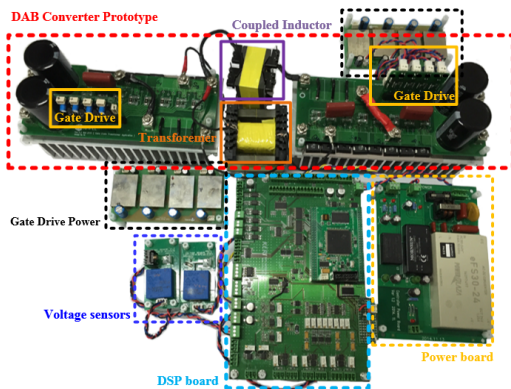
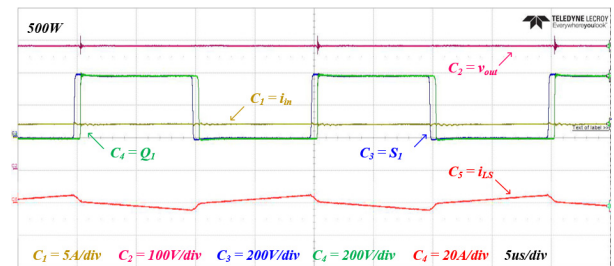


Fig. 15. Photograph of the 3.3 kW prototype DAB converter

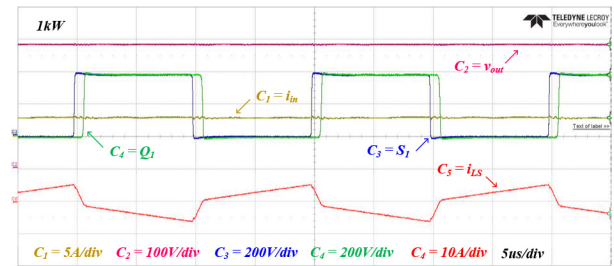
4. Experimental Results

Table 1 indicates the specifications of the target experimental conditions and the prototype converter.

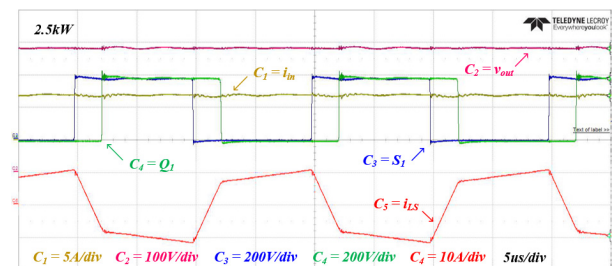
Following the suggested design guides, $t_d (= 0.52 \mu\text{sec})$ and $L_S (= 102 \mu\text{H})$ are selected. Particularly, the coupling inductance is selected as 102 μH based on the power rating and RMS current, as shown in Fig. 6 and Fig. 7. Fig. 14 shows the bi-directional power flows test condition. The resistor in front of the DAB converter is required to suppress the input current ripple. Another resistor which is connected to the output stage of the DAB converter is required to make a current source from a uni-directional power supply. Fig. 15 shows the 3.3 kW prototype DAB converter. It consists of a power stage board, a DSP board,



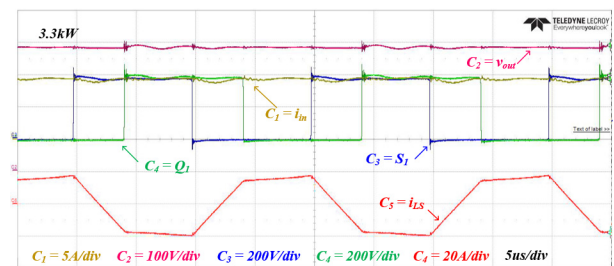
(a)



(b)



(c)

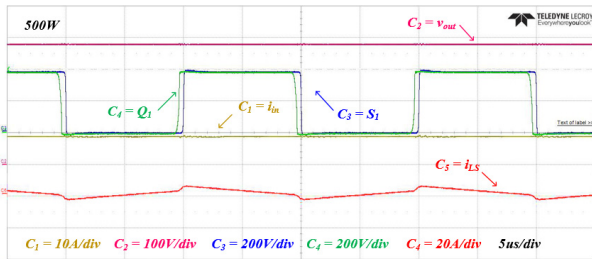


(d)

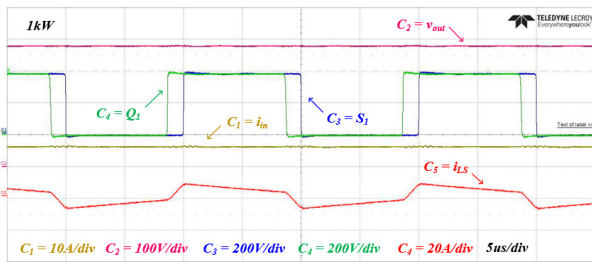
Fig. 16. Experiment waveforms of forward power flow according to power ratings: (a) 500 W; (b) 1 kW; (c) 2.5 kW; (d) 3.3 kW

voltage sensor boards, gate drivers, and auxiliary power supplies. The same PCB boards are applied on each transformer side due to the symmetric configuration. To get robustness against noise and disturbance, the high voltage ceramic capacitors are connected both high and low side legs. To suppress noise and stray inductance, the gate drives are located very close to the power switches.

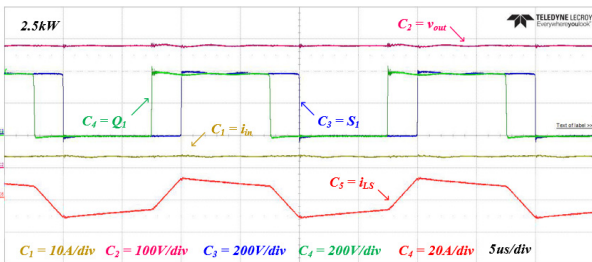
Fig. 16 and 17 indicate the bi-directional power flows experimental results in forward and backward conditions, respectively. Each result is measured according to load variations from 500 W to 3.3 kW. The input voltage is



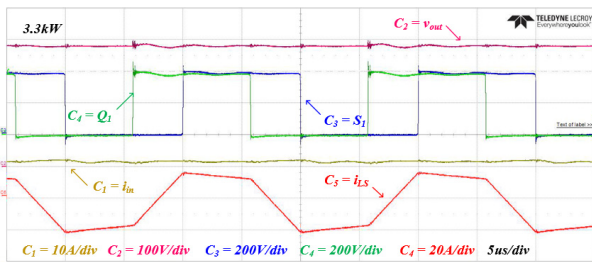
(a)



(b)



(c)



(d)

Fig. 17. Experimental waveforms of backward power flow according to power ratings: (a) 500 W; (b) 1 kW; (c) 2.5 kW; (d) 3.3 kW.

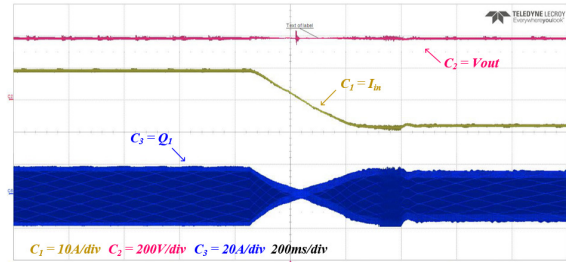


Fig. 18. Experimental waveform of bi-directional step load response from 3.3 kW to -3.3 kW

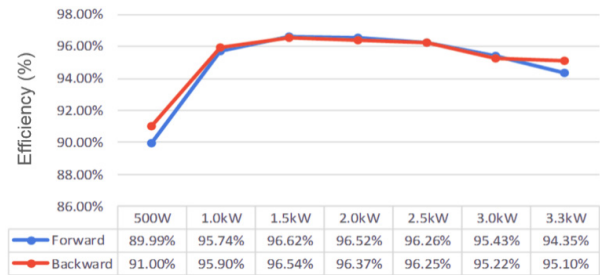


Fig. 19. Comparison of power conversion efficiency between forward and backward power flows

fixed to 380 V, and the target output voltage is regulated to 380 V. As shown in Fig. 16 and 17, phase gap between the primary and secondary legs signify the amount of transferred power. At the 3.3 kW condition in the forward power flow, the output voltage ripple is only about 2.5% of reference. Fig. 18 shows the bi-directional step load response from the forward direction of 3.3 kW to the backward direction of -3.3 kW. Although the dynamic step load variation is 6.6 kW with changing power flow directions, the output voltage is regulated well.

Fig. 19 indicates the efficiency curves of the prototype DAB converter according to the load variation from 500 W to 3.3 kW. At the 1.5 kW condition, the highest efficiency is measured as 96.62% and 96.54% with forward and backward power flow, respectively. In addition, at the full load conditions with forward and backward power flows, the power conversion efficiency is measured as 94.35% and 95.10%, respectively. At light load conditions, the efficiency is lower than the heavy load cases since the conduction loss due to the circulating current passing through the MOSFET, transformer and inductor is more significant. At the full load conditions, the power conversion efficiency also decreases since the conduction loss is increased by higher load current.

5. Conclusion

This paper presents an accurate DAB converter design methodology for SST applications. To ensure the maximum soft switching capability, and improve the overall efficiency, the proper design guidelines for the coupling inductance

and the dead time duration are presented by using detailed analysis of the DAB converter. In addition, by applying the effective soft start algorithm, the inrush current through the switches is drastically suppressed at the start-up state of the DAB converter. A 3.3 kW prototype DAB converter is designed and implemented to verify the bi-directional operation. The experimental results such as the fast bi-directional step load response with output voltage regulation and high power conversion efficiency demonstrate the practical feasibility of the proposed DAB converter design.

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