IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received October 25, 2021, accepted December 7, 2021, date of publication December 27, 2021, date of current version January 20, 2022.

Digital Object Identifier 10.1109/ACCESS.2021.3138988

A Hybrid Switching Modulation of Isolated Bidirectional DC-DC Converter for Energy Storage System in DC Microgrid

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This work was supported in part by the Energy Efficiency and Resources of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) Grant through the Korea Government Ministry of Knowledge Economy under Grant 20192010106750; and in part by the National Research Foundation (NRF), South Korea, under Project BK21 FOUR.

ABSTRACT Isolated bi-direction DC-DC converters are widely used for energy storage systems (ESS) of DC microgrids. Particularly, a current-fed isolated bi-directional DC-DC converter (CF-IBDC) receives much attention due to its merits such as the naturally attenuated current ripple on the battery side. However, high efficiency cannot be obtained at the light and heavy load conditions under the conventional control methods. In this paper, a hybrid switching modulation is proposed to improve the power conversion efficiency of the CF-IBDC under light and heavy load conditions. The duty cycle of the secondary sides and the phase shift angle are independently controlled according to the amount of the transferred power. The control strategy is based on the optimization of zero-voltage switching (ZVS) conditions and the minimization of the circulating current in the power converter. Using the proposed control algorithm, the ZVS capability can be obtained under the entire load condition, and the circulating current can be minimized under the single phase-shift modulation (SPSM). Experimental results with a 1-kW laboratory prototype CF-IBDC validate the effectiveness of the proposed modulation algorithm.

INDEX TERMS Current-fed topology, bidirectional dc-dc converter, pulse-width modulation, single phase shift modulation, hybrid control strategy, battery applications.

I. INTRODUCTION

Since renewable energy resources are required for DC microgrids, and developed energy from energy resources is commonly irregular due to various operating conditions such as weather and temperature. Therefore, an energy storage system (ESS) is essential to ensure the power quality and the reliability of the power supply. To interface the ESS with the DC microgrid, an isolated bi-directional DC-DC converter is used to charge and discharge batteries in the ESS system [1]–[3]. Since the ESS consists of many battery cells which have low voltage ratings and variable voltage ranges, an appropriate converter should handle the wide voltage range and high power conversion efficiency.

Under the single phase-shift modulation (SPSM) due to the inherent zero-voltage switching (ZVS) capability and the simple control algorithm with seamless bi-directional power flow capability, a voltage-fed dual-active-bridge (VF-DAB) converter is widely adopted to bi-directional applications [4]–[7]. However, this control strategy has drawbacks such as circulating current and backflow power in the VF-DAB converter under heavy load conditions [8], [9]. Without the DC blocking capacitor, the transient DC bias current of the transformer also makes the system unstable with additional loss, resulting in saturation [5], [8]. In addition, since the inductor current is highly sensitive to voltage gain and load conditions, the ZVS can be failed under light load conditions. In particular, the circulating current rapidly increases and the non-ZVS range is extended in the operating region far from the unity voltage gain.

To overcome the limitations of the SPSM, many control strategies such as pulse width modulation plus phase-shift [10]–[12], extended phase-shift [13], dual phase-shift [14], [15], triple phase-shift [16]–[18] modulations are

The associate editor coordinating the review of this manuscript and approving it for publication was S. K. Panda.

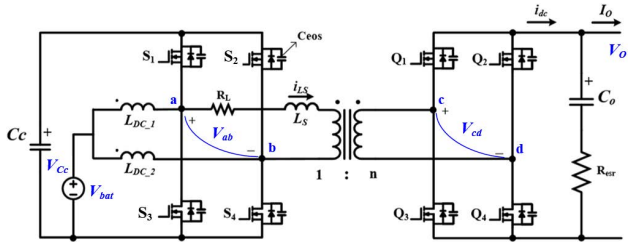

FIGURE 1. Current-fed isolated bidirectional DC-DC converter (CF-IBDC).

proposed. By introducing internal phase-shift (PS) between the two legs of full-bridges, three-level ac waveforms on the phase voltage can be generated, so that the length of a zero-vector can be adjusted. The key technique of those modulations is to extend the degree of freedom (DoF) of the control strategy which expands the soft-switching range and reduces the circulating current, thereby reducing the conduction loss. Although ZVS can be achieved over wide load ranges using various modulation schemes, it is difficult to obtain full ZVS capability over the entire load range because of the high complexity of its implementation [15]. Since there are lots of DoFs, including the internal phase shift of the primary bridge, the internal phase shift of the secondary bridge, and the external phase shift between two ac voltages, linear interpolation can be used to determine the selection of the variables based on the lookup table in the digital signal processor (DSP). However, it can degrade the system's dynamic response.

Furthermore, the characteristics of the VF-DAB converter are not suitable for charging and discharging batteries, which requires the power conversion capability for wide voltage ranges. This is because of a relatively high current ripple from the capacitive output filter of the VF-DAB converter, which adversely affects battery life. Therefore, the VF-DAB converter should not be used directly for the battery interface and a power filter should be connected between the battery and the converter.

As shown in Fig. 1, a current-fed isolated bi-directional DC-DC converter (CF-IBDC) consists of a synchronized buck/boost converter cascaded with the DAB converter including equivalent resistance [19]. The CF-IBDC is suitable for the interface between the battery and the high-voltage DC bus since it has the power conversion availability for the wide voltage range, small output voltage ripple, and high-power conversion efficiency. Compared with the VF-DAB converter, the CF-IBDC can expand the ZVS region under a wide voltage range since the synchronized buck/boost converter controls the output voltage based on PWM control, and it makes the effective gain of CF-IBDC unity. Also, the current-fed structure can make the current ripple in the battery side attenuated naturally, which can prolong the lifetime of energy storage.

To control the CF-IBDC over the wide-range voltage, a PWM plus phase shift (PPS) control has been proposed [20]. The output voltage is controlled by the clamping operation using the PWM technique on the low voltage side (LVS), while the duty ratio is fixed as 50% on the high voltage side (HVS). The bi-directional power flow is controlled by phase-shift modulation (PSM) between H-bridges. However, under the light load condition, the power conversion efficiency can be poor since high current spikes and high circulating current are induced. To overcome the PPS, a PWM plus dual phase-shift (PPDPS) was proposed to reduce the conduction loss [21]. However, ZVS cannot be obtained over the entire load range. The asymmetric PPDPS control is proposed in [22] to reduce the peak current and the circulating current, but only the zero current switching (ZCS) can be achieved instead of ZVS in HVS, which increases switching losses. In [23], a modified PWM plus phase-shift (MPPS) modulation is proposed to reduce conduction losses, but ZVS cannot be achieved under light load conditions. In [24], a fixed duty control between H-bridges is proposed to obtain ZVS capability of all the switches even under no-load conditions; however, in the heavy load condition, the circulating current increases due to the existence of zero-vectors in HVS by using the modulation method used in [24].

In this paper, a hybrid switching modulation of the CF-IBDC is proposed to improve power conversion efficiency and reduce the computational burden of the control algorithm. The model analysis based on mathematical approaches is presented. The circulating current and ZVS conditions are also analyzed. The structure of this paper is as follows: In Section 2, the operational principles of the proposed hybrid switching modulation are given. In Section 3, the circulating current based on peak current, RMS current, and ZVS conditions are presented. Also, the design considerations are analyzed. In Section 4, experimental results verify the validity and the performance enhancement of the proposed hybrid switching modulation and control algorithm using a 1-kW prototype CF-IBDC. Section 5 provides a conclusion

II. OPOERATION PRINCIPILES

The schematic of the CF-IBDC is illustrated in Fig. 1. In the LVS, there are two DC inductors of L_{DC1} and L_{DC2} which make up the interleaved and synchronized bi-directional buck/boost converter. It is assumed that $L_{DC1} = L_{DC2}$ is achieved in this paper. The inductance Ls represents the coupling inductance, which is coupled between the leakage inductance in the transformer and the external series inductance. The phase voltage of the LVS and the HVS is defined as vab and vcd, respectively. The clamping capacitor is defined as C_C. The phase-shift angle between v_{ab} and v_{cd} is normalized by π and defined as Φ_{PS} $(=\phi/\pi)$

A. OPERATION PRINCIPLES OF VOLTAGE MATCHING CONTROL

Fig. 2 shows the waveforms of the steady-state operations using the proposed modulation strategies for the CF-IBDC. The synchronized buck/boost converter can match the voltage gain of m $(=nV_{Cc}/V_O)$ as 1 when V_{bat} widely fluctuates during the charging and discharging process. On the LVS, S_1-S_4 control to help the clamping voltage of V_{Cc} to match the

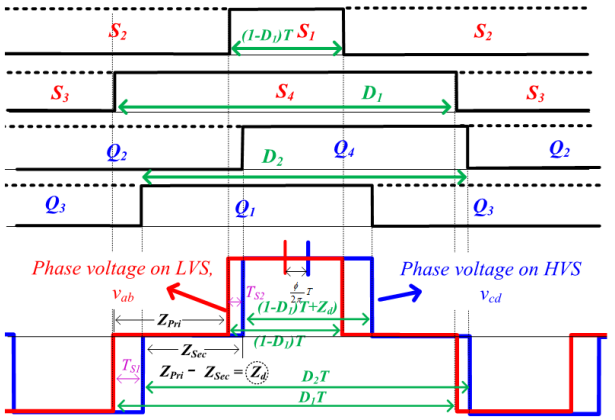

FIGURE 2. Proposed modulation strategy for the CF-IBDC.

output voltage. The battery voltage of V_{bat} is controlled to V_{Cc} ($= V_O/n$) by using the PWM control of bottom switches, D_1 where n is the turn ratio of the transformer. The relationship between V_{Cc} and V_{bat} is expressed as shown in (1).

$$V_{Cc} = \frac{v_{bat}}{1 - D_1} \tag{1}$$

Even if the unity voltage gain is not optimal in terms of the RMS phase current, the converter can achieve ZVS of all the switches at the light load when the voltage gain is unity [18]. Besides, if the gain is not unity voltage gain, the slew rate of the phase current will be steep, causing a high current spike and circulating loss. Therefore, to reduce both the switching loss and the conduction loss, the voltage gain of m is set as one in this paper and the slew rate of the phase current is zero during the positive or negative voltage overlapped period in v_{ab} and v_{cd}.

In Fig. 2, the phase voltage of the LVS and the HVS is indicated as red and blue lines of three-level waveforms, respectively. To control the length of zero-vector on each side, an asymmetrical PWM control is employed in the LVS, and an inner phase shift between legs of the H-bridge is adopted in the HVS. The duty ratio of the HVS is defined as D_2, which is like the duty ratio of the LVS. The zero-vectors duration of the phase voltage on the primary and secondary is defined as Z_{pri} and Z_{sec}, which are freewheeling time intervals expressed as follows:

$$Z_{pri} = D_1 T - \frac{T}{2}, \quad Z_{\text{sec}} = D_2 T - \frac{T}{2} \tag{2}$$

The difference between Z_{pri} and Z_{sec} is redefined as Z_d. The non-overlapped period between the LVS and the HVS is defined as T_{S1} and T_{S2}, respectively. The relation between T_{S1} and T_{S2} is expressed as follows:

$$\begin{cases} T_{S1} - T_{S2} = T(D_1 - D_2) = Z_d \\ \dfrac{T_{S1} + T_{S2}}{2} = \dfrac{\phi T}{2\pi} = \dfrac{\phi_{PS} T}{2} \end{cases} \tag{3}$$

As following [19]–[23], many patterns have already been proposed to control the CF-IBDC using the three-level waveforms of both bridges; however, those have the following disadvantages. In the case of $D_1 < D_2$, ZVS cannot be achieved even under medium load conditions due to not enough current for soft switching.

In addition, the transferred power is also limited even if the phase-shift angle increases. Besides, under the heavy load condition, even though ZVS can be achieved, the circulating current is high to make power conversion efficiency decrease. Therefore, the case of $D_1 < D_2$ is not considered in this analysis. The theoretical concept of the proposed control algorithm is shown in Fig. 3, in which ZVS can be achieved in all the switches with low conduction loss by a small circulating current. The mode can be divided into four modes according to the output power. Each mode is controlled by only one parameter which is duty ratio or phase shift.

B. ANALYSIS OF KEY OPERATION

The power delivered from the LVS to the HVS is defined as a forward bias, whereas the power transmission from the HVS to the LVS is defined as a reverse bias. Since the forward and reverse bias are symmetric, only the forward bias is chosen as an example for the analysis in this paper. In addition, since the operating waveforms are repeated every half cycle with opposite polarity, the analysis of the phase current is only obtained in a half switching period. Finally, the reverse bias can be analyzed in the same way.

1) LIGHT-LOAD (LL) - I OPERATION

Table 1 describes the characteristics of each control strategy given by existing CF-IBDC-related papers. In many CF-IBDC-related papers, even though there is each advantage, it has been difficult to satisfy ZVS conditions at no-load or very light load conditions. In [24], an effective modulation method was proposed to achieve ZVS even under no-load conditions. However, this method is not suitable for heavy load conditions due to the existence of the zero-voltage vector on the HVS regardless of load conditions, resulting in high circulating current and high reactive power in the converter. Therefore, the algorithm shown in [24] is employed in the proposed algorithm only for light load conditions

Fig.3-(a) shows the steady-state waveforms of the proposed algorithm under very light load conditions. In the light load I (*LL-I*) condition, to generate the bias current, the magnitude of Z_d is selected at a positive constant value as $T(D_1\text{-}D_2)$. It makes the active switches of the HVS enable ZVS operations. Based on Fig. 3-(a), specific times of t_0, t_1, t_2, t_3, and t_4 can be represented by D_1, D_2, and ϕ_{PS} as shown in (4).

$$\begin{cases} t_o = 0 \\ t_1 - t_0 = t_1 = \left(D_2 - \dfrac{1}{2}\right) T \\ t_2 - t_1 = \dfrac{T}{2}(D_1 - D_2 - \phi_{PS}) \\ t_3 - t_2 = (1 - D_1)T \\ t_4 = \frac{T}{2} \end{cases} \tag{4}$$

The phase current can be derived by (5) per period.

$$\Delta i_{Ls} = \frac{V_{Cc}}{L_S} \Delta t \tag{5}$$

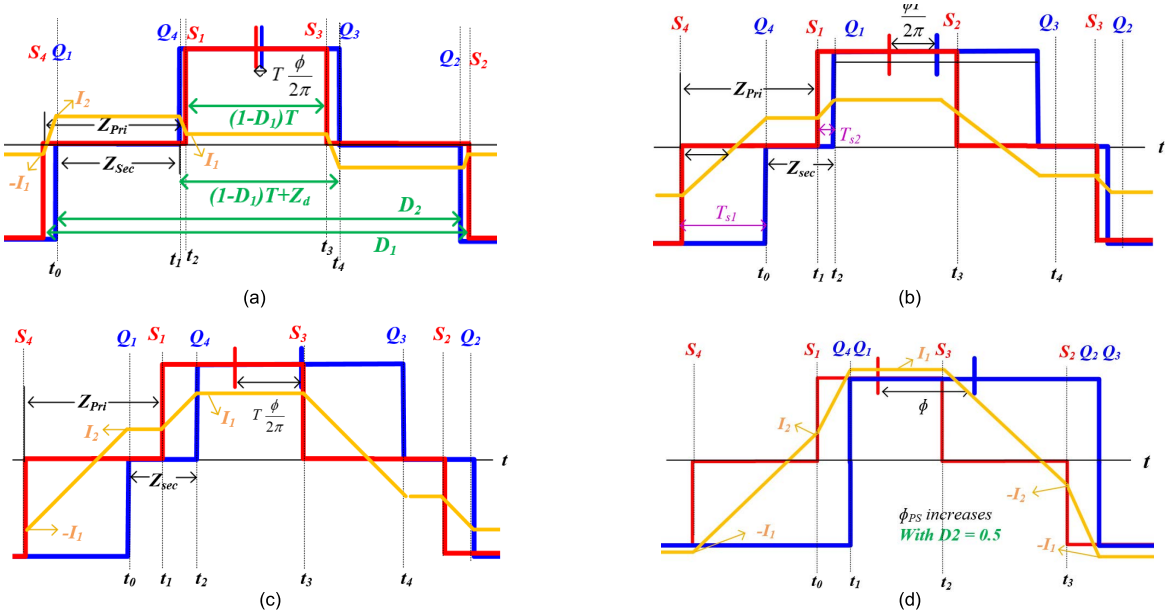

FIGURE 3. Theoretical voltage and current waveforms of four operating modes in the proposed converter according to the control strategies: (a) & (b) Light load mode I & II – PWM plus dual phase shift mode (PPDPS) with fixed '*Zd*' control, (c) Mid-load mode – PWM control, (d) Heavy load mode – PPS control.

TABLE 1. Comparison of control strategies of CF-IBDC converters.

	PPS [20]	PPDPS [21],[22]	MPPS [23]	PPDPS with fixed duty cycle [24]	Proposed control strategy
Control Variables	1	2	3	2	1
ZVS range	wide	wide – LVS No (only ZCS) -HVS	wide	Full range	Full range
Conduction loss	High @ light load condition	medium	low	High @ heavy load condition	low
Control complexity	low	medium	high	medium	low
Design complextiy	low	low	medium	medium	medium

The current of I_1 and I_2 in Fig. 3-(a) can be expressed as (6).

$$\begin{cases} I_1 = \dfrac{V_{Cc}}{2L_S f_S}\phi_{PS} \\ I_2 = \dfrac{V_{Cc}(D_1 - D_2)}{2L_S f_S} = \dfrac{V_{Cc}}{2L_S} Z_d, \quad (Z_d = T(D_1 - D_2) \end{cases} \tag{6}$$

The current of I_1 is only associated with variable ϕ_{PS}, and I_2 is only associated with variable Z_d.

The output power in LL-*I* mode is expressed as shown in (7).

$$P_O = \frac{2}{T}\left(\int_0^{t_4} v_{ab}(t) i_{Ls}(t) dt\right) = \frac{V_{Cc}^2}{L_S f_S}(1 - D_1)\phi_{PS} \tag{7}$$

The output power is only associated with D_1 and ϕ_{PS}. The peak phase current in the *LL-I* mode is represented as I_2 where it depends on D_1 and D_2. In the case of the duty ratio of D_2 is changed depending on D_1 to maintain the constant value of Z_d. Due to D_1 being controlled by the battery voltage, to reduce the RMS current and peak current, Z_d should be reduced. The design process of Z_d is introduced in Section 3 with the ZVS conditions of the HVS. The phase angle of this mode has the range as follows:

$$0 \le \phi_{PS} \le (D_1 - D_2) \tag{8}$$

2) LIGHT-LOAD (LL) - II OPERATION

When ϕ_{PS} reaches (D_1-D_2), the operating mode is changed to the light-load II (*LL-II*). As shown in Fig. 3-(b), this mode is the same as the PPDPS mode but the magnitude of D_2 depends on D_1 to maintain the fixed Z_d in the *LL-I* mode, which is the extended *LL-I* mode. According to Fig. 3-(b), t_0, t_1, t_2, t_3, and t_4 can be represented by D_1, D_2, and ϕ_{PS} as follows:

$$\begin{cases} t_o = 0 \\ t_1 - t_0 = t_1 = \dfrac{T}{2}(D_1 + D_2 - 1 - \phi_{PS}) \\ t_2 - t_1 = \dfrac{T}{2}\{-(D_1 - D_2) + \phi_{PS}\} \\ t_3 - t_2 = \dfrac{T}{2}(2 - D_1 - D_2 - \phi_{PS}) \\ t_4 = \dfrac{T}{2} \end{cases} \tag{9}$$

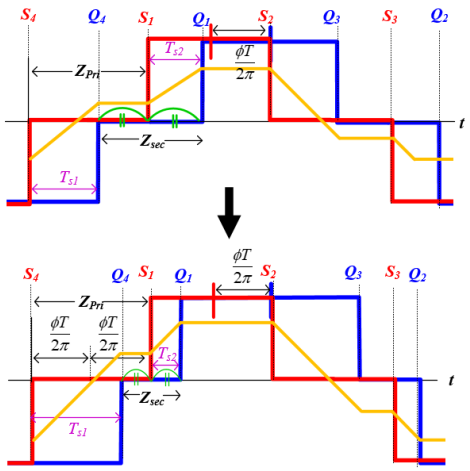

FIGURE 4. Proposed modulation strategies for the current-fed bi-directional DC-DC converter under mid-load condition.

The transmitted power in the *LL-II* mode is expressed as (10)

$$P = \frac{V_{Cc}^2}{4L_S f_S}\left[-\phi_{PS}^2 + 2(2 - D_1 - D_2)\phi_{PS} - (D_1 - D_2)^2\right]$$
$$= \frac{V_{Cc}^2}{4L_S f_S}\left[-\phi_{PS}^2 + 2(2-2D_1 + \frac{Z_d}{T})\phi_{PS} - (\frac{Z_d}{T})^2\right] \quad (10)$$

The transmitted power is related to D_1 and ϕ_{PS} in the *LL-II* mode as same as the *LL-I* mode. I_1 and I_2 in Fig. 3-(b) can be expressed as (6). Even if I_1 and I_2 in the *LL-II* mode are the same as the *LL-I* mode, the peak current is changed from I_2 to I_1 as ϕ_{PS} increases. The amplitude of I_2 does not change since I_2 depends on Z_d, which is held in overall *LL* mode. When ϕ_{PS} arrives at half of Z_{pri}, half of Z_{sec} is the same as T_{S2}.

In this mode, the phase angle is in the range expressed by (11).

$$(D_1 - D_2) \le \phi_{PS} \le D_1 - \frac{1}{2} \quad (11)$$

Therefore, D_1 and D_2 should be longer than $0.5 + (D_1 - D_2)$ and 0.5 to obtain the *LL-II* mode, respectively. Here, the range of D_1 is limited to as narrow as possible since the range of D_1 is proportional to the circulating current range. The circulating current can be minimized when D_1 is 0.5; however, to obtain the ZVS capability, the minimum value of D_1 should be greater than 0.5.

3) MEDIUM-LOAD (ML) OPERATION

When ϕ_{PS} is arrived at $(D_1 - 1/2)$, the entire *LL* mode is finished, and the operating mode is changed to the medium-load (*ML*) mode. Fig. 3-(c) shows the control concept of the *ML* mode. As the middle between the *LL mode* and the heavy-load (*HL)* mode, the *ML* mode connects the two modes smoothly. In the *ML* mode, D_2 is controlled to regulate the output voltage based on the PMW control of D_2 by using an inner PS modulation of the HVS. Fig. 4 shows the theoretical concept of the *ML* mode as output power increases. Since the waveforms of the phase voltage and the phase current in the *ML* mode are the same as the *LL-II* mode, the time interval is equivalent, which is represented in (6). The current of I_1 and I_2 in Fig. 3-(c) can be expressed as (12).

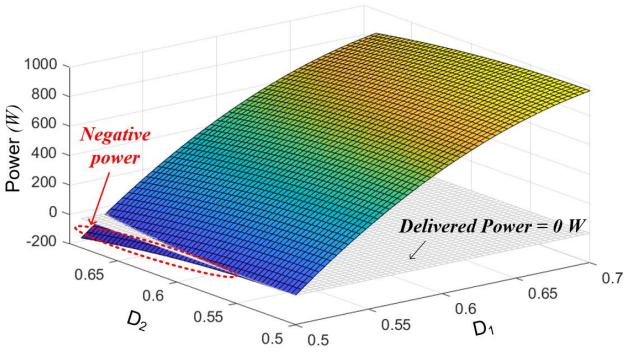

FIGURE 5. Output power versus D_1 and D_2 under medium-load condition.

$$\begin{cases} I_1 = \dfrac{V_{Cc}}{2L_S f_S}\phi_{PS} = \dfrac{V_{Cc}(2D_1 - 1)}{4L_S f_S} \\ I_2 = \dfrac{V_{Cc}(D_1 - D_2)}{2L_S f_S} \end{cases} \quad (12)$$

In the *ML* mode, since ϕ_{PS} is fixed, the amplitude of I_1 does not change unless the battery voltage alters. Being different from the entire *LL* mode, I_2 is changed during the *ML* mode. When D_2 decreases until 0.5, I_2 increases. The transmitted power in the *ML* mode is expressed as shown in (13).

$$P = \frac{V_{Cc}^2}{4L_S f_S}\left(-D_2^2 + D_2 - 4D_1^2 + 6D_1 - \frac{9}{4}\right) \quad (13)$$

From (13), since ϕ_{PS} is held as $(D_1 - 1/2)$ in the *ML* mode, the output power is only associated with D_1 and D_2. Before the *ML* mode, D_2 changes according to D_1 to maintain a constant Z_d, while D_2 in the *ML* mode actively changes to regulate the output voltage.

As shown in Fig. 5, when D_2 decreases, the transferred power increases, and the maximum power can be obtained when D_2 is 0.5 in the *ML* mode regardless of D_1. It should be noted that the several combinations of D_1 and D_2 are possible to transmit power to the backward bias. In Fig. 5, a gray plane shows delivered power zero. This is because D_2 in the *ML* mode can decrease to 0.5 regardless of D_1, which does not satisfy (11). Therefore, the proper range of D_1 is also required with the consideration of D_2. The intuitive criterion of mode change from the *ML* mode to the *HL* mode is the length of D_2. When D_2 reaches 0.5, the mode changes.

4) HEAVY-LOAD (HL) OPERATION

As shown in Fig. 3-(d), in the *HL* mode, the secondary phase voltage is a square waveform, and the transmitted power is controlled by only ϕ_{PS} control. This control strategy is the same as conventional PPS control. The time interval t_0, t_1, t_2,

and t_3 can be represented only by D_1 and ϕ_{PS} as follows:

$$\begin{cases} t_o = 0 \\ t_1 - t_0 = t_1 = \dfrac{T}{2}\left(\dfrac{1}{2} - D_1 + \phi_{PS}\right) \\ t_2 - t_1 = \dfrac{T}{2}\left\{\dfrac{3}{2} - (D_1 + \phi_{PS})\right\} \\ t_3 = \dfrac{T}{2} \end{cases} \tag{14}$$

In addition, I_1 and I_2 in Fig. 3-(d) can be expressed as (15).

$$\begin{cases} I_1 = \dfrac{V_{Cc}}{2L_S f_S}\phi_{PS} \\ I_2 = \dfrac{V_{Cc}}{2L_S f_S}(2D_1 - 1 - \phi_{PS}) \end{cases} \tag{15}$$

Since, in the *ML* mode, ϕ_{PS} is fixed to $(D_1 - 1/2)$, the output power consisting of D_1 and D_2 can be reorganized in terms of ϕ_{PS}, which is expressed as follows:

$$P = \frac{V_{Cc}^2}{4L_S f_S}\left(-4D_1^2 + 6D_1 - 2\right) = \frac{V_{Cc}^2}{4L_S f_S}\left(-4\phi_{PS}^2 + 2\phi_{PS}\right) \tag{16}$$

From (16), the maximum power can be obtained when ϕ_{PS} is 0.25. In the *HL* mode, the range of the phase angle is expressed by (17).

$$D_1 - \frac{1}{2} \le \phi_{PS} \le \frac{1}{4} \tag{17}$$

To satisfy (17), D1 is limited to 0.75. Finally, to protect the reverse power transmission, the proper range of D1 is limited as

$$\frac{1}{2} + \frac{Z_d}{2\pi} \le D_1 \le \frac{1}{4}. \tag{18}$$

C. CONTROL STRATEGY OF THE PROPOSED OPERATING MODE

Fig. 6 shows the phase voltage and the phase current waveforms under the various control modulations according to the load conditions. In Fig. 6-(a) and Fig. 6-(b), a high peak current occurs under the light load condition, resulting in high conduction loss and core loss. When the PPDPS with the fixed Z_d in Fig. 6-(c) is alternatively employed in this paper under the light load condition, power loss can be reduced since the duration of high peak current ends only when ϕ_{PS} reaches $Z_d/2$.

Meanwhile, the shaded area in Fig. 6 shows the circulating current of the phase current due to the zero-vector of the HVS. For the proposed control strategy in the *HL* mode, the PPS method is shown in Fig 6-(d) is adopted to reduce the circulating current. Since the PPS method can eliminate the zero-vector on the HVS under the heavy load condition, it can minimize circulating current and reactive power compared with Fig. 6-(e) and Fig. 6-(f). As shown in Fig. 6-(e), when the PPDPS is employed, the non-power transmission region is extended as power increases. The PPDPS with the fixed Z_d under the heavy load condition shown in Fig. 6-(f) also has the same problem since the zero-vector on the HVS is

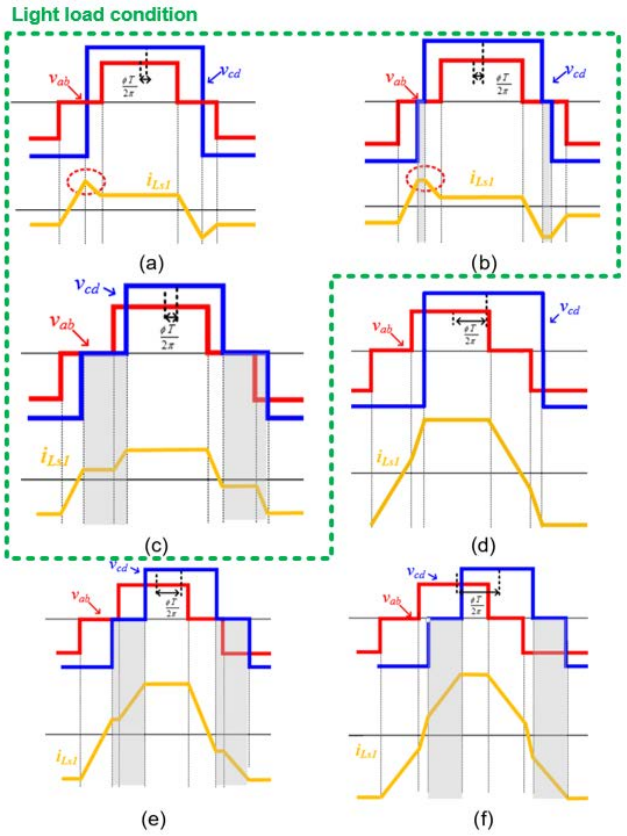

FIGURE 6. Phase voltage and current waveforms under operating modes: (a) PPS at light load, (b) PPDPS at light load, (c) PPDPS with fixed ΔT in [24] at light load (d) PPS at heavy load, (e) PPDPS at heavy load, and (f) PPDPS with fixed ΔT at heavy load [24].

maintained continuously. This is the reason why the fixed Z_d with the PPDPS is limited to be used only in the light load condition. The *ML* mode is an intermediate process from the *LL* mode to the *HL* mode. Since in the *ML* mode, the PWM of D_2 is only used to control the output power, the PPDPS with the fixed Z_d at the light load condition can be smoothly changed to the PPS control as power increases with the simple control strategy.

Fig. 7 shows the control diagram of the CF-IBDC based on the proposed algorithm. Two control loop controllers are required to implement: the clamping voltage control loop (G_{vc}(s)) and an output voltage control loop (G_{vo}(s) & G_i(s)). The clamping voltage control loop is required for voltage matching control with the reference of V_O/n based on the modulation of D_1. The output voltage control loop consists of a dual closed-loop system. The inner-control loop is essential to control the battery current. The outer-control loop is used to control power flows, which is based on the adjustment of ϕ_{PS} and D_2. The output of the outer-control loop of G_{vo}(s) is the reference of the inner-control loop. The control variables of ϕ_{PS} and D_2 are independently controlled by considerations of the ZVS operation and the minimization of the circulating current and the simple control strategy.

Fig. 8 shows the trajectory for the output power when the value of D_1 is different from the proposed control

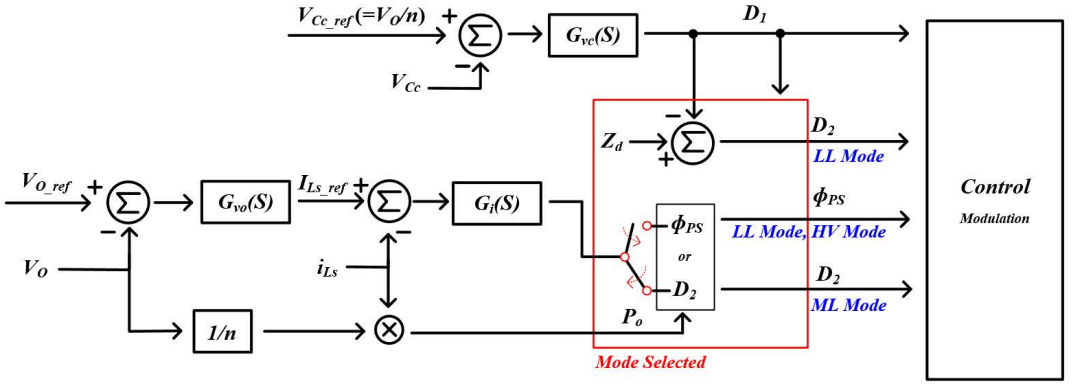

FIGURE 7. Decoupling control diagram for the proposed current-fed bi-directional DC-DC converter.

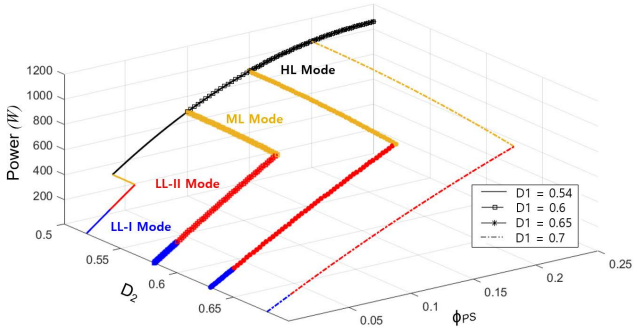

FIGURE 8. Trajectories for output power versus D_2 and ϕ_{PS} according to the proposed modulation strategy.

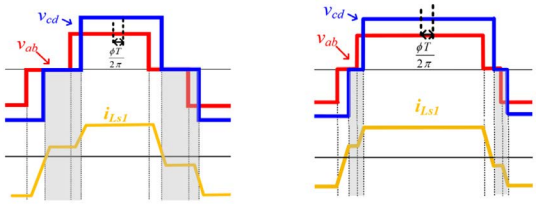

FIGURE 9. Time interval of circulating current according to D_1 and D_2 at LL mode: (a) Case of large D_1 and D_2, (b) Case of small D_1 and D_2.

modulation where $V_O = 380$V, $V_{Cc} = 127$ V, $L_S = 20\ \mu$H, $V_{bat} = 48$ - 60 V, and $f_S = 50$ kHz. As shown in Fig. 8, the control variables of D_2 and ϕ_{PS} can be separated and be individually controlled, making transmitted power increases smoothly and seamlessly. The maximum power can be obtained when ϕ_{PS} is 0.25, and D_2 is 0.5. As D_1 is smaller, the region of the *LL-II* and the *ML* mode is reduced, and the range of the *HL* mode is extended. As the increase in the time interval of *LL-II* and the *ML* mode under the same power conditions, the circulating time is extended, resulting in reactive power and conduction losses increased. In order words, to obtain high efficiency, the duration of the *LL-II* and the *ML* mode should be minimized. Therefore, although the maximum value of D_1 is calculated as 0.75 from (18), the CF-IBDC converter operates under the D_1 range as narrow as possible.

III. EFFECTIVE HARDWARE DESIGN STRATEGY

When handling the application of the wide voltage range applications such as ESS, there is commonly a trade-off between the conduction loss and the switching loss. Therefore, careful design considerations are required to obtain the high performance of the CF-IBDC.

A. ANALYSIS OF CURRENT STRESS

1) PEAK OF PHASE CURRENT

The peak current has a significant effect on the RMS current and it also relates to the core loss of the transformer and extra series coupling inductance. To improve the efficiency, the conduction loss, and the core loss in the CF-IBDC should be minimized. Based on the analysis of peak phase current, the tendency of the conduction loss and the core loss can be estimated. The peak phase current shown in Fig. 3 can be derived as follows:

$$\begin{cases} \dfrac{V_{Cc}}{2L_S} Z_d, & 0 \le \phi_{PS} \le (D_1\ D_2)\ \&\ D_2 = (D_1 - Z_d) \\ \dfrac{V_{Cc}}{2L_S f_S} \phi_{PS}, & (D_1\ D_2) \le \phi_{PS} \le (D_1 - \dfrac{1}{2}) \\ & \quad \&\ D_2 = (D_1 - Z_d) \\ \dfrac{V_{Cc}(2D_1 - 1)}{4L_S f_S}, & \phi_{PS} = (D_1\ \dfrac{1}{2})\ \&\ (D_1 - Z_d) \le D_2 \le \dfrac{1}{2} \\ \dfrac{V_{Cc}}{2L_S f_S} \phi_{PS}, & (D_1 - \dfrac{1}{2}) \le \phi_{PS} \le \dfrac{1}{4}\ \&\ D_2 = \dfrac{1}{2} \end{cases} \tag{19}$$

From (19), the peak current is expressed as the function of Z_d, D_1, and ϕ_{PS}. Since the proposed algorithm is employed to the PPDPS with a fixed Z_d at light load conditions and the PPS algorithm at heavy load conditions, the peak current at the light load and the heavy load is equal to each control method. Therefore, the proposed algorithm has a low peak current over the entire load range compared with the conventional control strategies.

2) DISCUSSION OF PHASE CURRENT IN CIRCULATING TIME INTERVAL

As shown in Fig. 9, each waveform represents non-active power transfer stages shown in the shadowed area, which depends on the load conditions and the modulation methods.

Since the proposed algorithm consis0ts of the PPDPS with the fixed Z_d control in the *LL* mode, PWM of D_2 control in the *ML* mode, and PPS control in the *HL* mode, respectively, the circulating current is required to be analyzed for each mode. For the simplification of the analysis, when the dead time of the gate signal and the resonance between the output capacitance of the power switches and the coupling inductance is negligible, the circulating current in the *LL-I* mode can be expressed as (20).

$$i_{cLL-II\&ML}\begin{cases}0, & 0<t<\dfrac{\phi_{PS}T}{2}+\dfrac{Z_d}{2}\\ \dfrac{V_{Cc}Z_d}{2L_S}, & \dfrac{\phi_{PS}T}{2}+\dfrac{Z_d}{2}<t<Z_{pri}\\ \dfrac{V_{Cc}}{L_S}\left(\dfrac{Z_d}{2}+t-Z_{pri}\right), & \\ & Z_{pri}<t<Z_{pri}+\dfrac{\phi_{PS}T}{2}-\dfrac{Z_d}{2}\\ 0, & Z_{pri}+\dfrac{\phi_{PS}T}{2}-\dfrac{Z_d}{2}<t<\pi\end{cases} \tag{20}$$

The RMS value of the circulating current in the *LL-I* mode can be derived as follows:

$$\begin{aligned}I_{cir,RMS,LL-I} &= \sqrt{\frac{1}{T}\int_0^T i_{cLL-I}^2(t)dt}\\ &= \frac{V_{Cc}Z_d}{2L_S}\sqrt{3D_2-D_1-\phi_{PS}-1}\end{aligned} \tag{21}$$

where $I_{cir,RMS,LL-I}$ is the RMS value of the circulating current during the *LL-I* mode, i_{cLL-I} is the circulating current expressed in (18). In the same way, the circulating current in the *LL-II* mode and the *ML* mode can be derived as shown in (22).

$$i_{cLL-II\&ML}\begin{cases}0, & 0<t<\dfrac{\phi_{PS}T}{2}+\dfrac{Z_d}{2}\\ \dfrac{V_{Cc}Z_d}{2L_S}, & \dfrac{\phi_{PS}T}{2}+\dfrac{Z_d}{2}<t<Z_{pri}\\ \dfrac{V_{Cc}}{L_S}\left(\dfrac{Z_d}{2}+t-Z_{pri}\right), & \\ & Z_{pri}<t<Z_{pri}+\dfrac{\phi_{PS}T}{2}-\dfrac{Z_d}{2}\\ 0, & Z_{pri}+\dfrac{\phi_{PS}T}{2}-\dfrac{Z_d}{2}<t<\pi\end{cases} \tag{22}$$

The RMS value of the circulating current at the LL-*II* mode can be obtained as shown in (23).

$$\frac{V_{Cc}}{2L_S}\sqrt{\frac{4Z_d^3-15Z_d^2\phi_{PS}T+6Z_d\left\{(\phi_{PS}T)^2+Z_dZ_{pri}\right\}-(\phi_{PS}T)^3}{6\pi}} \tag{23}$$

Since the shape of the phase current is the same as the case of the *LL-II* mode, the circulating current and the RMS current can be obtained by replacing Z_d with $(D_1\text{-}D_2)T$ in (22) and (23). Since the zero-vector in HVS is zero in the *HL* mode, the circulation time interval does not exist.

As shown in Fig. 6, even if the peak current shown in Fig. 6-(c) is lower than that shown in Fig. 6-(a) and Fig. 6-(b), the circulating time interval in Fig. 6-(c) is larger than that in Fig. 6-(a) and Fig. 6-(b). Therefore, the proper range of D_2 should be decided. Fig. 9 shows the circulating region according to D_2. As D_2 is set far from 0.5, the circulating time interval increases. Since the value of D_2 at the *LL* mode is determined by D_1, the maximum value of D_1 should be as small as possible with a suitable voltage matching control strategy.

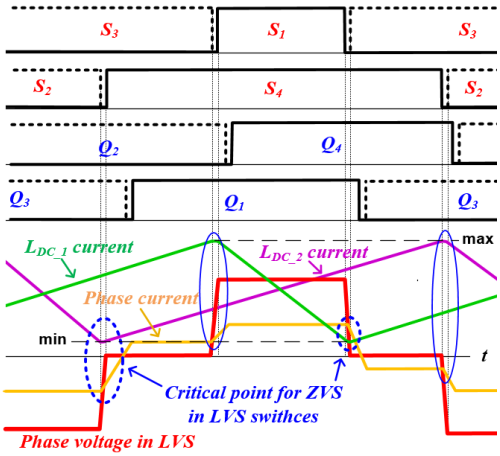

FIGURE 10. Theoretical switching waveforms including DC filter current at LVS.

B. ANALYSIS OF SOFT-SWITCHING CONDITIONS

1) LOW VOLTAGE SIDE (LVS)

Since the CF-IBDC should handle the wide range voltage, the current-fed structure of the battery connected side and the DC bus interface is used as shown in Fig. 1. Therefore, the ZVS condition is different from each side. Fig. 10 shows theoretical switching waveforms in the LVS containing the DC filter current and the dead time duration. In Fig. 10, the maximum and minimum values of the DC filter inductor current are indicated by the phase current. The ZVS criteria of the power switches are indicated as blue circles. Since the switch current in the LVS is related to the filter current, the output capacitance of the switches in the LVS, $C_{oes,LVS}$, is charged and discharged by the current difference between i_{LDC} and i_{LS} during the dead time. The ZVS conditions can be derived by the relationship between the phase current and the filter current as follows:

$$\begin{cases}S_1: i_{LDC1,\max}-i_{LS}(t)>2C_{oes,LVS}\dfrac{V_{Cc}}{\Delta t(=t_d)}=I_{\min,req,L}\\ S_2: i_{LDC2,\max}-i_{LS}(t)>I_{\min,req,L}\\ S_3: i_{LS}(t)-i_{LDC1,\min}>I_{\min,req,L}\\ S_4: -i_{LS}(t)-i_{LDC2,\min}>I_{\min,req,+L}\end{cases} \tag{24}$$

where t_d is the dead time duration, $I_{LDC,max}$ and $I_{LDC,min}$ are the maximum and minimum value of the DC filter current, respectively, and $I_{min,req,L}$ is the desired minimum current for fully charging or discharging $C_{oes,LVS}$. The maximum and

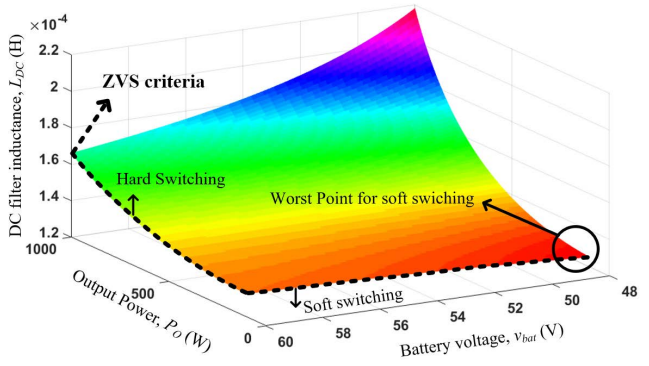

FIGURE 11. Design area of DC filter inductance with considerations of output power and battery voltage.

minimum values of the DC filter current can be expressed as follows:

$$\begin{cases} I_{LD1,\max} = I_{LDC2,\min} = I_{LDC} + \dfrac{V_{Cc}}{2L_{DC}f_S} D_1(1-D_1) \\ I_{LD1,\min} = I_{LDC2,\max} = I_{LDC} - \dfrac{V_{Cc}}{2L_{DC}f_S} D_1(1-D_1) \end{cases} \tag{25}$$

where I_{LDC} is the average current passing through the DC filter, which can be derived by the average input current of the boost converter, I_{out}/(1-D), where D is the duty ratio of power switches. According to Fig. 10 and (24), the upper switches in the LVS, S_1 and S_2, are easier to obtain the ZVS capability than the lower switches in the LVS, S_3 and S_4, which is indicated in the dotted circles in Fig. 10. The ZVS conditions for the LVS switches can be obtained by designing the DC filters in the LVS. The design guide of the DC filter for the ZVS capability can be expressed as (26).

$$\begin{cases} L_{DC} < \dfrac{V_{bat}(V_{Cc} - V_{bat})}{2V_{Cc}f_S \left\{ I_{\min\_req} - \Delta i_{LS} + \frac{P_O}{V_{bat}} \right\}} \\ \Delta i_{LS} = I_{peak,LS} - \dfrac{V_{Cc}}{2L_S} t_d \end{cases} \tag{26}$$

Fig. 11 shows the criteria of the DC filter inductance for the ZVS capability according to V_{bat} and output power. In Fig. 11, when the inductance is less than the boundary area, the ZVS capability in the LVS is obtained. It is most difficult to obtain the ZVS capability when V_{bat} = 48 V at the no-load condition. If L_{DC1} and L_{DC2} are small enough, the ZVS capability of the LVS switches can easily be obtained; however, the peak current and the RMS current of the DC filter increase, which causes high conduction loss. Therefore, the DC filter inductance should be designed as large as possible to obtain ZVS in the LVS.

2) HIGH VOLTAGE SIDE (HVS)

Being different from the ZVS condition of the LVS switches, that of the HVS switches only depends on the phase current. The basic ZVS condition of the HVS switches can be derived

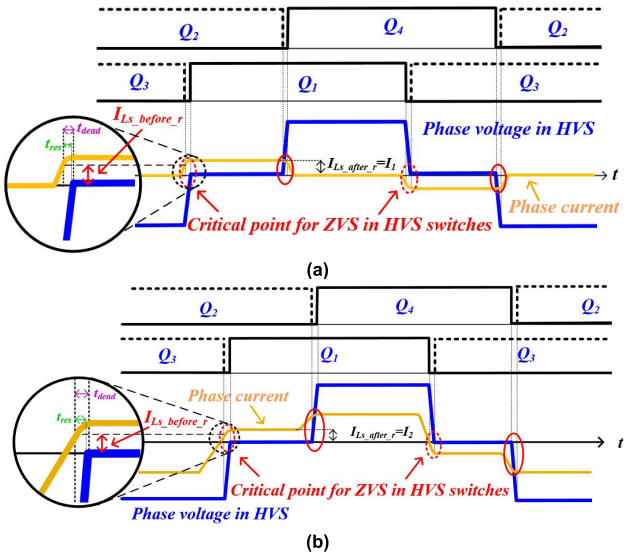

FIGURE 12. Theoretical switching waveforms in HVS: (a) LL-I mode under no-load condition, (b) LL-II mode.

as follows:

$$\begin{cases} Q_1\&Q_4 : \dfrac{i_{LS}(t)}{n} > 2C_{oes,HVS}\dfrac{V_O}{t_{dead}} = I_{\min,req,H} \\ Q_2\&Q_3 : -\dfrac{i_{LS}(t)}{n} > I_{\min,req,H} \end{cases} \tag{27}$$

where $C_{oes,HVS}$ is the output capacitance of the switches in the HVS and $I_{min,req,H}$ is the desired minimum current for fully charging and discharging of $C_{oes,HVS}$. Since, as shown in (27), the ZVS capability can be obtained by the phase current, the amplitude of the phase current at the switching moment is significant, which means that the ZVS can easily be achieved under not the light load condition but the heavy load condition in the CF-IBDC. This is the same as the performance issue in most of the DAB converters.

To overcome this limitation, the proposed control algorithm using the fixed Z_d with the PPDPS is employed under the light load condition as shown in Fig. 3-(a). Fig. 12 shows the ZVS process in the HVS under the proposed control algorithm. Just as shown in Fig. 10, the ZVS criteria for each switch in the HVS are described as red circles. Difficult points for the ZVS condition are indicated as dotted circles. Details of the resonant time interval are also shown in Fig. 12 where t_{res} is the resonant time duration between $C_{oes,HVS}$ and L_S. In Fig. 12-(a) and Fig. 12-(b), the DC currents of $I_{Ls,before,r}$ and $I_{Ls,after,r}$ are generated by the fixed Z_d with the PPDPS in the *LL-I* mode and the *LL-II* mode, respectively. The current of $I_{Ls,before,r}$ indicates that the constant value before the resonance during the dead time, and it makes charging and discharging of the output capacitance of the HVS switches.

The most important consideration of selecting Z_d is the minimum current, $I_{Ls,before,r}$, for charging/discharging the output capacitance of the power switches. As Z_d increases, the amplitude of the minimum current increases, which can reduce ZVS failure. However, it also increases the conduction

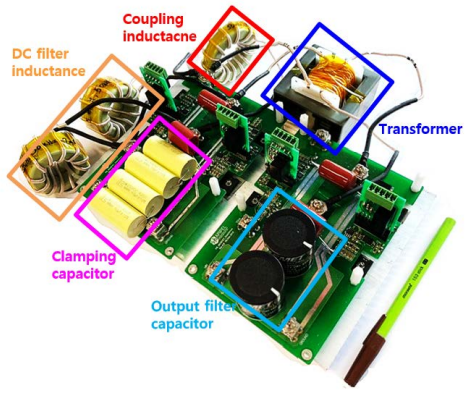

FIGURE 13. Photograph of the proposed CF-IBDC converter prototype.

loss because of RMS current increment. This is the reason why the optimal value of Z_d is required. In [24], the ZVS condition for the HVS switches with the fixed Z_d is explained in detail by considering the resonant process and the parameter design of ΔT. From [24], the length of Z_d can be derived. The ZVS condition is that $I_{Ls,before,r}$ should be larger than zero at the fixed Z_d as follows:

$$\begin{cases} Z_d \geq t_{res} + \dfrac{\left(I_{Ls,before,r} + I_{Ls,after,r}\right) L_S}{V_{Cc}} \\ t_{res} = \dfrac{\arctan\left(\frac{V_O}{Z_r I_{Ls,before,r}}\right)}{\frac{1}{2n\pi}\sqrt{\frac{1}{2C_{oes,HVS}L_S}}}, \quad Z_r = \sqrt{\dfrac{L_S}{2C_{oes,HVS}}} \\ I_{Ls,after,r} = \sqrt{I_{Ls,before,r}^2 + \left(\dfrac{V_O}{Z_r}\right)^2} \end{cases} \tag{28}$$

Even though the large Z_d can easily make the output capacitance of HVS switches charge and discharge, it makes long circulation time interval as analyzed above, which causes higher conduction loss, i.e., the trade-off between the switching loss and the circulation status. Meanwhile, as shown in Fig. 13, t_{res} should be shorter than t_d for obtaining full ZVS condition. Therefore, the dead time is desired to get the ZVS condition as shown in (29).

$$t_{res} \leq t_d < t_{d,\max} = \frac{\pi\sqrt{2L_S C_{oes,HVS}}}{2} \tag{29}$$

Note that the dead time duration should be shorter than $t_{d,max}$ to prevent capacitor voltage dumping where the resonant current flowing in the reverse direction again to charge the output capacitance.

IV. EXPERIMENTAL RESULTS

Table 2 shows the parameter specifications of the CF-IBDC, which are used in analysis and experiment. A prototype of the CF-IBDC converter is shown in Fig. 13. It is composed of two DC inductors and an H-bridge which make the interleaved boost converter in the LVS. In the LVS, SUG80050E manufactured by VISHAY is selected as the power switch since it has a low $R_{ds,on}$ of 5.4 mΩ with 150 V rated voltage, resulting

TABLE 2. Design specifications of CF-DAB converter.

.	Quantity	Value
P_O	Output Power	1-kW
V_{bat}	Battery voltage (LiFePO4)	48 V-60 V
V_{Cc}	Clamping voltage	127 V
V_{out}	Output voltage	380 V
D_1	Range of lower switches on LVS	0.527-0.622
n	Turn ratio	1:3
fs	Switching frequency	50 kHz
Ls	Coupling inductance	30 µH
$C_{oes,LVS}$	Output capacitance of switches in LVS	540 pF
$C_{oes,HVS}$	Output capacitance of switches in HVS	55 pF
Z_d	Difference zero-vector in LVS and HVS.	130 nsec
L_{DC}	DC filter Inductance	120 µH
C_O	HVS filter capacitor	680 µF
S_1-S_4	Switches in LVS	SUG80050E
Q_1-Q_4	Switches in HVS	SCT3060KL

in decreasing conduction loss. In the HVS, a SiC MOSFET of SCT3060KL manufactured by ROHM is selected to reduce the junction capacitance which is 55 pF with 60 mΩ of $R_{ds,on}$. In addition, to reduce internal leakage inductance, a toroidal DC inductor core is employed due to its singularity: the closed concentric geometry [25]. According to the considerations of the ZVS condition and the conduction loss in section 3.2, each L_{DC} is selected to 120 μH. From (26) and Fig. 12, Z_d is selected to 130 ns, and the dead time duration of t_d is selected around 0.3 μs. As the controller of TM320F28335 manufactured by TI is employed to control the proposed power converter.

A. STEADY-STATE OPERATING WAVEFORMS

Fig. 14 and Fig. 15 show the steady-state waveforms as the output current increases when v_{bat} is fixed at 48 V and 60 V using the proposed hybrid control algorithm under the forward bias, respectively. Fig. 14-(a) and Fig. 15-(a) show the waveforms of the *LL-I* mode under the no-load condition. The phase voltage of each side under 60 V condition is magnified in Fig. 15-(a). Even though T_{S1} and T_{S2} are narrow, a DC bias current is generated by Z_d according to (3). It helps to achieve the soft switching of the HVS switches under the no-load conditions as shown in Fig. 12. The *LL-II* mode is shown in Fig. 14-(b) and Fig. 15-(b). In the *LL* mode, Z_d is maintained and ϕ_{PS} is controlled as power changes. When Φ_{PS} reaches half of Z_{pri}, the *ML* mode in Fig. 14 - (c) and Fig.15-(c) starts. In Fig. 14, the *ML* mode starts at 550 W and ends at 800 W, while the *ML* mode in Fig. 15 starts at 300 W and ends at 400 W. As the output power increases, D_2 is going to 0.5 in the *ML* mode, which makes the duty of the secondary side be 0.5. After that, it moves to the *HL* mode, which is the same as the conventional PPS control. In the *HL* mode shown in Fig. 14-(d) and Fig. 15-(d), only ϕ_{PS} is controlled to regulate the output power.

The entire mode transition is smooth and seamless. The difference between Fig. 14 and Fig. 15 is only the time interval of the *ML* mode. In Fig. 14, it has a large portion of

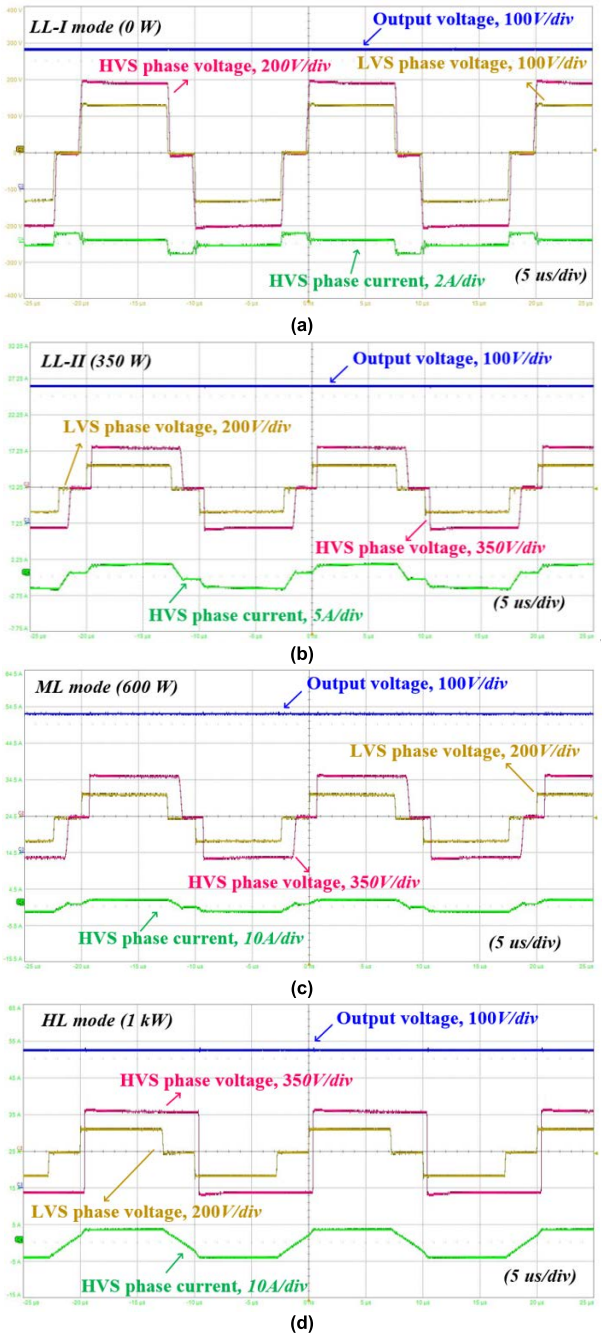

FIGURE 14. Steady-state operating waveforms using the proposed control algorithm under $V_{bat} = 48$ V: (a) *LL-I* mode, (b) LL-II mode (c) ML mode (d) HL mode.

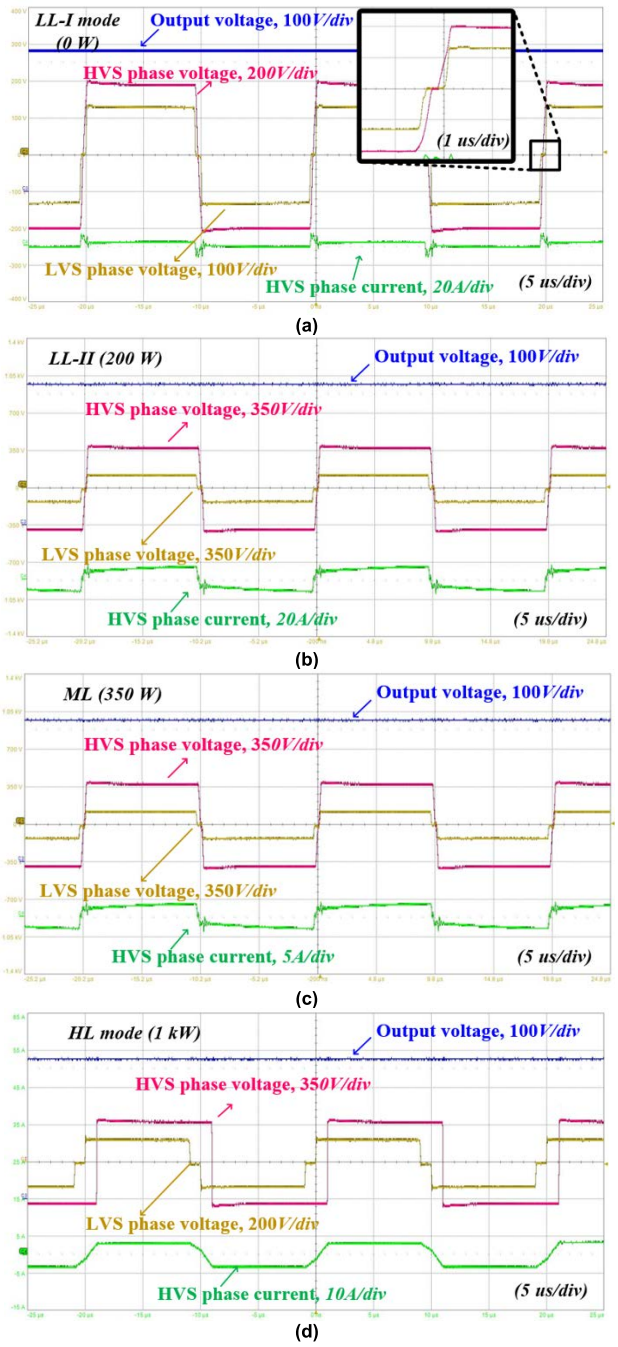

FIGURE 15. Steady-state operating waveforms using the proposed control algorithm under $V_{bat} = 60$ V: (a) *LL-I* mode, (b) *LL-II* mode (c) *ML* mode (d) *HL* mode.

power transmission, while the ML mode shown in Fig. 15 is narrow. As D_1 is longer, the interval of ML mode becomes wider, resulting in relatively easy ZVS conditions. Since D_2 goes to 0.5 as the output power increases in the ML mode, the reactive power and the circulating current is reduced in the *HL* mode as shown in Fig. 6 and Fig. 9, respectively, resulting in the trapezoidal current waveform.

Fig. 16 illustrates the experimental measurements of a step load response from 200 W to 1-kW with $V_{bat} = 48$ V under the forward bias. Zoomed waveforms are shown on the right side, which operates under the *LL* mode (above) and the *HL* mode. The phase current passing through the LVS increases from 4.7 A to 23.2 A during the step load experiment. The undershoot of the output voltage is measured as around 10 V, which is 3% of the output voltage. The transient state returns to the steady state within about 25ms. It shows that the proposed CF-IBDC converter shows good dynamic performance and enough stability in the transient operation. Since the control variable changes during the power transition

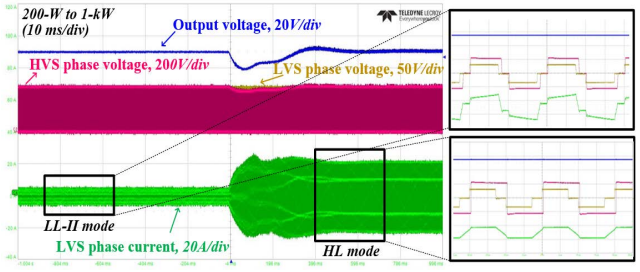

FIGURE 16. Experimental waveforms of step load response employing the proposed hybrid control algorithm from *LL-II* mode to *HL* mode.

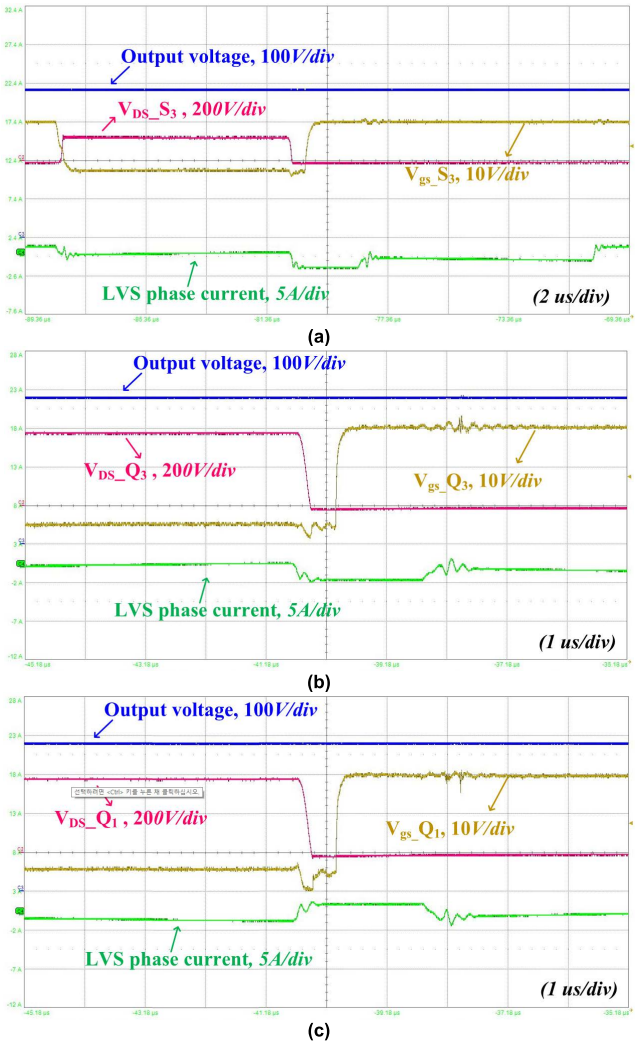

FIGURE 17. Experimental waveforms of double pulse test for power switches under the worst case of ZVS condition under $V_{bat} = 48$ V at no load condition: (a) Bottom switches of S_4 in LVS, (b) Upper switches of Q_1 in HVS, (c) Bottom switches of Q_4 in HVS.

from ϕ_{PS} to D_2 and from D_2 and ϕ_{PS}, the transient time seems to be relatively long. However, as the proposed hybrid control algorithm can maximize the efficiency of battery applications. Using the uninterrupted power flow control of the entire load range with only a single control variable, the transient time duration of ESS is less important than the case of steady-state operations.

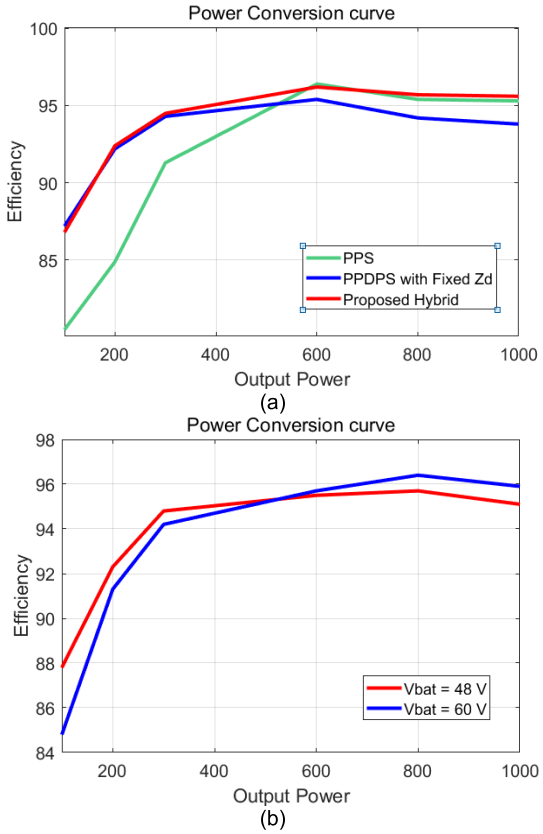

FIGURE 18. Power conversion efficiency curves: (a) Comparison between the proposed and conventional algorithms, (b) According to battery voltage.

B. SOFT SWITCHING WAVEFORMS

Fig. 17 shows the double pulse test waveforms of power switches to verify the ZVS conditions of the proposed hybrid control algorithm. The worst case of the ZVS condition is the lowest battery voltage at the no-load condition. In Fig. 17, the gate voltage, the drain-to-source voltage, and the leakage inductor current of the bottom switches in the LVS of S_4 and the upper and bottom switches in the HVS of Q_1 and Q_4 are captured. As shown in Fig. 17, the soft-switching capability can be obtained even under the no-load condition with the lowest V_{bat}. The bias current of $I_{Ls,before,r}$ shown in Fig. 12 is selected as the smallest value to decrease the circulating current. The experimental waveforms demonstrate that the theoretical analysis in Section III-2 of the ZVS condition is well achieved for the full load range.

C. POWER CONVERSION EFFICIENCY

Fig. 18 shows the power conversion efficiency curves according to load and battery voltage variations. Fig. 18-(a) shows the comparison of power conversion efficiency between the proposed control algorithm (red line) and the conventional control algorithms of the PPS (green line) and the PPDPS with ΔT (blue line) when V_{bat} is 48 V. Under the light

load condition, the efficiency when the PPDPS with ΔT is employed is significantly higher than the case of the PPS control. This is because the ZVS can be achieved under the former control method under low RMS phase current. While, at the heavy load condition, the PPS modulation makes high efficiency compared with the PPDPS due to the decrement of the circulating current in the secondary side, which induces low conduction loss. Since the proposed algorithm is employed by the PPDPS with ΔT at the light load condition and by the PPS at the heavy load condition, the efficiency can be maximized. Therefore, the efficiency of the proposed algorithm is matched by PPDPS with ΔT under light load conditions, and by PPS under the heavy load condition, i.e., measured higher efficiency in most of the entire load range than the conventional control algorithm.

Fig. 18-(b) shows efficiency curves according to battery voltage conditions of 48 V and 60 V. The maximum power conversion efficiency is measured as 96.67% at 800 W under 60 V of V_{bat}. The overall power conversion efficiency is relatively high except for very light load conditions since the ZVS capability can be obtained for all the active switches. Since the core loss of the DC inductor and the transformer is dominant at the light load condition, efficiency becomes low when V_{bat} is 48 V compared with the case of 60 V. In the cases of the heavy load condition, the conduction loss accounts for most of the total power losses. Therefore, efficiency becomes low when V_{bat} is 60 V compared with the case of 48 V, which is the opposite situation of the light load condition.

V. CONCLUSION

This paper proposes the effective hybrid switching modulation to overcome the limitations of the existing control algorithm and to improve the power conversion efficiency under the light and heavy load conditions of the CF-IBDC. By adopting the fixed Z_d and designing DC-filter based on the theoretical analysis at light load conditions, the entire ZVS range can be guaranteed. To minimize the circulating current and the reactive power, the duty cycle of the secondary sides is changed according to load conditions. In addition, the proposed hybrid algorithm controls the decoupled duty cycle of the secondary sides and the phase shift angle between the primary and secondary sides, which can mitigate control complexity.

The effectiveness of the proposed hybrid control algorithm is verified by the prototype of 1 kW CF-IBDC from 48 to 60 V of V_{bat} at 380 V of V_{out}. The ZVS conditions of all the power switches are verified using the double pulse test. The performance of the proposed control algorithm is also verified by the steady-state operation and the dynamic response. Based on the experimental results with the proposed hybrid algorithm, the efficiency of both light and heavy load conditions is improved to 3.3 % and 1.8 %, respectively, compared with the conventional control algorithms. The highest efficiency is measured as 96.67% at 800 W under $V_{bat} = 60$ V and the effectiveness of the proposed switching pattern is demonstrated.

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