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CMOS Backplane Pixel Circuit With Leakage and Voltage Drop Compensation for an Micro-LED Display Achieving 5000 PPI or Higher

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ABSTRACT Micro-displays based on micro-LEDs are becoming more and more attractive in AR/MR (Augmented/Mixed Reality) applications. A display size of 0.5 to 0.7-inch is preferred, with 5,000 PPI (Pixel Per Inch) or higher. Due to this pixel density and size, a CMOS (Complementary Metal-Oxide-Silicon) backplane is an ideal solution to drive these pixelized micro-LEDs. As the required pixel size gets smaller, the design of the appropriate pixel circuit becomes more challenging. The simplest 2T1C (2 transistors & 1 capacitor) pixel circuit has potential problems, due to the leakage current of the switch transistor and the voltage drop on the matrix array layout. In this paper, a pixel circuit is proposed as a solution to overcome these two issues. Our simulation results show that the variation of the driving current to the LED is improved by 95 %, and the IR drop error rate is around 2.2 % compared to the 2T1C circuit. The test results also show that the error rate of I_{PIXEL} for the whole region of display is under 2.5 %. This work is verified using a test chip implementation with 180 nm CMOS process technology.

INDEX TERMS Micro-LED display, microdisplay, high-resolution, DRAM type, voltage driving, low leakage switch, IR drop compensation, CMOS backplane, and high-PPI.

I. INTRODUCTION

Micro-display technology based on micro-LEDs is still in the early stages of commercial deployment, but it is expected to slowly replace the existing display technologies, such as LCDoS (Liquid Crystal Display on Silicon) or OLEDoS (Organic Light Emitting Diode on Silicon) displays, for certain applications [1]. One of the biggest hurdles for commercializing micro-LED displays is the transfer technology by which the pixelized LEDs are attached to the backplane. Because of this, the following applications are likely to be among the early adopters of these micro-LED displays. The first are micro-display applications for AR/MR (Augmented-/Mixed-Reality), where the silicon CMOS backplane IC and LEDs are hybridized by wafer-to-wafer bonding [2]. The second are super-size display applications, such as outdoor signage or TV screens larger than 110 inch,

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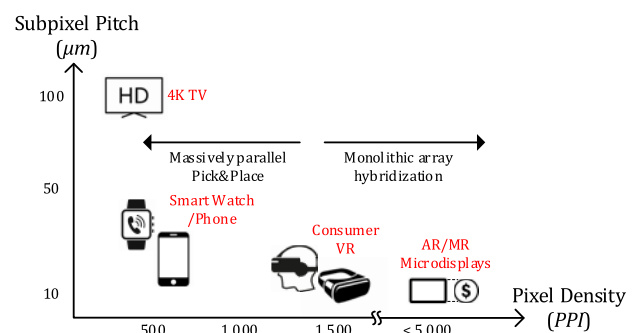


FIGURE 1. Pixel pitch vs. pixel density [1].

which cannot be manufactured using the existing glass-based flat panel displays [3]. Fig. 1 shows the requirements for each display application in terms of pixel pitch and their pixel density, or PPI.

AR/MR applications require a pixel density of 5,000 PPI or higher for 0.5- to 0.7-inch displays. Thus, recent research has concentrated on these requirements [4], [5].

As shown in Fig. 1, the pixel pitch for AR/MR should be in the range of $2\ \mu\text{m} \sim 5\ \mu\text{m}$. The display size of the microdisplay is less than 1 inch [6], [7]. For this reason, silicon CMOS process technology is an ideal solution that lets us manufacture a backplane with a smaller pixel size [8] and integrated peripheral circuitry.

Each pixel contains a current-driving circuit in order to drive the micro-LED. The maximum driving current to each LED is in the range of a couple of micro-ampere due to the size of the LED. The brightness of the LED is directly proportional to the driving current. The pixel size required by a certain application confines the freedom of the pixel circuit design.

In general, there are two approaches to driving the LED in such high PPI display applications. The first one, PAM (Pulse Amplitude Modulation), is the analog control of pixel current or voltage in order to adjust gray level. The other is PWM (Pulse Width Modulation), in which the gray level is adjusted by controlling the turn-on time of the LED using a maximum driving current. The PAM scheme is often called “voltage driving”, since the voltage information is used to control the driving current level to the LED. On the other hand, PWM is often called “current driving” or “digital driving”, since it uses a fixed driving current while controlling the pulse width to adjust the light intensity of the LED.

The PAM driving scheme can easily achieve a higher pixel density, per a given display size, thanks to a relatively simple pixel circuit structure. However, the leakage current at the transistors of the pixel circuit deteriorates the display uniformity. It also requires rather complex peripheral circuitry, which results in higher power consumption. The PWM driving scheme needs higher transistor counts in the pixel circuit compared to the PAM scheme, since it requires combinational logic gates and SRAM (Static Random-Access Memory) cells. However, it has the advantage of using a simpler peripheral circuitry with less power consumption.

This paper proposes a CMOS backplane based on a PAM-based pixel circuit, along with a solution to the leakage current and IR drop problems. A display resolution of 1280RGB x 768 is used to verify the proposed backplane. The driving current to each micro-LED is limited to a maximum of $2\ \mu\text{A}$ after consideration of the total power consumption of the display module.

II. 2T1C PIXEL CIRCUIT

A. 2T1C CIRCUIT

A CMOS backplane contains two main function blocks: an active-matrix pixel array, and its peripheral circuit to drive the pixel array. All these functions are included on a single silicon backplane [9]. The pixel circuit stores the display data in a voltage form and converts it into a current form to drive the LED, while maintaining its value during a given frame time (T_{FRAME}).

The simplest pixel circuit is a 2T1C structure, as shown in Fig. 2 [10], [11]. Micro-LEDs can be configured by either

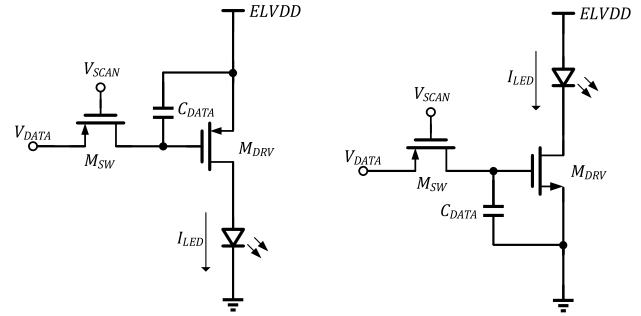


FIGURE 2. 2T1C pixel circuit: common cathode (left) & common anode (right).

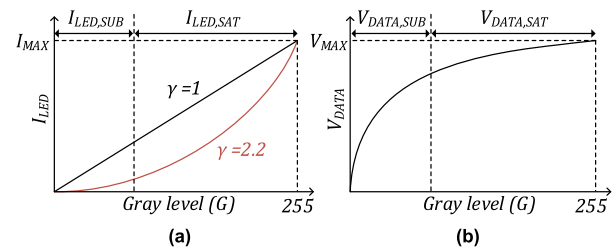


FIGURE 3. The LED grayscale curve of a pixel: Current vs Grayscale (a), Voltage vs. Grayscale (b).

common-cathode or common-anode topology. The pixel circuit consists of only three components: a switch transistor (M_{SW}), a driving transistor (M_{DRV}), and a storage capacitor (C_{DATA}). The basic operation is as follows: when M_{SW} is turned on by V_{SCAN} , the value of V_{DATA} is stored at C_{DATA} , which sets the V_{GS} bias of M_{DRV} . Then, the voltage level stored at C_{DATA} is converted by M_{DRV} to the amount of current going to an LED (I_{LED}), which consequently controls the light intensity. Even after M_{SW} is off, its current level is kept by the charge stored at C_{DATA} . Therefore, maintaining the charge during a given frame time is critical to ensuring the consistent light intensity of the LEDs.

A typical display for an AR/MR application requires grayscale with at least 8-bit or 256 gray levels of a color. The driving current, I_{LED} , is proportional to the light intensity of an LED. It often has a non-linear relationship to the gray scale input, as shown in Fig. 3(a). A typical display uses a specific value of the gamma correction value, $\gamma = 2.2$. I_{LED} is determined by [12]

$$I_{\text{LED}} = I_{\text{MAX}} \left(\frac{G}{255} \right)^{\gamma} = \alpha \cdot G^{\gamma} \quad (1)$$

where α is $I_{\text{MAX}}/255^{\gamma}$, and G is the grayscale input with 256 gray levels. I_{LED} has different values depending on the subthreshold and saturation region of M_{DRV} , as shown below: [13]

$$I_{\text{LED,SUB}} = \eta e^{\frac{(V_{\text{GS}} - V_{\text{TH}})}{S}} \quad (2)$$

$$I_{\text{LED,SAT}} = k \left(\frac{W}{L} \right) (V_{\text{GS}} - V_{\text{TH}})^2 \quad (3)$$

where η is a scale factor [14], S is the subthreshold swing of the transistor, k is the process transconductance parameter, and V_{TH} is the threshold voltage of M_{DRV} . Assuming that the switch transistor is ideal, (1), (2), and (3) produce the relationship between V_{DATA} and G as

$$V_{DATA,SUB} = S\gamma \ln G + C \quad (4)$$

$$V_{DATA,SAT} = \alpha' G^{\frac{\gamma}{2}} + V_{TH} \quad (5)$$

where α' is $\alpha/\sqrt{k(W/L)}$, and C is $V_{TH} + S \ln(\alpha/2\eta)$. With a typical gamma correction value of $\gamma = 2.2$, the $V_{DATA,SUB}$ has a logarithmic relationship to G , and the $V_{DATA,SAT}$ is proportional to $G^{1.1}$, as shown in (4), (5) and Fig. 3(b).

Assuming the maximum voltage of the V_{DATA} is 1.8 V, the step size of V_{DATA} for the gray scale at the lower gray region is around 162 mV. However, in the higher grayscale region it would be as small as 1.4 mV. This means that the grayscale of the LED light will be affected by just a few milli-volt difference in the V_{GS} value of M_{DRV} . On the other hand, the step size of I_{LED} has the opposite tendency, since it is quadratically proportional to the V_{GS} of M_{DRV} . Thus, it has a smaller value in a low grayscale region, and a larger value in a high grayscale region. Table 1 shows the minimum step size of those parameters in each grayscale region. The mismatch problem becomes critical, regardless of whether grayscale is in the low or high region.

TABLE 1. Gamma Step size of V_{DATA} and I_{LED} assuming maximum $V_{DATA} = 1.8$ V.

Grayscale region	ΔV_{DATA}	ΔI_{LED}	Critical parameter
Lowest (0-1)	162 mV	34.7 pA	ΔI_{LED}
Highest (254-255)	1.4 mV	16.4 nA	ΔV_{DATA}

The mismatch among pixel circuits of the array would severely affect the uniformity of the display. Thus, it is necessary to minimize the mismatch between the V_{DATA} among the pixel circuits.

B. THE PROBLEM OF THE 2T1C CIRCUIT

There are many variations on the basic 2T1C circuit to improve the performance of the pixel circuit [15], [16]. The V_{GS} bias of M_{DRV} in the 2T1C circuit should be maintained during a given frame time (T_{FRAME}) to display the target gray scale. Therefore, the amount of charge at C_{DATA} should not be changed during a given frame time. However, leakage current affects the amount of charge at the storage capacitor. This becomes worse when there is limited space for the storage capacitor due to the allowable pixel size. Therefore, a compensation technique for the leakage current must be considered.

Fig. 4 shows a model of a switch transistor, including its leakage current. The leakage current, I_{LEAK} , can be expressed as

$$I_{LEAK} = I_{OFF} + I_{D_REV} \quad (6)$$

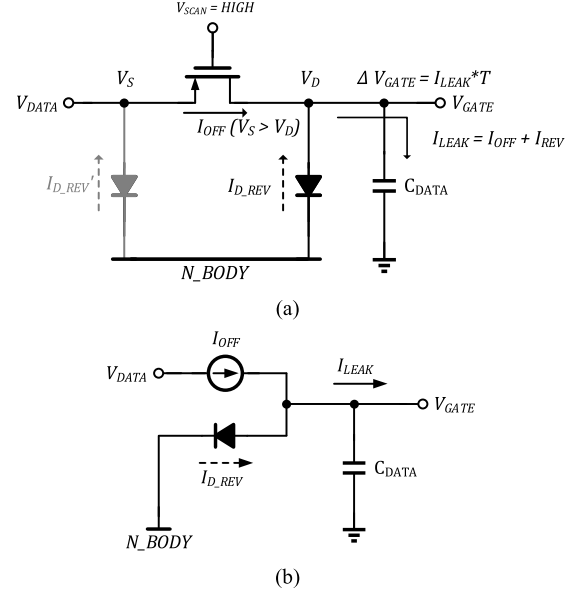


FIGURE 4. (a) I_{LEAK} model on switch device and C_{DATA} , (b) simplified circuit.

where I_{OFF} represents the off-current through the channel under the gate of the switch transistor, and I_{D_REV} is the reverse-bias current of the parasitic diode of the switch transistor.

I_{LEAK} is represented as a summation of I_{OFF} and I_{D_REV} , which can be expressed as below [13]:

$$I_{OFF} = \eta e^{-\frac{V_{TH}}{S}} \quad (7)$$

$$I_{D_REV} \propto V_{D_REV} \quad (8)$$

where V_{D_REV} is the applied reverse bias [17]. Equation (7) shows I_{OFF} at $V_{GS} = 0$ [14], which is a function of V_{TH} . Fig. 5 shows the leakage current behavior based on the bias parameter.

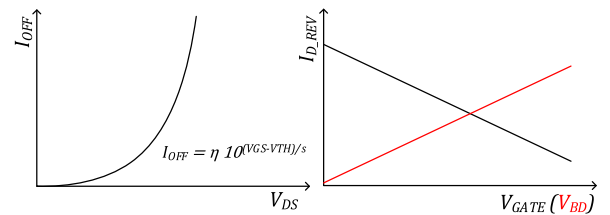


FIGURE 5. Current depending on bias condition: I_{OFF} (left) & I_{REV} (right).

According to (7) and (8), I_{OFF} increases as the V_{TH} of the switch transistor decreases, while I_{D_REV} decreases as the V_{BD} , the body-drain voltage, decreases. I_{D_REV} cannot be controlled by design because V_{GATE} , the drain of the switch transistor, is always set by the image data value. Therefore, only I_{OFF} can be controlled by the design parameters. It can be found using the following:

$$V_{TH} = V_{TH0} - (V_{DS}) e^{-L/l_d} \quad (9)$$

where V_{TH0} is the intrinsic threshold voltage of a transistor, V_{DS} is the applied drain-source bias, L is the drawn gate length, and l_d is the minimum gate length. It is shown in Fig. 6.

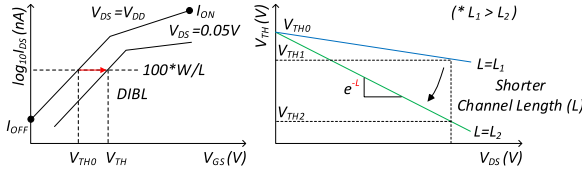


FIGURE 6. I_{OFF} characteristic (left) & V_{TH} role-off (right).

Equation (9) shows that the V_{TH} of the transistor is dependent on V_{DS} . This phenomenon is called the DIBL (Drain-Induced-Barrier-Lowering) effect [18]. When the finer CMOS process technology is used, I_{OFF} increases due to the short-channel effect. This means that the smaller the V_{DS} , the smaller the I_{OFF} .

Depending on the bias condition at the source and the drain node of the switch transistor, I_{LEAK} can flow in either direction and then affect the amount of charge at C_{DATA} . This change in the charge amount directly affects not only the V_{GS} bias of the driver transistor, but also the gray scale.

Fig. 7 and Table 2 show three cases of the bias condition at the switch transistor. Assuming that I_{D_REV} always flows in the direction of the charging C_{DATA} due to the reverse-biased diode, I_{LEAK} can be categorized into three cases: 1) when $V_D > V_S$, I_{OFF} flows in the direction of the discharging C_{DATA} ; 2) when $V_D \approx V_S$, I_{OFF} is almost zero and I_{LEAK} is determined only by I_{D_REV} , (in this case, C_{DATA} is charging); 3) when $V_S > V_D$, I_{OFF} flows in the direction of the charging C_{DATA} . This should be considered the worst case.

TABLE 2. I_{LEAK} cases with bias condition.

Case	I_{OFF}	I_{LEAK}	C_{DATA} (or V_{GS})	Worst Pattern	Re- marks
$V_D > V_S$	$I_{OFF} < 0$	$- I_{OFF} + I_{D_REV}$	Discharged	White \rightarrow Black	-
$V_D = V_S$	$I_{OFF} = 0$	I_{D_REV}	No change	-	Best
$V_D < V_S$	$I_{OFF} > 0$	$ I_{OFF} + I_{D_REV}$	Charged	Black \rightarrow White	Worst

Whatever the case, ideally the change in V_{GS} or $|\Delta V_{GS}|$ due to the leakage current would be small enough not to affect the target gray scale during the given frame time. In other words, $|\Delta V_{GS}|$ should be less than $|\Delta V_{GAMMA}|$, as in

$$|\Delta V_{GS}| = \frac{I_{LEAK} \cdot T_{FRAME}}{C_{DATA}} < |\Delta V_{GAMMA}| \quad (10)$$

where T_{FRAME} is the frame time of the display, and ΔV_{GAMMA} is the voltage step of a gray scale. $|\Delta V_{GAMMA}|$ varies in each of the lines because of the nature of the array driving pattern. The resolution of the V_{DATA} step size is different at the

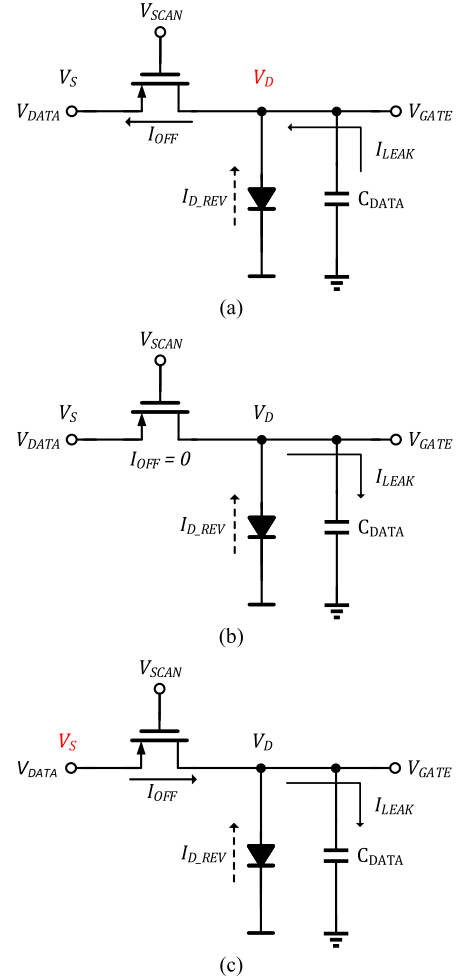


FIGURE 7. I_{LEAK} tendency on C_{DATA} : (a) $V_D > V_S$, (b) $V_D = V_S$, (c) $V_D < V_S$.

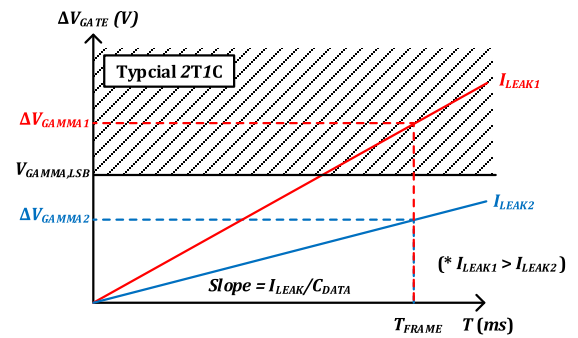


FIGURE 8. ΔV_{GATE} with I_{LEAK} on the C_{DATA} graph.

higher- and lower-gray scale regions. Unfortunately, in a typical 2T1C, $|\Delta V_{GS}|$ is greater than $|\Delta V_{GAMMA}|$ because of the large leakage current. Fig. 8 shows a linear curve representing the ratio between I_{LEAK} and C_{DATA} . I_{LEAK} should be reduced enough to lower the curve slope, so that the ΔV_{GAMMA} during a given T_{FRAME} is less than the minimum step size of the gamma curve, $V_{GAMMA,LSB}$ in the case of I_{LEAK2} .

According to (7), the capacitance should be maximized at a given pixel dimension, while minimizing the leakage current.

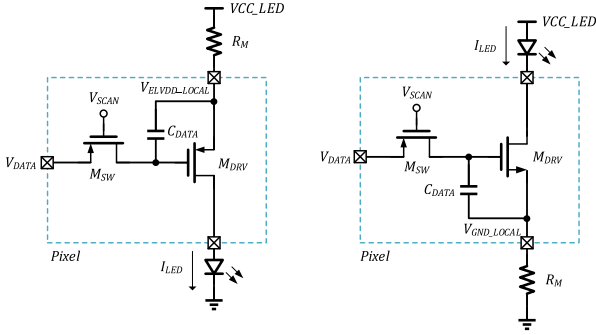


FIGURE 9. Pixel Circuit model for an IR drop.

When a smaller pixel dimension is required, there is a tradeoff between the capacitance value and the leakage current.

Another critical problem is the IR drop, caused by the metal routing trace between the reference node for each pixel and the global reference node or I/O pad for the backplane [19]. Due to the layout constraints of the pixel array, the power/reference node for V_{DATA} and V_{GS} does not use the same reference point. As explained earlier, the driving current to an LED is determined by the V_{GS} of M_{DRV} , which comes from the V_{DATA} . This means that the I_{LED} can be different from the expected value, due to the IR drop in the pixel circuit. Therefore, the real display image would have a deviation from the target display image. This problem becomes more severe at a lower gray scale, since the step size of the lower gray scale would be in the range of \sim pA. Fig. 9 represents a model metal line, R_M , connected to the source of M_{DRV} . Equation (11) shows that V_{DATA} deviates in the metal line as follows:

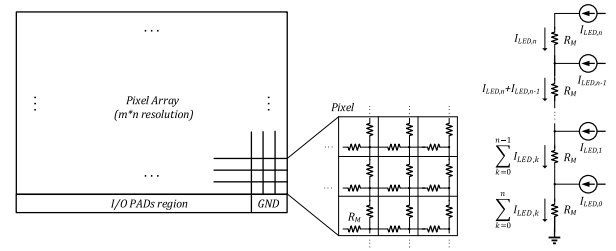
$$V_{DATA} = V_{GS} + V_{DROP} \quad (11)$$

where V_{DROP} can be expressed as

$$V_{DROP}|_{k^{th} \text{ pixel}} = \sum_1^n (n-k)^2 R_M I_{LED} \quad (12)$$

where k represents the row number of the display, n the whole row number of the display, and R_M the resistance of the metal routing trace. Equation (12) shows that V_{DROP} with the k^{th} pixel can vary on a specific pixel location inside the array and the mode of the display. In this case, it is assumed that the $I_{LED,k}$ in all rows are the same. The I/O pads are placed on the bottom perimeter of the backplane, so the V_{DATA} of the top pixel has the worst voltage drop. Fig. 10 shows an example of the IR drop on a pixel array. Even if exactly the same image data or V_{DATA} is written into all pixels, each micro-LED would have a different brightness, which in turn would affect the uniformity of the display image. It could also become worse when the total number of pixels increases.

In summary, the 2T1C pixel circuit has the advantage of achieving smaller pixel dimensions, but the display image is prone to leakage, as well as an IR drop problem. In order to achieve a smaller pixel size with a uniform display, a more sophisticated pixel circuit is required.

FIGURE 10. Simple example with IR drop issue for R_{GND} on a pixel array.

III. PIXEL CIRCUIT DESIGN

A. LEAKAGE CURRENT

In order to minimize the leakage current, a “T-Switch” structure has been introduced [20]. Fig. 11 shows the structure of the “T-Switch”. I_{OFF} is greatly reduced with this structure, thanks to V_{HOLD} which modifies (7) so that it becomes

$$I_{OFF} = \eta e^{\left(\frac{-V_{HOLD} - V_{TH}}{S}\right)} \quad (13)$$

where V_{HOLD} is the bias voltage connected to V_{SAMPLE} through the switch transistor, M_3 . However, this scheme adds an extra transistor and bias source, V_{HOLD} , to the pixel circuit. This addition could become a burden in the layout when the pixel size gets smaller.

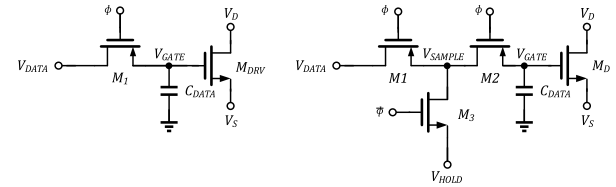


FIGURE 11. Conventional (left) and improved (right) pass gates structure introduced in [16].

In this paper, we investigated alternative solutions which aim to minimize the leakage current. The first is to use a ground reference instead of V_{HOLD} at the source node of M_3 , thus removing the extra bias requirement, as shown in Fig. 12. If the switch control signal, ϕ , is low, M_3 is off while M_1 & M_2 are on. In this case, V_{GATE} becomes the same as V_{DATA} . When the transistors M_1 & M_2 are off, then V_{GATE} and V_{DATA} nodes are disconnected. The intermediate node, V_{SAMPLE} , is set to the ground reference. This reduces the I_{OFF} of M_2 at the lower gray levels, thereby avoiding the above-mentioned worst I_{LEAK} case. However, this approach still has a problem

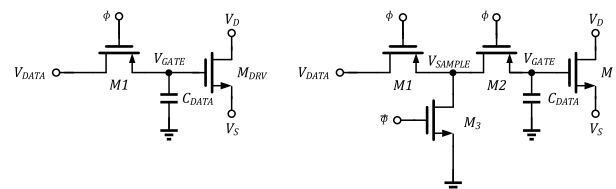


FIGURE 12. Conventional (left) and improved (right) pass gates with the first proposed method.

at higher gray levels, where I_{OFF} increases as the V_{DS} of M_2 becomes the highest value.

The other approach investigated here is to simply split the switch transistor into two transistors in series, as shown in Fig. 13. This scheme creates a V_{SAMPLE} node with the parasitic capacitors, M_1 and M_2 (C_{G1} & C_{G2}), without requiring an extra bias voltage. It reduces the difference between V_{GATE} and V_{SAMPLE} by delaying the change of V_{SAMPLE} with C_{G1} & C_{G2} because the V_{SAMPLE} usually follows the V_{DATA} . Therefore, the V_{DS} of M_2 is close to zero, minimizing the I_{OFF} of M_2 across the entire gray scale. In addition, it does not require the extra transistor, as is the case in Fig. 12.

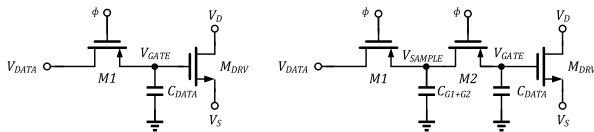


FIGURE 13. Conventional (left) and improved (right) pass gates with the second proposed method.

B. IR DROP

To alleviate the IR drop problem, the V_{GS} bias of the M_{DRV} should be independent of any ground reference. Fig. 14 illustrates the proposed solution by adding a transistor to avoid the problem caused by the IR drop. Unlike the 2T1C pixel circuit, the bias current to the LED is determined by a combination of the gate-source voltages of M_{DRV_N} and M_{DRV_P} . The M_{DRV_P} configured with a PMOS is always on, because the gate is connected to the local reference node, and the current of the pixel is determined to be

$$\begin{aligned} I_{LED} &= k_n \frac{W}{L} (V_{DATA} - V_S - V_{THN})^2 \\ &= k_p \frac{W}{L} (V_S - V_{THP})^2 \end{aligned} \quad (14)$$

where k_n and k_p are the process transconductance parameters of each MOSFET, and V_S is the source voltage at each of M_{DRV_N} and M_{DRV_P} .

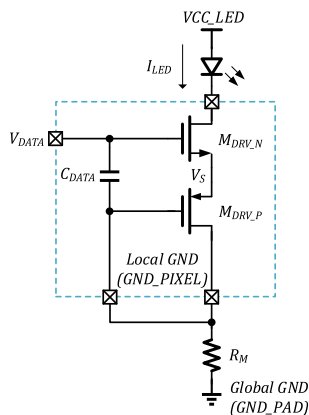


FIGURE 14. Pixel Structure with an IR drop compensation.

C. PROPOSED PIXEL CIRCUIT

Fig. 15 shows the proposed pixel circuit, 4T1C, which combines a low leakage switch structure and an IR drop compensation circuit.

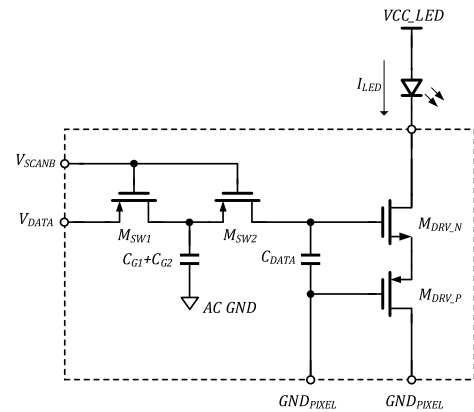


FIGURE 15. Proposed sub-pixel circuit with a solution of subthreshold leakage and IR drop.

The pixel size of the 4T1C pixel circuit can be minimized by using a low breakdown voltage transistor with the minimum gate length at any given CMOS process. However, the transistor directly connected to the LED of the pixel should have a high enough breakdown voltage, because the LEDs often use a higher supply voltage than the ones used in normal logic transistor devices, due to the turn-on voltage requirement of the LEDs. In this paper, a 1.8 V power supply is used for the logic transistors. Therefore, a transistor with a high breakdown voltage, M_{REF_BIAS} , is added in order to provide a voltage clamp, as shown in Fig. 16. The voltage at the drain of M_{DRV_N} can be arbitrarily set by adjusting the V_{REF_BIAS} connected to the gate. The V_{REF_BIAS} is determined by the following expression:

$$I_{PIXEL} = k_{BIAS} \frac{W_{BIAS}}{L_{BIAS}} (V_{REF_BIAS} - V_D - V_{TH})^2 \quad (15)$$

where k_{BIAS} is the conduction parameter of M_{BIAS} , and V_D is the drain voltage of M_{BIAS} .

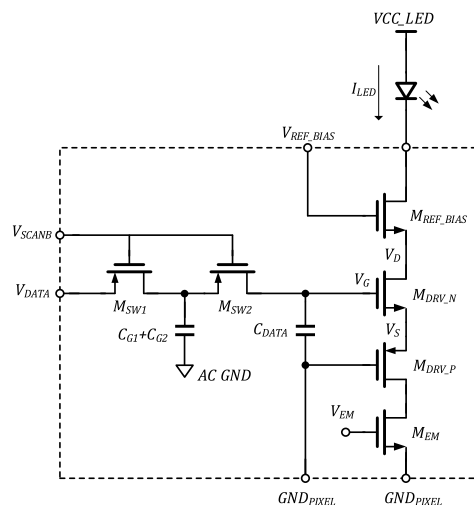


FIGURE 16. Completed sub-pixel circuit.

IV. SIMULATION AND MEASUREMENT RESULTS

A. SIMULATION RESULTS

Fig. 17 shows the pixel current (I_{LED}) behavior with different switch transistor configurations. V_{DATA} is set to the condition where the switch leakage current, I_{LEAK} , reaches the maximum. For the simulation, we used the image pattern of the white image data on the first line of the array and the black image data on the next line (WB...B Pattern). The simulation time was set as one frame time, or 16.6 ms. As shown in Fig. 17 and Table 3, I_{LED} at 2T1C circuit changed significantly during the one frame time, to 45.2 nA from $2\text{ }\mu\text{A}$ at the typical process corner, and to 4.43 nA at the worst process corner. With the proposed pixel circuit, it changed a lot less: to $1.57\text{ }\mu\text{A}$ at the typical process corner model, and to $1.02\text{ }\mu\text{A}$ at the worst process corner. Thus, I_{LED} leakage is improved by 75.9 % at the typical corner and 51.3 % at the worst corner.

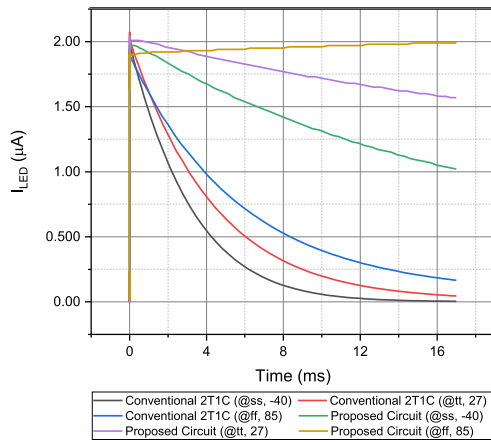


FIGURE 17. I_{LED} leakage (White to Black) with conventional 2T1C circuit and proposed pixel circuit.

TABLE 3. I_{LED} behavior at 1 frame time (T_{FRAME}).

Pattern	2T1C Pixel	Proposed Pixel	Improvement
WB...B	45.2 nA (typical)	1.57 μA (typical)	75.9 %
	4.43 nA (worst)	1.02 μA (worst)	51.3 %
BW...W	219 nA (typical)	11.3 nA (typical)	94.8 %
	354 nA (worst)	17.7 nA (worst)	95.0 %

The simulation results of other cases are shown in Fig. 18, Fig. 19, and Fig. 20, Table 3, and Table 4. As shown in these figures and tables, I_{LED} and V_{GATE} behavior in the proposed circuit is improved in all cases, compared to the conventional 2T1C circuit.

Fig. 21 shows the error rate of the I_{LED} in the proposed pixel circuit under an IR drop in the local GND line, which is from the global GND line on the I/O pads. The IR drop error rate is defined using the following equation [19]:

$$\text{Error rate}(\%) = \frac{I_{LED0} - I_{LED}}{I_{LED0}} \times 100 \quad (16)$$

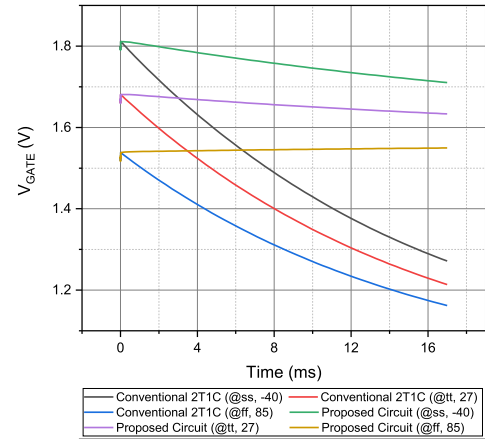


FIGURE 18. V_{GATE} of driving transistor leakage (White to Black) with conventional 2T1C pixel circuit and proposed pixel circuit.

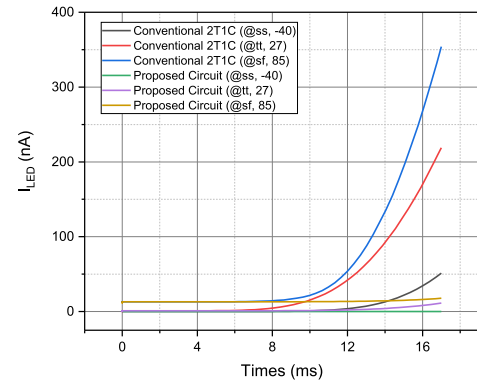


FIGURE 19. I_{LED} leakage (Black to White) with conventional 2T1C pixel circuit and proposed pixel circuit.

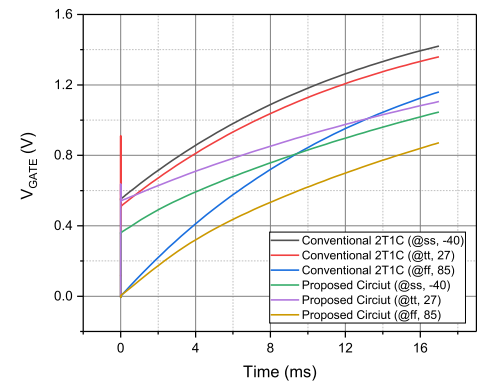


FIGURE 20. V_{GATE} of driving transistor leakage (Black to White) with conventional 2T1C pixel circuit and proposed pixel circuit.

where I_{LED0} is the driving current in the ideal case, and I_{LED} is the driving current with an IR drop. In the case of a $2\text{ }\mu\text{A}$ driving current to the micro-LED, the error rate between the conventional 2T1C pixel circuit and the proposed pixel circuit is shown in Fig. 21. The error rate of the proposed pixel circuit is reduced significantly thanks to the IR drop

TABLE 4. V_{GATE} behavior at 1 frame time (T_{FRAME}).

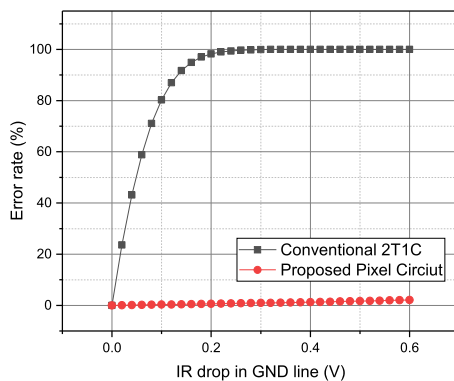
Image Pattern	2T1C Pixel Circuit	Proposed Pixel Circuit	Improvement
$WB \cdots WB$	1.21 V (typical)	1.63 V (typical)	25.0 %
	1.27 V (worst)	1.71 V (worst)	24.3 %
$BW \cdots BW$	1.36 V (typical)	1.11 V (typical)	21.9 %
	1.16 V (worst)	0.87 V (worst)	25.0 %

TABLE 5. Performance summary of the CMOS backplane.

Parameter	Specification
CMOS process technology	180nm
Power supply for logic/LED	1.8 V/5 V
Power dissipation	138.8mW* ¹
Die area	13.8 mm x 9.68 mm
Pixel size* ²	10 μ m x 10 μ m
Resolution	1280RGB x 768
PPI (sub-pixel base)	5,080

¹ Tested with the checker pattern image (BWBW...BW)

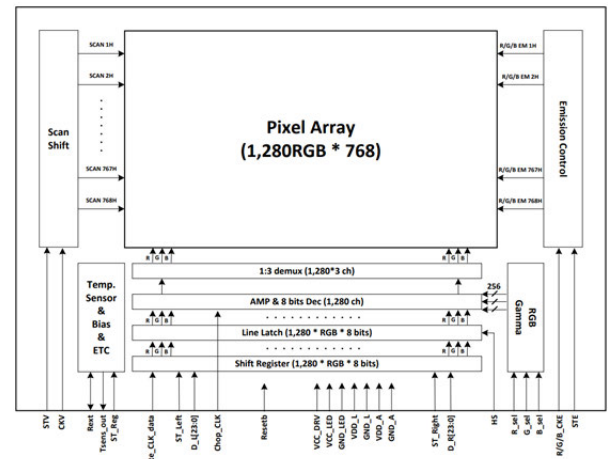
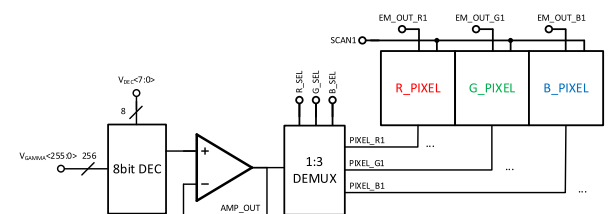
² Each pixel contains 2 by 2 (RGRB) sub-pixels

**FIGURE 21.** Error rate with IR drop on local GND line of conventional 2T1C pixel circuit and proposed pixel circuit.

compensation of the pixel circuit. It is suppressed under 2.2 % for $GND_{PIXEL} = 0.6$ V with the proposed pixel circuit.

B. MEASUREMENT RESULTS

Fig. 22 shows the overall functional block diagram of the CMOS backplane with the proposed pixel circuit. It includes the peripheral circuitry that drives the pixel array, including a scan driver, source amplifiers, a separate gamma generator for RGB color, and an emission control. The RGB pixel drive scheme for the proposed sub-pixel circuit is shown in Fig. 23. It is designed to support a separated 8-bit color control for RGB. One of the 255 gray scales, which is generated by the gamma generator, is delivered through DEC to the buffer amplifier. The output of this buffer is written into each pixel by R_SEL , B_SEL , and G_SEL through 1-to-3 DEMUX when the switch control signal (V_{SCAN}) is enabled. Then it is passed to the gate of the driving transistor inside R_PIXEL,

**FIGURE 22.** Top Block Diagram of CMOS Backplane.**FIGURE 23.** Block diagram of driving RGB pixel with the proposed sub-pixel.

G_PIXEL , or B_PIXEL , accordingly. The timing diagram of the driving RGB pixel is shown in Fig. 24.

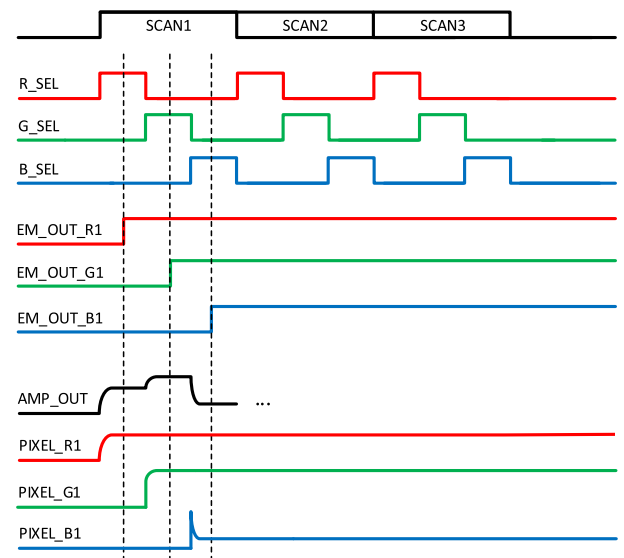
**FIGURE 24.** Timing diagram of driving RGB pixel with proposed sub-pixel.

Fig. 25 shows the die photo of the finished CMOS backplane IC which is fabricated using 180 nm CMOS process technology. The average power consumption is 138.8 mW.

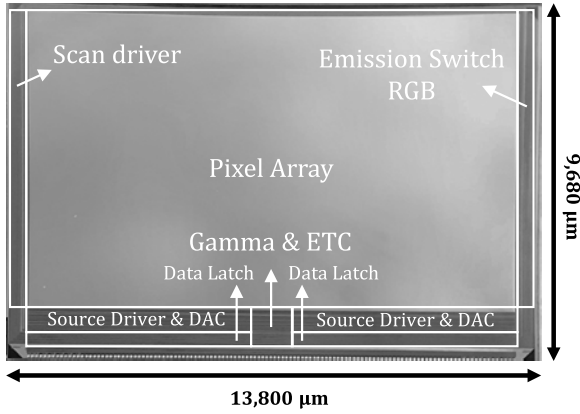


FIGURE 25. Die photo of the finished CMOS backplane.

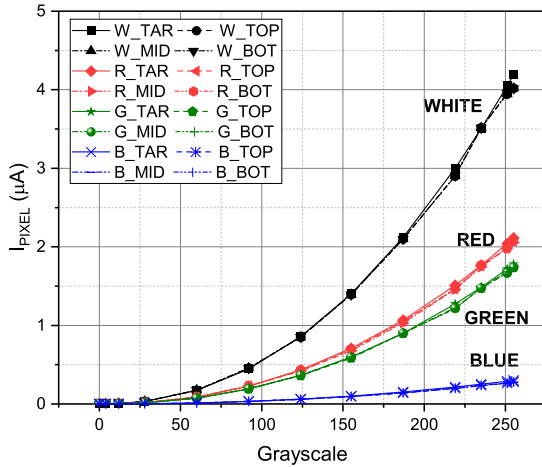


FIGURE 26. Simulated and measured I_{PIXEL} under the test pattern image. (5 line: White, Red, Green / 20line: Blue).

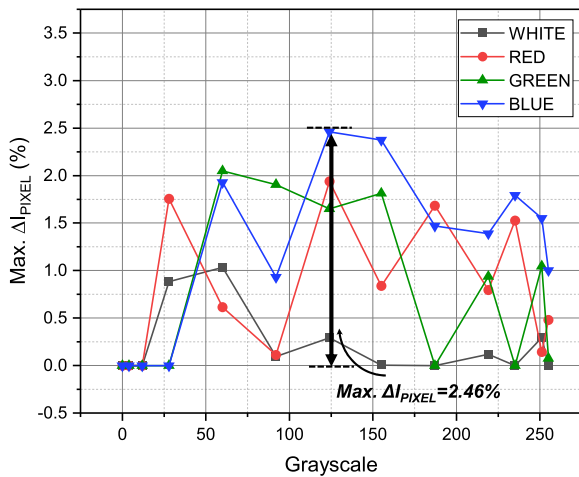


FIGURE 27. Maximum current difference ($\text{Max. } \Delta I_{PIXEL}$) at different test patterns.

The sub-pixel pitch is $5 \mu\text{m}$ and a single RGB pixel pitch is $10 \mu\text{m}$ (2 by 2 with RGBR sub-pixel structure).

Fig. 26 shows the simulated and measured I_{PIXEL} using the test images. In order to verify the IR drop compensation scheme of the proposed circuit, three test images were used: the top, middle, and bottom regions of the array.

(W/R/G/B)_TAR is the simulated target I_{PIXEL} , while (W/R/G/B)_TOP, (W/R/G/B)_MID, and (W/R/G/B)_BOT are the measured I_{PIXEL} in each test image. This simulation shows that the measured I_{PIXEL} fits well with the target I_{PIXEL} . Fig. 27 shows the maximum pixel current difference ($\text{Max. } \Delta I_{PIXEL}$) in each test image. The ΔI_{PIXEL} of each side is defined as (16), and $\text{Max. } \Delta I_{PIXEL}$ is the maximum ΔI_{PIXEL} with all the gray scales of each color.

The maximum ΔI_{PIXEL} of the white, red, green, and blue line pattern is 1.04 %, 1.94 %, 2.05 %, and 2.46 %, respectively. This proves that the non-uniformity of the pixel current with the proposed circuit is less than 2.5 % with the whole region on display.

V. CONCLUSION

In this paper, a 4T1C-based pixel circuit scheme has been introduced to address the degradation of the display image caused by the leakage current of the switch transistor, as well as the IR drop of the array. Due to the driving current, and the characteristics of its display gamma correction value, the proposed pixel circuit improves the uniformity of the display image. A detailed circuit analysis of the proposed pixel circuit, and its simulation results have been presented. The simulation and test results show that the proposed pixel circuit helps to solve the problems of the leakage current of the switch transistor and the IR drop.

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