Investigation of source-to-drain capacitance by DIBL effect of silicon nanowire MOSFETs

Seongjae Cho¹, In Man Kang², and Kyung Rok Kim³a)
¹ Inter-university Semiconductor Research Center (ISRC) and School of Electrical Engineering and Computer Science, Seoul National University, San 56–1, Sillim-dong, Gwanak-gu, Seoul 151–742, Republic of Korea
² School of Electronics Engineering, Kyungpook National University 1370, Sankyuk-dong, Buk-gu, Daegu 702–701, Republic of Korea
³ School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology, 100 Banyeon-ri, Eonyang-eup, Ulju-gun, Ulsan 689–798, Republic of Korea
a) krkim@unist.ac.kr

Abstract: We investigated the source-to-drain capacitance ($C_{sd}$) due to DIBL effect of silicon nanowire (SNW) MOSFETs. Short-channel SNW devices operating at high drain voltages have the positive value of $C_{sd}$ by DIBL effect. On the other hand, junctionless SNW MOSFETs without source/drain (S/D) PN junctions have negative or zero values by small DIBL effect. By considering the additional source-to-drain capacitance component, the accuracy of a small-signal model was significantly improved on the imaginary part of $Y_{22}$-parameter.

Keywords: silicon nanowire, source-to-drain capacitance, model

Classification: Electron devices, circuits, and systems

References

1 Introduction

As the channel length of metal-oxide-semiconductor field-effect transistor (MOSFET) decreases, the short-channel effects (SCEs) and drain-induced barrier lowering (DIBL) effect become important in terms of the device performance. To overcome the SCEs, the silicon nanowire (SNW) MOSFETs have been proposed [1, 2]. The conventional SNW MOSFETs, however, have the problem due to the DIBL effect by source/drain (S/D) P/N junctions. The unexpected change of channel inversion charges in MOSFETs results from the DIBL effect. Because the source-to-drain capacitance ($C_{sd}$) of transistors is fixed by inversion channel charges, the values of $C_{sd}$ are influenced by the DIBL effect [3]. In this paper, we investigate the values of $C_{sd}$ for conventional SNW MOSFET with long and short-channel lengths. Moreover, we extract the capacitances of junctionless SNW (JLSNW) MOSFET [5]. JLSNW MOSFET is the device structure based on junctionless transistors proposed by J. P. Colinge research group [4, 5], and it can suppress the DIBL effect because of structure without S/D P/N junctions. To exactly model the effects of DIBL on $C_{sd}$ in normal SNW MOSFETs, the additional source-to-drain capacitance ($C_{sdx}$) has to be added to RF model [3].

2 Device structures and RF model of MOSFETs

In this work, the SNW n-type MOSFETs have gate length ($L_G$) of 30 nm and 1 μm. JLSNW n-type MOSFET has $L_G$ of 30 nm. TCAD device simulation is performed by using ATLAS 3-D simulator [6]. The channel and S/D concentrations of SNW nMOSFET are $5 \times 10^{18}$ cm$^{-3}$ and $1 \times 10^{20}$ cm$^{-3}$, respectively. The n-type doping concentration of JLSNW nMOSFET is constant through the channel and S/D regions as $2 \times 10^{19}$ cm$^{-3}$.

Figure 1 (a) shows a small-signal equivalent circuit of RF MOSFETs to extract $C_{sd}$ for SNW and JLSNW MOSFET. $C_{sdx}$ is the additional component reflecting the charge variation due to DIBL effect in the short-channel MOSFETs [3]. $\tau$ is the time constant of transport delay [7]. The term of $g_{ds}/(1+j\omega\tau)$ shown in Fig. 1 (a) can be modeled by the parallel combination of $g_{ds}$ and $C_{sd}$ as shown in Fig. 1 (b) [7]. Therefore, $C_{sd}$ is given by $-\tau g_{sd}$ as follows:

$$\frac{g_{ds}}{1+j\omega\tau} \approx g_{ds} - j\omega\tau g_{ds} = g_{ds} + j\omega C_{sd}$$

Without $C_{sdx}$ in Fig. 1 (a), the imaginary part of $Y_{22}$-parameter (Im($Y_{22}$)) is derived by following equation.

$$\text{Im}(Y_{22}) = -\omega\tau g_{ds} + \omega C_{gd} + \frac{\omega g_m R_g C_{gd}}{1 + \omega^2 R_g^2 (C_{gs} + C_{gd})^2}$$
Since $-\tau g_{ds}$ is equal to $C_{sd}$, we can extract $C_{sd}$ by Eq. (2). The extraction results of $C_{sd}$ will be discussed in next section.

### 3 Parameter extraction and model verification

Figure 2 shows the extraction results of $C_{sd}$ and $C_{sdx}$ for SNW and JLSNW MOSFET. Eqs. (1) and (2) show that $C_{sd}$ has the negative or zero values. $C_{sd}$ is defined as the following equation [7].

\[
C_{sd} = -\frac{dQ_s}{dV_d}
\]  

(3)

where $dQ_s$ is the change of channel inversion charges and $dV_d$ is the change of drain voltage. Generally, $C_{sd}$ is negative in non-saturation region and becomes zero in saturation region for long-channel devices [7]. However, as shown in Fig. 2 (a), the values of $C_{sd}$ without $C_{sdx}$ for SNW MOSFET with short-channel are positive at high drain bias conditions. All the devices have the same channel radius ($R_{ch}$) of 5 nm. As the drain voltage increases, the DIBL effect occurs in the conventional SNW MOSFET with S/D PN junctions and the injection of electrons from source region increases. And then $C_{sd}$ becomes positive value. On the other hand, $C_{sd}$ is always negative or zero in long-channel SNW MOSFET and JLSNW MOSFET regardless of bias conditions. Since the JLSNW MOSFET doesn’t contain S/D PN junctions and current flows in heavily doped body channel, the DIBL effect of JLSNW device is suppressed. It reveals that junctionless device has the robust immunity to DIBL effect.
To exactly model the DIBL effect on $C_{sd}$, the additional component has to be added to a conventional small-signal equivalent circuit model of a MOSFET [3]. Adding $C_{sdx}$ to the small-signal model, $\text{Im}(Y_{22})$ is derived as follows:

$$\text{Im}(Y_{22}) = \omega C_{sdx} - \omega \tau g_{ds} + \omega C_{gd} + \frac{\omega g_m R_g C_{gd}}{1 + \omega^2 R_e^2 (C_{gs} + C_{gd})^2}$$  \hspace{1cm} (4)

By the addition of $C_{sdx}$, $C_{sd}$ is given by $C_{sdx} - \tau g_{sd}$. Figure 2 (b) shows the extraction results of $C_{sdx}$. In case of short-channel SNW MOSFET, the values of $C_{sdx}$ due to the DIBL effect are much larger than long-channel SNW MOSFET and JLSNW MOSFET.

Fig. 2. The extraction results of (a) $C_{sd}$ and (b) $C_{sdx}$ with different $V_{DS}$.

Fig. 3. Comparison of modeled (line) and 3-D simulated (symbol) $Y_{22}$-parameters. (a) $\text{Im}(Y_{22})$ of short-channel SNW, short-channel JLSNW, and long-channel SNW MOSFETs at $V_{GS} = V_{DS} = 1\, \text{V}$. (b) $\text{Im}(Y_{22})$ of short-channel SNW MOSFET as a function of frequency at different $V_{DS}$.

In order to check the accuracy of the RF model with $C_{sdx}$, the extracted $\text{Im}(Y_{22})$ by SPICE simulation with our RF model were compared with that by TCAD device simulation as a reference data (Fig. 3). As shown in Fig. 3 (a),
the model without $C_{sdx}$ failed to describe $\text{Im}(Y_{22})$ accurately only for the short-channel SNW MOSFET, while it keeps accurate with case of the model with $C_{sdx}$ in JLSNW and long-channel SNW MOSFET due to small DIBL effect. Figure 3 (b) shows $\text{Im}(Y_{22})$ of short-channel SNW MOSFET with $L_G=30\,\text{nm}$ according to different drain voltages. The effect of $C_{sdx}$ on $\text{Im}(Y_{22})$ at low drain voltage is negligible owing to small DIBL effect. As the drain voltage increases, however, the DIBL effect occurs remarkably, and the model with $C_{sdx}$ becomes much more accurate than that without $C_{sdx}$. Consequently, $\text{Im}(Y_{22})$ for short-channel device can be accurately modeled by adding $C_{sdx}$ to RF model.

4 Conclusion

The investigation of source-to-drain capacitance due to the DIBL effect was investigated for SNW and JLSNW based on the rigorous TCAD device simulation. The values of $C_{sd}$ of the short-channel SNW MOSFET were influenced remarkably by the DIBL effect. The JLSNW device and long-channel SNW MOSFET had the negative or zero $C_{sd}$, while the short-channel SNW MOSFET had the positive $C_{sd}$ for high drain voltages. By the addition of $C_{sdx}$, $\text{Im}(Y_{22})$ was accurately modeled.

Acknowledgments

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2010-0006270).