IEICE Electronics Express, Vol.8, No.20, 1730–1735

A low-power/high-resolution dual-mode analog-to-digital converter for wireless sensor applications

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Abstract: A successive approximation register (SAR) analog-to-digital converter (ADC) with an integrating resolution booster (IRB) is proposed and experimentally verified to provide the capability of dual-mode operation, that is, low-power and high-resolution modes. This dual-mode architecture corresponds to a kind of hybrid ADC architecture, combining a low-power SAR ADC and a high-resolution integrating-type ADC together. A prototype ADC design is fabricated in a 0.18 μm CMOS process, and its dual-mode operation is experimentally verified. The total power consumption in the low-power mode was only 8 μW with the resolution of 6 bits, and the high-resolution mode achieved an additional resolution of 4 bits by activating the IRB, consuming the instant power of 380 μW.

Keywords: integrating resolution booster, successive approximation register, dual-mode architecture, wireless sensor

Classification: Wireless circuits and devices

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DOI: 10.1587/elex.8.1730
Received August 22, 2011
Accepted September 16, 2011
Published October 25, 2011

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1 Introduction

Recent wireless sensor nodes and mobile devices need to minimize their power consumption during normal monitoring period and allow further power only when communications or accurate measurements are required. This technology trend would necessitate an adaptive analog-to-digital converter (ADC) to be capable of changing its power consumption and bit resolution according to its operating status. Recent ADCs for wireless sensor applications are adopting the successive approximation register (SAR) architecture to achieve the low-power performance [1, 2]. Since the SAR ADC requires only one comparator and other digital logics, low-power characteristic is inherently obtained. However, when higher bit resolution is required, other power-consuming architectures such as pipeline and delta-sigma ADCs should be used [3, 4]. Recently many researches have tried to reduce the power of these high-resolution ADCs, but it is still not easy to achieve the μW-level power. Therefore, a kind of dual-mode architecture is proposed to control its power consumption adaptively. During the monitoring status, it minimizes its power consumption with reasonable bit resolution, and it enhances its resolution performance only when more accurate measurement is required, thereby optimizing its overall power consumption properly.

2 Dual-mode architecture

The proposed dual-mode ADC supports two operation modes of low power and high resolution. Fig. 1 (a) shows the proposed architecture which is mainly composed of a SAR ADC, an integrating resolution booster (IRB), and an output combiner. The low-power mode is provided only by the SAR ADC and the output combiner, and the high-resolution mode activates the IRB block additionally. Capacitive digital-to-analog converters (C-DAC), one comparator, and their control logic comprise the SAR ADC. Fig. 1 (b) shows the overall ADC operation concept and its simplified output waveforms of the SAR C-DAC and the IRB integrator. The SAR operation is like conventional differential SAR ADCs [5].

In the first cycle, it samples its differential input voltages, and then it performs analog-to-digital conversions for the remaining period whose number

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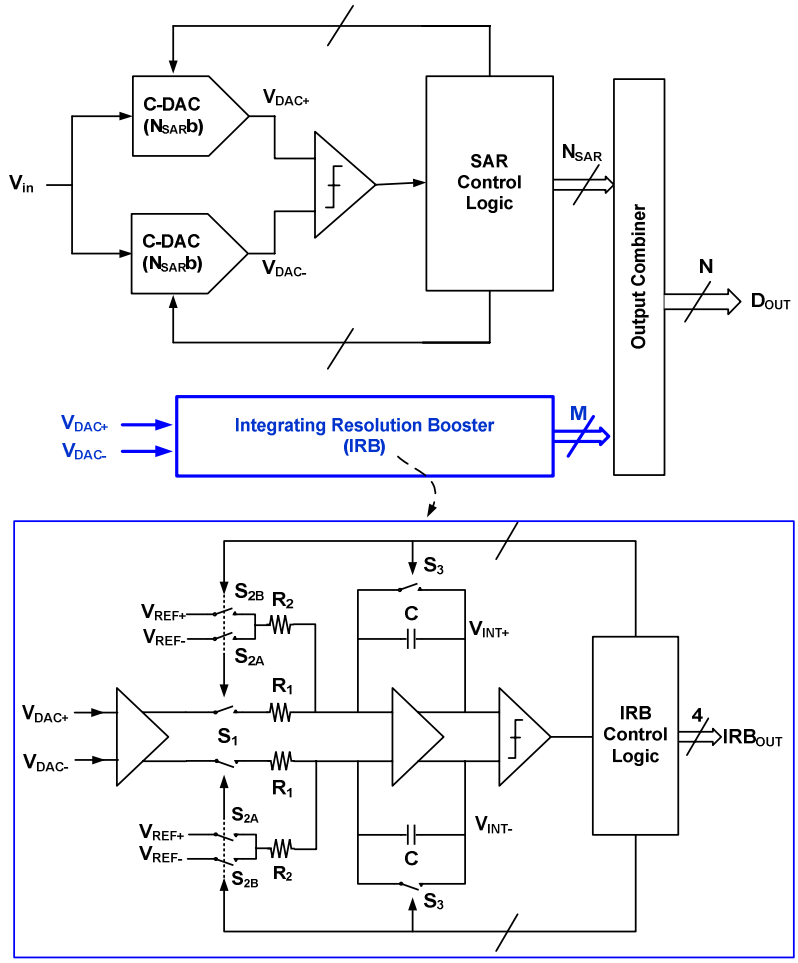
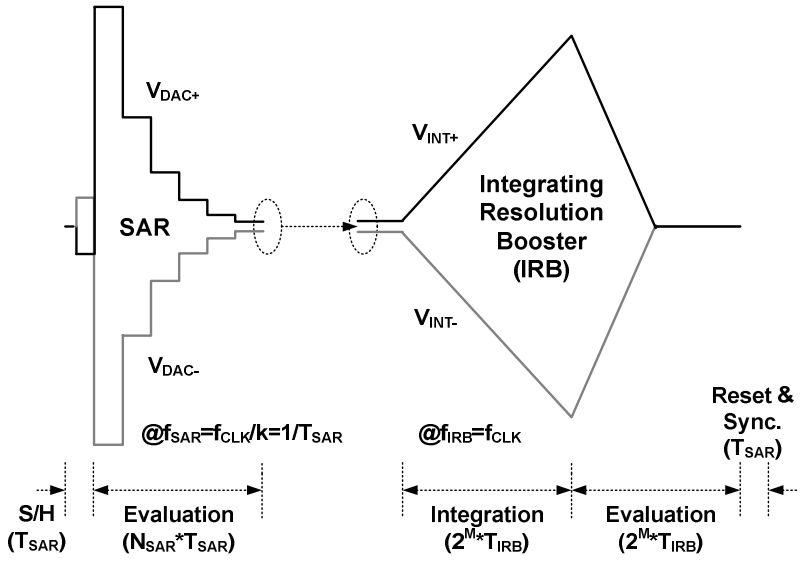


(a)



(b)

Fig. 1. (a) Simplified schematic of Proposed dual-mode ADC. (b) its overall operational waveforms in case of hi-resolution mode.

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Received August 22, 2011
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of cycles is equal to N_{SAR}, the number of SAR resolution bits. Since the high-resolution mode should provide additional resolution bits, the IRB should be implemented to have better resolution capability. Among various ADC types, integrating ADCs are known to have good resolution performance only with a few circuits, and so their concept is adopted into the proposed IRB. As in Fig. 1 (b), the IRB starts right after the SAR conversion cycle is finished, and final outputs of a differential C-DAC are taken as IRB inputs. For first M cycles, it integrates differentially with a slope proportional to the input, and then it starts discharging with a fixed slope. When the discharge ends, its internal M-bit counter status is latched as the IRB output. Since the discharge time varies depending on its input value, the IRB evaluation period is designed to be the same as the integration time, making overall conversion rate consistent. Finally, the output combiner converts the IRB output of M bits into the corresponding voltage information and generates the overall ADC output (D_{OUT}) by combining with the SAR output of N bits

3 Integrating resolution booster

The IRB circuit is the most critical block in the dual-mode ADC architecture in that it is responsible for additional resolution bits below the LSB (least significant bit) of the SAR ADC. It is comprised of an input buffer, an R-C integrator, a comparator and their control logic with M-bit counter. Fig. 1 (a) includes the simplified schematic of the IRB, where every significant signal paths are differentially implemented for better noise immunity and bit-resolution capability, and all components are turned off during the low-power mode. The IRB operation details are as follows. First, if the switch S1 is turned on, the IRB capacitor C is charged for 2M cycles with the current proportional to the difference between the C-DAC output (V_{DAC+}/V_{DAC-}) and the common-mode voltage (V_{COM}). The charge current is given by $(V_{DAC} - V_{COM})/R_1$. Then, by turning S_1 off and S_{2A}/S_{2B} on, the evaluation period begins. The IRB control logic measures the discharge time of the integrator which would be converted into the voltage information in the output combiner. The discharge current is given by $(V_{REF} - V_{COM})/R_2$.

4 Measured results

A prototype ADC to verify the feasibility of the proposed dual-mode architecture is fabricated in a 0.18 μm standard CMOS process. The resolution of the SAR ADC is designed as 6 bits. The IRB clock is made 8 times faster than the SAR clock ($k = 8$) to minimize its speed degradation, and its voltage references (V_{REF+}/V_{REF-}) are tied onto supply voltage and ground to support rail-to-rail operation. Fig. 2 (a) shows a chip photograph of the prototype circuit. The total area is 1.0 mm^2, and the core areas of the SAR ADC and the IRB are 0.16 mm^2 and 0.13 mm^2 respectively. The additional resolution of 4 bits was achieved, only allowing 0.8 times area increment. With 1.8 V power supply and external clock of 10 MHz/8, the low-power mode operation provided 178.6 kS/s sampling rate and ultra-low power consumption of 8 μW.

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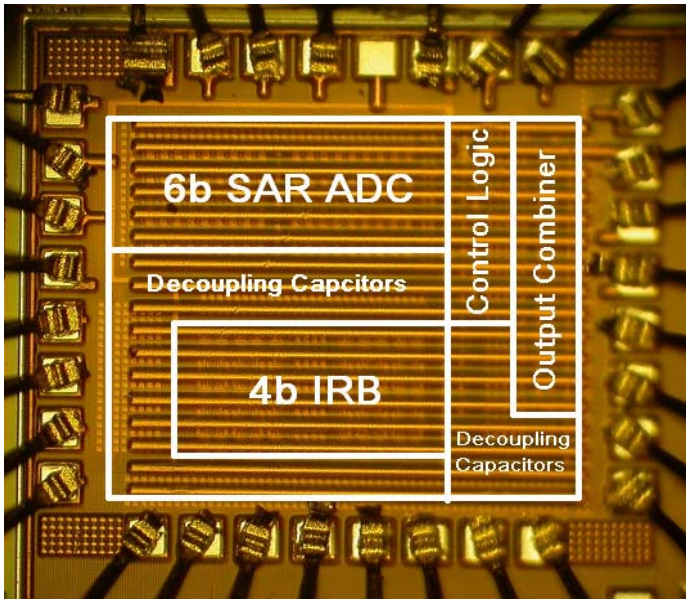
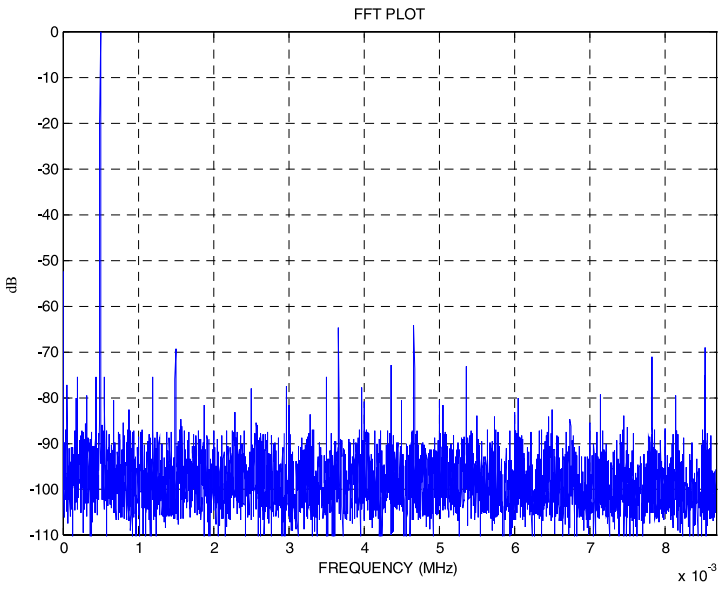


(a)



(b)

Fig. 2. (a) Chip photograph of a dual-mode ADC prototype. (b) Measured FFT spectrum @ f_{in} = 0.5 kHz, f_s = 17.4 kHz.

In the high-resolution mode, the sample rate is 17.4 kS/s and the power was 0.4 mW. Fig. 2 (b) shows the FFT (fast Fourier transform) spectrum plots for 10b final ADC outputs. The 10-bit final ADC which is obtained after combining with 4b IRB outputs, provided 8.9 ENOB (effective number of bits), peak DNL (differential non-linearity) of 0.5 LSB, peak INL (integral non-linearity) of 0.8 LSB. Measured results are summarized in Table I.

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Table I. Measured Performance Summary.

Operation Mode	Low power	Hi resolution
Power Dissipation @ 1.8V supply	8 mW	380 mW
Resolution	6 bit	10 bit
Sampling rate @ 10MHz/8 clock	178.6 kS/s	17.4 kS/s
DNL	+/- 0.1 LSB	+/- 0.5 LSB
INL	+/- 0.2 LSB	+/- 0.8 LSB
ENOB	5.9 bit	8.9 bit
SINAD	37.0 dB	55.5 dB
SFDR	46.2 dBc	65.1 dBc
Input range	Rail-to-rail	
Standby Power	9 nW	
Chip area	1 mm^2	
Process	0.18mm 1P5M CMOS Process	

5 Conclusion

A dual-mode ADC architecture and a resolution booster concept were proposed and experimentally verified through a prototype design to have controllability on its power consumption and bit resolution. In a low-power mode, ultra-low power characteristic of 8 μW was achieved by operating a SAR ADC only. In a high-resolution mode, an integrating resolution booster with power of 0.4 mW provided the bit-resolution enhancement of 4 bits.

Acknowledgements

This work was supported by the year of 2011 Research Fund of the UNIST (Ulsan National Institute of Science and Technology).

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