IEICE Electronics Express, Vol.8, No.21, 1783–1788

Diffusion-rounded CMOS for improving both I_{on} and I_{off} characteristics

Myunghwan Ryu, Hung Viet Nguyen, and Youngmin Kim[a)]
School of Electrical and Computer Engineering, UNIST (Ulsan National Institute of Science and Technology), Ulsan, 689–798, Republic of Korea
a) *youngmin@unist.ac.kr*

Abstract: This paper presents a simple and optimized device layout developed by using diffusion rounding effect for better electrical behavior of transistors. TCAD analysis shows that diffusion rounding at the transistor source side can provide increased I_{on} with decreased I_{off} because of the edge effect. The proposed diffusion-rounded CMOS shows as much as 10% improvement in the on-current (driving) and the off-current (leakage) is saved up to 10%. The inverter layout shows that proposed method requires less than a 4% cell area increase for the same driving strength of original cells.

Keywords: diffusion rounding, CMOS, variation, I_{on}, I_{off}, optimization
Classification: Integrated circuits

References

[1] ITRS 2010 [Online] http://www.itrs.net/Links/2010ITRS/Home2010.htm.
[2] P. Gupta, A. B. Kahng, Y. Kim, S. Shah, and D. Sylvester, "Investigation of diffusion rounding for post-lithography analysis," *Design Automation Conference, ASPDAC 2008*, pp. 480–485, 21-24 March 2008.
[3] Y. Ban, S. Sundareswaran, R. Panda, and D. Z. Pan, "Electrical Impact of Line-Edge Roughness on Sub-45nm Node Standard Cell," *SPIE*, vol. 7225, 2009.
[4] T.-B. Chan and P. Gupta, "On Electrical Modeling of Imperfect Diffusion Patterning," *VLSI Design, 2010. VLSID '10. 23rd International Conference on*, pp. 224–229, 3-7 Jan. 2010.
[5] R. Singal, A. Balijepalli, A. Subramaniam, F. Liu, S. Nassif, and Y. Cao, "Modeling and analysis of non-rectangular gate for post-lithography circuit simulation," *Design Automation Conference*, pp. 823–828, 2007.
[6] Cadence GPDK45nm PDK, [Online] http://www.cadence.com
[7] Synopsys Sentaurus TCAD, [Online] http://www.synopsys.com
[8] PTM 45nm bulk CMOS model, [Online] http://ptm.asu.edu
[9] Mentor graphics Calibre Workbench, [Online] http://www.mentor.com

DOI: 10.1587/elex.8.1783
Received September 08, 2011
Accepted September 27, 2011
Published November 10, 2011

1 Introduction

As semiconductor industries move to aggressive scaling to reduce the area and dynamic power consumption, the channel length has become as short as a few nanometers [1]. Thus imperfect patterning becomes significant not only in the poly gate channel shape but also in the diffusion profile. Many researches have been conducted to model and analyze the transistors' profile in terms of driving current (I_{on}) and leakage current (I_{off}) for post-lithographic simulations [2, 3, 4, 5]. In this paper, we propose a novel layout approach to achieve a better driving capability and better leakage property by using imperfect diffusion rounding patterning. TCAD simulations and analysis have shown that I_{on} and I_{off} characteristics behave differently depending on whether diffusion rounding occurs at the source side or at the drain side of the transistor. Both I_{on} and I_{off} properties become positive when the diffusion rounding happens at the source side. Therefore, the optimized layout for simultaneous device performance is boosted, and leakage power saving is made possible. In this paper, we propose a diffusion-rounded CMOS layout to exploit this positive effect of diffusion rounding at the transistor source side. The paper is organized as follows; Section 2 explains electrical properties of diffusion rounding effect in detail, Section 3 investigates the proposed diffusion-rounded CMOS in delay and standby power. Section 4 analyzes several logic families to validate how much benefit we can achieve by employing the proposed diffusion-rounded CMOS. In Section 5, the layout issue of the proposed method is presented, and conclusions are drawn in the final section.

2 Diffusion rounding effect

A few attempts have been made to model the impact of diffusion rounding in the MOSFET. In [2] the authors proposed a simple model to capture the electrical effects by diffusion rounding in the NMOS and PMOS. It used effective width change by diffusion rounding for I_{on} and effective channel length change for I_{off}. Another work [4] proposed an analytical approach to calculate effective V_{th}, channel length and device width by diffusion rounding. Both papers indicated that diffusion rounding has different effects on the transistors' electrical characteristics depending on the location of the rounding (either source side or drain side). To quantify the benefit of diffusion rounding in the electrical characteristics of transistors, TCAD simulations of 45 nm bulk CMOS are conducted. The parameters of nominal devices are calibrated to match the 45 nm predictive models [7]. Table I lists the I_{on} and I_{off} comparison between nominal devices and diffusion-rounded devices. The source side diffusion rounding shows better property both in I_{on} and I_{off}. In other words, the driving current increases and the leakage current decreases at the same time when the source side diffusion shape rounded. Therefore, we can generate an optimized layout to achieve better I_{on}/I_{off} characteristics by shaping the rounding in the source side. In the conventional CMOS layout, the source side active area is connected to the power supply; VDD for

DOI: 10.1587/elex.8.1783
Received September 08, 2011
Accepted September 27, 2011
Published November 10, 2011

Table I. TCAD simulation results showing the effect of diffusion rounding.

	length (nm)		TCAD		Normalized	
NMOS	**source**	**drain**	**I_{on} (uA)**	**I_{off} (nA)**	**I_{on}**	**I_{off}**
rectangular	155	155	**161.73**	**72.56**	**1.00**	**1.00**
source +45nm	200	155	180.87	68.99	1.12	0.95
source +90nm	245	155	**199.15**	**65.57**	**1.23**	**0.90**
drain +45nm	155	200	175.80	77.61	1.09	1.07
drain +90nm	155	245	188.91	81.92	1.17	1.13
PMOS	**source**	**drain**	**I_{on} (uA)**	**I_{off} (nA)**	**I_{on}**	**I_{off}**
rectangular	300	300	**184.31**	**67.18**	**1.00**	**1.00**
source +45nm	345	300	194.40	63.85	1.05	0.95
source +90nm	390	300	**204.64**	**61.92**	**1.11**	**0.92**
drain +45nm	300	345	192.66	68.15	1.05	1.01
drain +90nm	300	390	201.18	70.77	1.09	1.05

PMOS and GND for NMOS. And the diffusion rounding size depends not only on the manufacturing process but also on the layout rules such as the gate channel line end extension (LEE) and distance between the gate poly and the active area bending. In the gpdk45 nm [6] layout, the design rule of the minimum distance from the poly edge to the diffusion is 50 nm. And the width of the active area (either source or drain) is 140 nm. Therefore, 90 nm width and 45 nm height bending shape to form diffusion rounding can be easily applied.

3 Electrical properties of diffusion-rounded MOSFET

To introduce diffusion rounding in the source side to improve both I_{on} and I_{off}, a 45 nm active area protrusion is chosen at both sides of the source area. The Sentaurus TCAD setup of NMOS/PMOS is calibrated to the SPICE I_{on}/I_{off} data in 45 nm BPTM [8]. After calibration, the diffusion-rounded NMOS and PMOS are generated by using analytical models which are proposed in [4]. We applied the models by changing width of the transistors for I_{on} and I_{off} to include the diffusion rounding effects.

Figure 2 shows the proposed layout for NMOS. As can be seen in Table I in Section 2, a 45 nm diffusion rounding at the source side can increase 10% of driving current (I_{on}), saving up to 10% leakage current (I_{off}).

These observations led us to conclude that having diffusion rounding at the source side improves both I_{on} and I_{off} characteristics of the transistors. The effective channel width for the diffusion-rounded device is longer than that of the original device. Therefore, the driving current of the diffusion-rounded transistors is greater than that of the original, non-diffusion-rounded transistors [2, 4]. The V_{th} of the device is not uniform along the channel width, but the V_{th} at the edge of the device is much smaller than that at the center [2]. The effective channel length at the edge of the device is longer for a diffusion-rounded device than that of the original device without diffusion rounding. Therefore, the diffusion-rounded CMOS shows less I_{off} than the original nominal devices. E-field and current density analysis of TCAD also

DOI: 10.1587/elex.8.1783
Received September 08, 2011
Accepted September 27, 2011
Published November 10, 2011

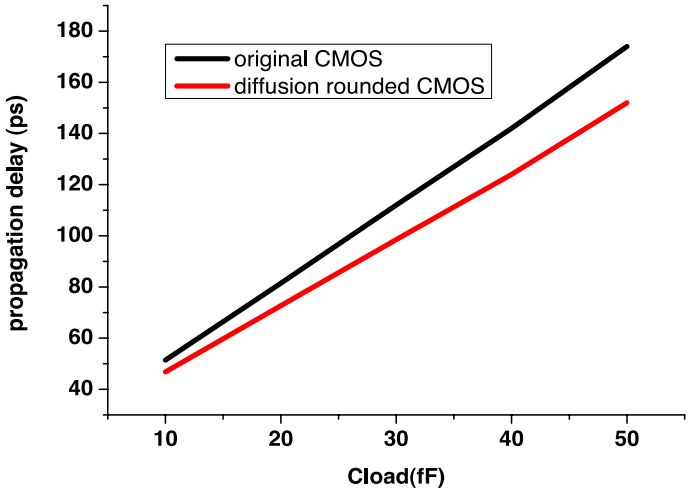

Fig. 1. Propagation delay improvement with diffusion rounded CMOS.

indicate reduced I_{off} and increased I_{on} when we form rounding shape at the source side of the transistors. So we can conclude that source side diffusion rounding provides higher driving current due the effective channel increment at the same time lower leakage current due to the reduced edge effect and e-field.

4 Simulations results

Using the analytical diffusion rounding models proposed in [4], we generate the diffusion-rounded NMOS and PMOS by changing effective V_{th}, effective width, and channel length. And hspice simulations are conducted for several CMOS logic gates such as the inverter, NAND2, and NOR2 to measure the benefits of diffusion rounding. To investigate circuit level implication of diffusion rounding benefits, the 101 stage ring oscillators and FO4 delay metrics are used. Figure 1 shows the inverter propagation delay result of original CMOS and diffusion-rounded CMOS. The diffusion-rounded CMOS inverter represents up to 13% speed up greater than the original CMOS inverter with 50 fF load capacitance. Power simulation shows that the leakage power of the original CMOS is 142 nW and that of the diffusion-rounded CMOS is 127 nW, which is nearly 10% smaller than the original CMOS inverter leakage power.

5 Layout perspective

To form diffusion-rounded transistors for PMOS and NMOS, the active area layout and thus mask design are modified and the overall cell layout is increased to meet the design rules. Several gate layouts (i.e., INV, NAND2, NOR2) are generated and compared to assess the layout tradeoff by improving electrical property in diffusion-rounded CMOS. The cadence generic 45 nm design package and the layout rules are used for the layouts [6]. Figure 2 shows the inverter layout comparison between the original and the diffusion-rounded CMOS. (a) shows the original layout of conventional CMOS

DOI: 10.1587/elex.8.1783
Received September 08, 2011
Accepted September 27, 2011
Published November 10, 2011

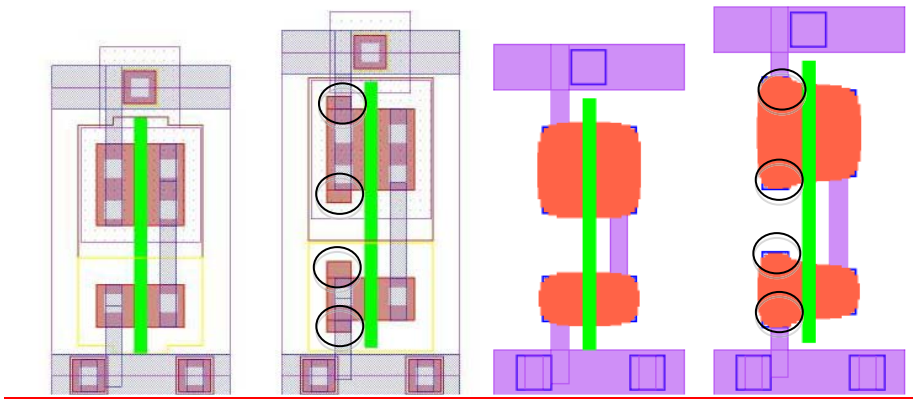

Fig. 2. Inverter layouts of both original and diffusion-rounded CMOS; (a) shows layouts and (b) shows the printed image with OPC. Note, black circles indicated the source side bending shape to form diffusion rounding.

and the proposed diffusion rounded one and (b) represents the printed images with OPC in Calibre Workbench [9] simulations. We used the minimum space for all the layers in the GPDK45 nm design rule [6]. The minimum distance between the poly edge and the diffusion is 50 nm. The 90 nm width and 45 nm height bending shape is inserted to form the rounding at the source side diffusion. As shown in Figure 2-(b), the rounding shape at the source side appears with the 193 nm wavelength optical lithography. The cell height increases from 1.07 μm to 1.19 μm, which is about 11% in the diffusion-rounded CMOS layout, but we have a better driving strength in the diffusion-rounded CMOS. Therefore, we can match the same driving strength by using a smaller channel width in the diffusion-rounded CMOS gates. For the same driving strength, the diffusion-rounded CMOS cell height increases only 50 nm that results in less than a 4% cell area increase compared to the conventional CMOS. In addition, as the gate width increases and the logic gates become complicated, the area penalty to form the diffusion rounding shape in the source sides will be minimal. As the minimum feature size of the chip becomes small, the cost for mask generation increases to apply intensive RET techniques including OPC. Thus the complexity and controllability of the proposed design layout might be worse. However, we can apply the proposed diffusion-rounded logics in minimal area where we require either faster transistors to improve overall speed and/or less leaky gates to reduce standby power for specific blocks.

6 Conclusion

In this paper, we propose a simple layout method to boost the driving strength of logic gates and also to save the leakage power with a minimal area overhead. The proposed method provides up to 13% speed up and also saves up to 10% leakage current in an inverter simulation by exploiting the

DOI: 10.1587/elex.8.1783
Received September 08, 2011
Accepted September 27, 2011
Published November 10, 2011

diffusion rounding phenomena in the transistors. The layout of the diffusion-rounded CMOS shows a minimal impact in the cell area compared to the original compact layout. To verify the feasibility and benefit of the diffusion rounding effect on the real wafer, further research and simulations are necessary on the layouts of transistors with different diffusion rounding size and locations.

Acknowledgments

This work was supported by the 2009 Research Fund of the UNIST (Ulsan National Institute of Science and Technology). This work also was partially sponsored by NRF grant #2010-0012867. EDA tools were partially supported by IDEC at KAIST.

DOI: 10.1587/elex.8.1783
Received September 08, 2011
Accepted September 27, 2011
Published November 10, 2011