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An Optimized Device Structure with Improved Erase Operation within the Indium Gallium Zinc Oxide Channel in Three-Dimensional NAND Flash Applications

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Abstract: In this paper, we propose an optimized device structure to address issues in 3D NAND flash memory devices, which encounter difficulties when using the hole erase method due to the unfavorable hole characteristics of indium gallium zinc oxide (IGZO). The proposed structure mitigated the erase operation problem caused by the low hole mobility of IGZO by introducing a filler inside the IGZO channel. It facilitated the injection of holes into the IGZO channel through the filler, while the existing P-type doped polysilicon filler material was replaced by a P-type oxide semiconductor. In contrast to polysilicon (band gap: 1.1 eV), this P-type oxide semiconductor has a band gap similar to that of the IGZO channel (2.5 to 3.0 eV). Consequently, it was confirmed through device simulation that there was no barrier due to the difference in band gaps, enabling the seamless supply of holes to the IGZO channel. Based on these results, we conducted a simulation to determine the optimal parameters for the P-type oxide semiconductor to be used as a filler, demonstrating improved erase operation when the P-type carrier density was 10^{19} cm^{-3} or higher and the band gap was 3.0 eV or higher.

Keywords: 3D NAND; polysilicon; IGZO; erase operation; Cell-On-Peri (COP)

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1. Introduction

Since the initial introduction of the 3D NAND flash structure in 2007 [1], many memory companies have launched their products, contributing to the growth of a vast memory market that is gradually replacing traditional hard disks [2,3]. The vertical stacking structure, a key advantage of the 3D NAND flash memory, is recognized for its significant reduction in manufacturing costs. Unlike 3D structures in logic semiconductors or other product groups, the vertical stacking structure does not require a lithography process, which is the primary cost factor when increasing the number of stacks. As of 2023, owing to this advantage, the number of stacked stages in this structure has already exceeded 256, making it feasible to achieve an increase in the number of stacks to the range of 300 to 500 steps in the near future [4].

Nevertheless, the 3D NAND flash structure has encountered various issues, including electrical problems such as threshold voltage instability and operating current instability due to temperature change, as well as mechanical issues such as silicon substrate bending caused by differences in the stress properties between different materials during the technology development process. Although advancements in process technology have mitigated

these issues, there is an anticipation that such progress may reach its limits sooner or later. To improve the efficiency of data processing, various components, such as memristors, which have realized the integration of memory and computing, have been studied in the field of memory technologies [5–7]. While various issues have emerged in the evolution of highly integrated 3D NAND flash structures, there is a strong demand to specifically focus on channel-related issues. As is widely known, crystallized silicon channels cannot be utilized in 3D NAND flash structures due to process limitations, leading to the adoption of polycrystalline silicon channels. However, a number of electrical problems have been reported in these polysilicon channels due to the presence of grain boundaries within the numerous amorphous structures and the traps found in the channels [8,9].

Typical issues include the distribution of the threshold voltages of each flash memory cell based on trap distribution, changes in operating current with temperature changes, and, significantly, very low electron mobility. Consequently, studies on alternative material channels that can replace polysilicon channels, identified as the root causes of these issues, have been conducted. Furthermore, materials such as gallium nitride (GaN) and silicon germanium (SiGe) have been considered as potential candidates. However, it was found that all of these materials exhibited issues in mobility and stability, ultimately leading to the conclusion that polysilicon channels could not be effectively substituted.

Indium gallium zinc oxide (IGZO) exhibits stability, making it suitable for widespread adoption in display materials, distinguishing it from other channel materials. In particular, IGZO presents several advantages, including low leakage current and high mobility, particularly within amorphous structures [10,11]. Moreover, IGZO can form a self-aligning structure known as the C-AXIS crystal structure [12–15], offering the potential to fundamentally address the issue of the polycrystalline state in existing polysilicon channels.

In contrast, IGZO has several disadvantages, as follows. It exhibits higher contact resistance compared to other semiconductor materials, and there are instability issues in TFT operation due to defects in both the IGZO bulk and the IGZO/dielectric interface. While several studies have been conducted to resolve these issues [12–17], applying IGZO to 3D NAND flash memory structures presents significant hurdles due to its very large hole effective mass and very slow hole mobility, which are the fundamental properties of N-type oxide semiconductors. These unfavorable hole-related material properties make it unsuitable for hole erasing methods like 'bulk erase' and 'GIDL erase', commonly employed in 3D NAND flash memory structures. Consequently, despite its excellent material properties, IGZO is not considered suitable for use as a channel in 3D NAND flash structures [18,19].

To address the erase operation issue in the 3D NAND flash structure applying these IGZO channels, we propose an IGZO filler structure by changing the 'Filler' located inside the channel from the existing silicon oxide to P-type polysilicon, enabling the delivery of holes to the IGZO channel through this filler structure [20]. The core idea behind this structure is based on the assumption that, given that the thickness of the IGZO channel is as thin as 10 nm or less, the transfer and movement of holes would be feasible if the holes were supplied from a P-type polysilicon filler already abundant in holes despite the low hole mobility of IGZO.

Based on this assumption, the initial simulation results indicated that the proposed IGZO filler structure can perform very rapid erasing operations not only as a source for supplying holes, but also as a conduit through which electrons emitted from the silicon nitride layer, an electron storage layer, can be quickly discharged during the erasing operation. However, through further research using realistic parameters and models, we identified fundamental limitations when using polysilicon fillers. Specifically, a significant disparity exists between the band gaps of polysilicon and IGZO, resulting in a substantial barrier on the contact surface between the two materials. This barrier essentially stems from the fundamental material properties of polysilicon and IGZO, leading to the prediction that the erase operation will face considerable challenges, especially under ideal process conditions (assuming the formation of a highly ideal interface) [20].

Therefore, as a novel solution to this issue, this paper proposes a structure using P-type oxide semiconductors as the material for a filler structure. P-type oxide semiconductors, such as 'Tin oxide' (SnO) and 'Copper Oxide' (Cu_2O), initially received much less attention in early studies compared to N-type oxide semiconductors due to their very low mobility and thermal stability. However, recent studies on these materials have revealed numerous cases of achieving high carrier density, mobility, and thermal stability [21,22].

In particular, as the band gap of this P-type oxide semiconductor is almost similar to that of IGZO, the barrier issue observed in the polysilicon filler will not occur fundamentally. Thus, as long as it remains reasonably stable, it can be considered the most ideal type of structure. Therefore, this paper aims to verify and analyze the erasing performance of the 3D NAND flash structure when applied with the IGZO channel, drawing insights from the latest research results on P-type oxide semiconductors.

2. Details of the Proposed Structures

Figure 1a shows the proposed structure with the filler material of a P-type metal ox-ide semiconductor, which transfers holes through channels. Figure 1b,c depict the distribution of energy bands when different filler materials of polysilicon and SnO are used, respectively. Figure 1b shows a large energy barrier of approximately 2.1 eV formed at the interface between the polysilicon (band gap: 1.1 eV) used for the filler material and the IGZO (band gap: 3.1 eV) used for the channel material, indicating difficulties in transferring holes generated from other materials to the oxide semiconductor channels.

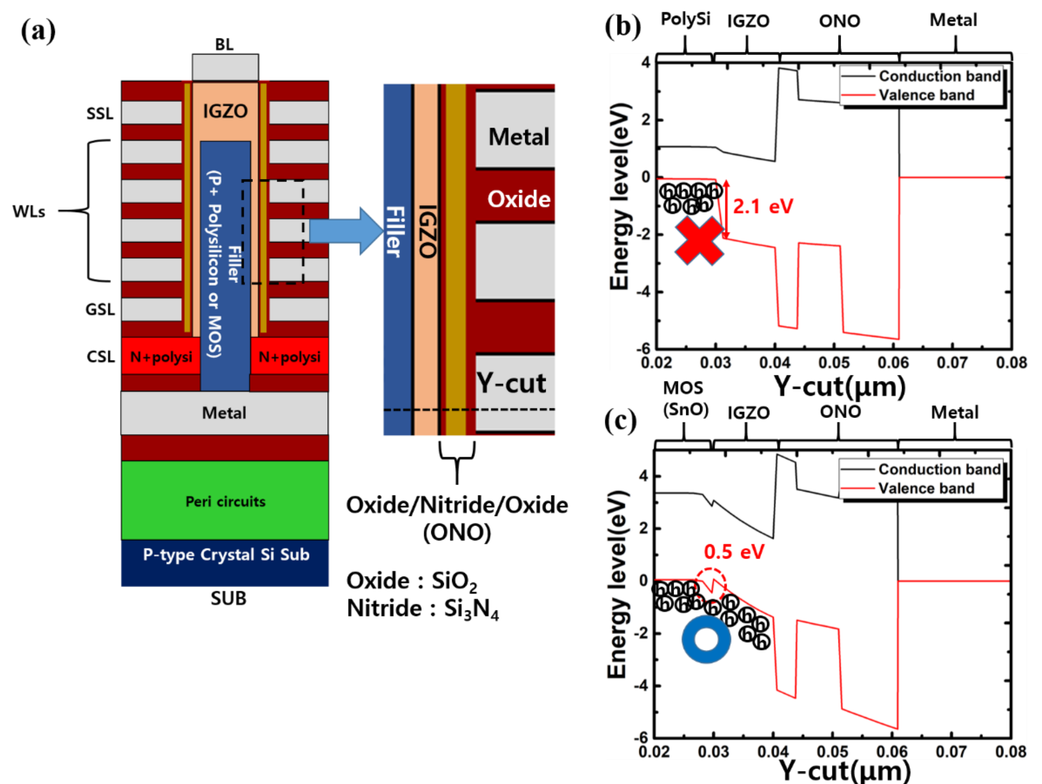

Figure 1. Comparison of proposed structures: (**a**) shows the schematic structure of the proposed structure, and (**b**,**c**) show the difference in energy band level and corresponding barrier size depending on the material of the filler structure.

To address this problem, the only viable solution is to create a strong electrical field surpassing the barrier formed, achieved by employing a voltage much higher than that used in the erase operation (~20 V) in the current 3D NAND flash memory. However, the use of high voltage basically implies the utilization of a very high electric field, posing the risk of damaging the IGZO in the structural and operational aspect when subjected to the

application of such a high electric field. It becomes evident that the accumulation of such damage will adversely affect the reliability of the structure.

Therefore, the proposed structure aims to address this issue at its core by incorporating P-type oxide semiconductors for filler structures. As depicted in Figure 1c, when tin oxide (SnO) is used for the filler material, its band gap of 3.5 eV is only slightly different from that of IGZO (3.1 eV). Consequently, the barrier at the interface between the two sub-stances is almost absent, except for a 0.5 eV Schottky barrier resulting from the slightly higher band gap of tin oxide. As a result, holes within this filler structure can readily move to the IGZO channel. Simultaneously, given that the thickness of the channel is less than 10 nm, hole delivery remains viable despite the relatively low hole mobility of IGZO, thereby enabling the erase operation. For the successful establishment of this structure, it is essential to assume that the process stability and channel characteristics of the P-type oxide semiconductor must reach an operational level. The P-type oxide semiconductor, as previously reported in [20], showed much poorer performance and reliability compared to N-type oxide semiconductors. Consequently, P-type oxide semiconductors are not widely utilized in semiconductor devices such as those associated with logic and memory.

Considering the aforementioned assumptions, we recently conducted research on P-type oxide semiconductor materials and obtained meaningful results regarding thermal stability and material properties, presenting the proper erase operation characteristics of the proposed structure, verified through the TCAD device simulation [23]. In particular, among the P-type oxide semiconductor research findings, the outcomes of applying parameters reflecting material characteristics specialized for mobility, bandgap, and carrier density were confirmed.

3. Simulation Results and Discussion

3.1. Simulated Structures, Models, and Parameters

Figure 2 shows the detailed device structure employed in the simulation, configured as a virtual Gate-All-Around (GAA) structure during the device simulation. The implemented structure, which is represented by only half of Figure 2a, is employed to evaluate the operation of the fully vertical channel 3D NAND string. In addition, each contact is composed as follows. First, the bottom SUB contact controls the operation of the connected 'Filler', while the Common-Source-Line (CSL) contact serves as the source for the entire channel. The Ground-Select-Line (GSL) located on it is responsible for controlling the contact between the CSL and the channel, with the 10 word lines (WLs) present on it functioning as gates. Additionally, the Source-Select-Line (SSL) contact controls the contact between the BL and the channel at the top, and, finally, the upper bit line (BL) acts as the drain. In the enlarged Figure 2b near the SSL, we rounded and treated the edge part to prevent the unintended generation of a high electric field. While this structure is slightly different from the actual 3D NAND flash structure, a sharp edge in this region can lead to the generation of a high electric field, potentially allowing the movement of holes. To prevent such unintended movements, we made these adjustments to fundamentally block them.

Figure 2c shows an enlarged view of the device employed in the simulation, including the element dimensions. The thickness of the IGZO channel was set at 10 nm, which has been commonly used in 3D NAND flash structures utilizing polysilicon channels [1–4]. The thicknesses of the oxide, nitride, and block oxide layer in the tunnel were set at 4, 7, and 11 nm, respectively. A P-type oxide semiconductor, such as Cu_2O or SnO, served as the filler material and occupied all available space, in contrast to the previous filler of polysilicon. In contrast to previous studies that required the stabilization of polysilicon fillers with the use of macaroni oxide due to unstable material properties [21], the proposed structure utilizes oxide semiconductors known for high stability and excellent performance in both the channel [12–15] and filler [21,22]. In this work, to isolate the factors influencing the erase operation performance to the material properties of IGZO channels and the filler

structure, the proposed 3D NAND flash structure was designed to exclude macaroni oxide, filling all remaining space with fillers.

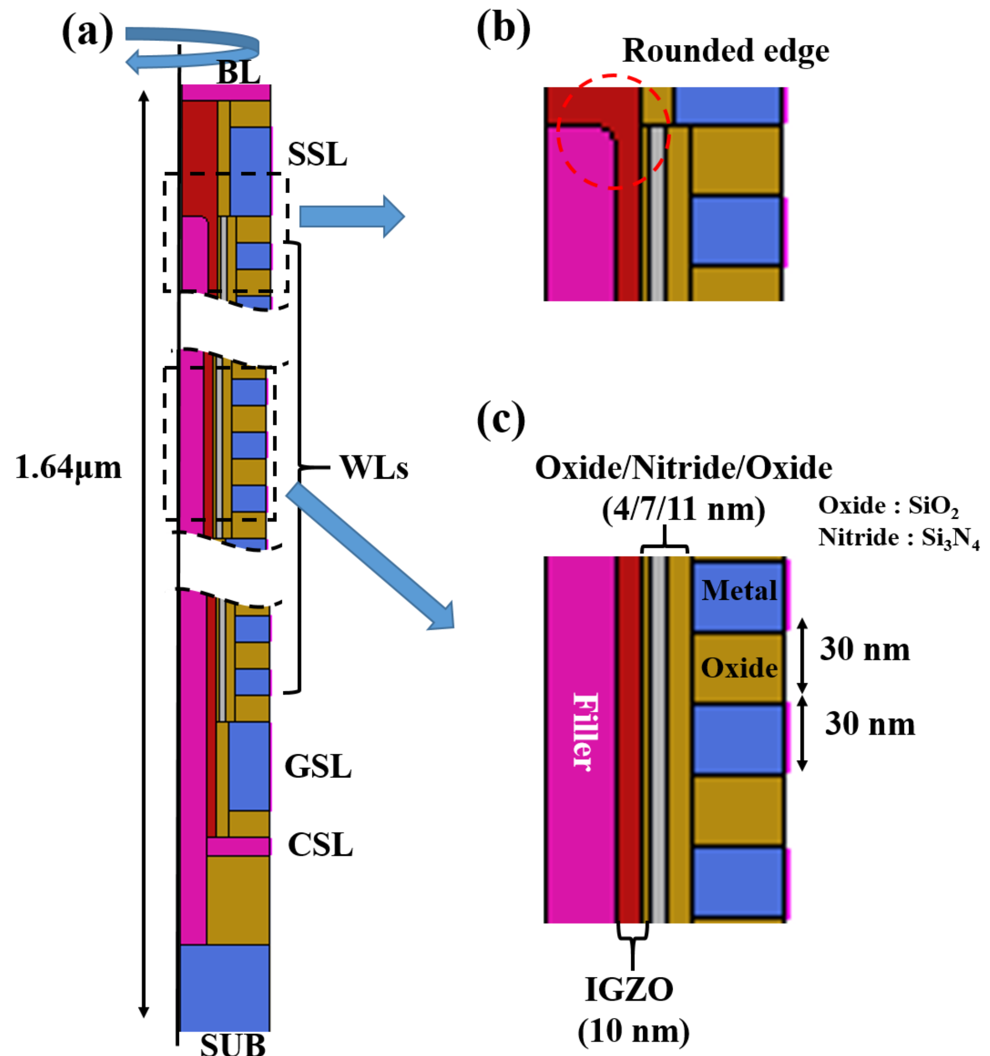

Figure 2. Details of the simulated device. (**a**) Schematic of the 10 stacked memory cells, word lines WL0 to WL9, and select transistors, GSL, SSL, BL, and CSL; (**b**) shows a rounded edge structure to block unnecessary high electric field generation; (**c**) expanded view of the simulated structure with dimensions of the constituent parts.

In the SSL region, the length of the SSL gate was set to 100 nm, which was also applied to the GSL. This was configured to suppress the leakage current flowing to the BL and CSL, and to enhance the gate control capability. Such a structure, or a plurality of gates, is known to be used in the actual 3D NAND structure. Finally, the CSL and BL were polysilicon contacts, with a doping concentration set at 10^{20} cm^{-3}.

Given that material parameters, including the doping concentration of the filler, play a crucial role in this work, a detailed discussion of identifying the best combination under various conditions will follow later. Table 1 lists the trap parameters of the materials applied to the polysilicon and silicon nitride, and Table 2 presents the applied voltage for each operation.

Table 1. Trap parameters of each material.

Parameters	Value		
	Polysilicon [20]	**Si_3N_4 [20]**	**IGZO [20]**
Trap concentration (cm^{-3}) (electro, hole trap)	1×10^{21}	5×10^{19}	1×10^{20}
Energy level (eV)	0.1 (electron) −0.1 (hole)	2.5 (electron) −1.0 (hole)	0.1 (electron) −0.1 (hole)

Table 2. Applied voltage for each operation.

Operation	Value				
	Target (WL8)	**Non-Targets (Other WLS)**	**SUB**	**CSL**	**BL**
Program	20 V	9 V	0 V	0 V	0 V
Erase	0 V	0 V	20 V	20 V	20 V
Read	−5~8 V	5 V	0 V	0 V	1 V

3.2. Simulation Results and Analysis of Fillers' Material Changes

Table 3 shows representative material parameters for the three filler materials used in this work. Two types of P-type oxide semiconductors with high band gaps (2.5 eV or higher) were used as filler materials, including tin oxide (SnO) with a very high carrier density and relatively low mobility, and copper oxide (Cu_2O) with a low carrier density and mobility five times higher than that of SnO.

Table 3. Parameters of each material.

Parameters	Value		
	Polysilicon [20]	**Cu_2O [21]**	**SnO [22]**
P-type carrier density (cm^{-3})	5×10^{18}	1×10^{15}	4×10^{19}
Bandgap (eV)	1.1	2.5	3.5
Mobility (cm^2/V.s)	100	50.1	10.1

By using two types of P-type oxide semiconductors with opposing properties in the filler structure and conducting a comparative analysis of the erase operation through simulation, we aim to identify which material properties used in the filler structure play a crucial role in enhancing the erase operation. The annealing temperatures were reported as 420 °C for Cu_2O and 600 °C for SnO [19,20]. Considering that both of these values exceed the annealing temperature of the existing P-type oxide semiconductor, it is inferred that the thermal stability of these materials is ensured within this temperature range.

Figure 3a shows the threshold voltage (V_{th}) change during the erase operation using various filler materials such as polysilicon, Cu_2O, and SnO. In the case of polysilicon fillers, some degree of the erase operation is observed. However, this outcome is not a result of hole injection into the IGZO channel; rather, it is the result of electrons being pulled out of the electron storage layer solely due to the high voltage generated by the filler. Naturally, during this operation, IGZO, lacking holes for the filler voltage transmission, experiences an excessively high electric field, potentially causing significant damage to the material itself [24]. In the case of Cu_2O fillers, a limited degree of the erase operation is observed, considered to be attributed to the insufficient hole supply, given the very small P-type carrier density of Cu_2O at 10^{15} cm^{-3}. Finally, in the case of SnO with a much higher

P-type carrier density, a remarkably excellent erase operation is observed despite its slower mobility compared to Cu_2O.

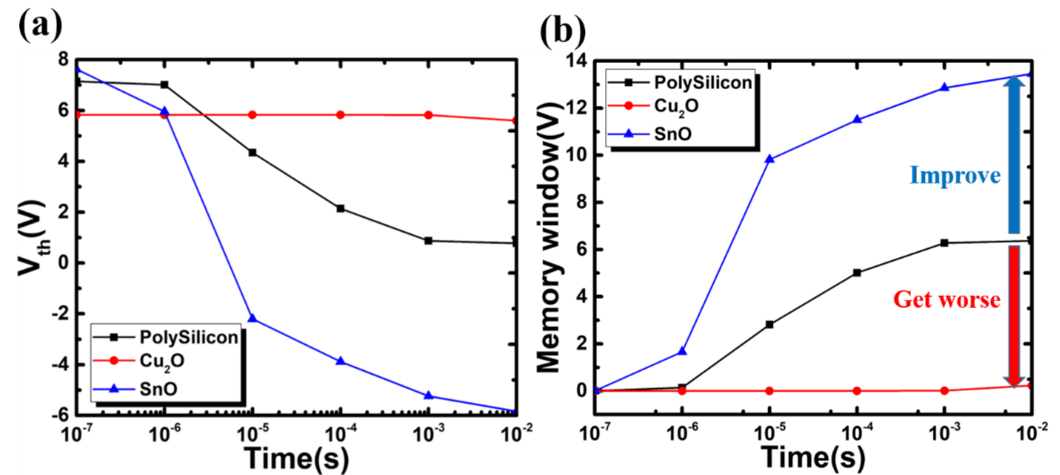

Figure 3. (**a**) Change in the threshold voltage over erase operation time; (**b**) change in the memory window calculated from the result of (**a**).

Figure 3b shows the memory window (programmed V_{th}—erased V_{th}) change calculated from the results in Figure 3a. Notably, in Figure 3b, the erase operation performance of SnO fillers improves more than twice as much as that of polysilicon fillers. Therefore, with the proposed structure, it is anticipated that not only can the problem of the erase operation difficulty, which arises when the IGZO channel is applied, be addressed, but also an improvement in the erase operation performance can be expected. In addition, Cu_2O, characterized by high mobility but low carrier density, exhibited very poor efficacy in erase operations as a filler. In contrast, SnO, with contrasting properties, showed excellent performance in erase operations. Based on these findings, it can be inferred that carrier density is more crucial than mobility in determining the effectiveness of the material used as a filler.

To analyze the root cause of the disparity in the erase operation speed observed in Figure 3, a detailed investigation of various electrical states during the erase operation process (1 µs) was conducted corresponding to the different filler materials, as shown in Figure 4.

In the case of polysilicon fillers, as depicted in Figure 4a, the filler itself exhibits a high hole density, but these holes are not transferred to IGZO. Consequently, as shown in Figure 4d, within the IGZO channel, despite a high voltage of 17 V (yellow) at the inter-face with the filler, there is a sharp voltage drop of 10 V (green) at the interface with the tunnel oxide on the opposite side. As shown in Figure 4g, this results in a high electric field of up to 10 MV/cm being applied to the IGZO channel, indicating the potential ad-verse effect on the reliability of the IGZO channel. In the case of Cu_2O fillers, the filler exhibits poor performance in terms of both hole density and potential distribution, as shown in Figure 4b,e, respectively. These results reveal that when the P-type carrier density is as small as 10^{15} cm^{-3}, it becomes ineffective because there are few carriers available to transfer holes, regardless of the mobility. In the case of SnO fillers, the filler exhibits much slower mobility compared to Cu_2O fillers, but shows an ideal hole density and potential distribution, as shown in Figure 4c,f, respectively. In particular, it was confirmed that the hole density in the IGZO channel can be increased to 10^{20} cm^{-3} within an initial erase time of 1 µs, attributed to the high density of the P-type carrier that transfers holes. In addition, because there are few barriers due to the bandgap being similar to that of IGZO, the electric field distribution of IGZO remains very stable at around 2 MV/cm, as shown in Figure 4i. These results also demonstrate that the voltage is evenly distributed across the IGZO channel.

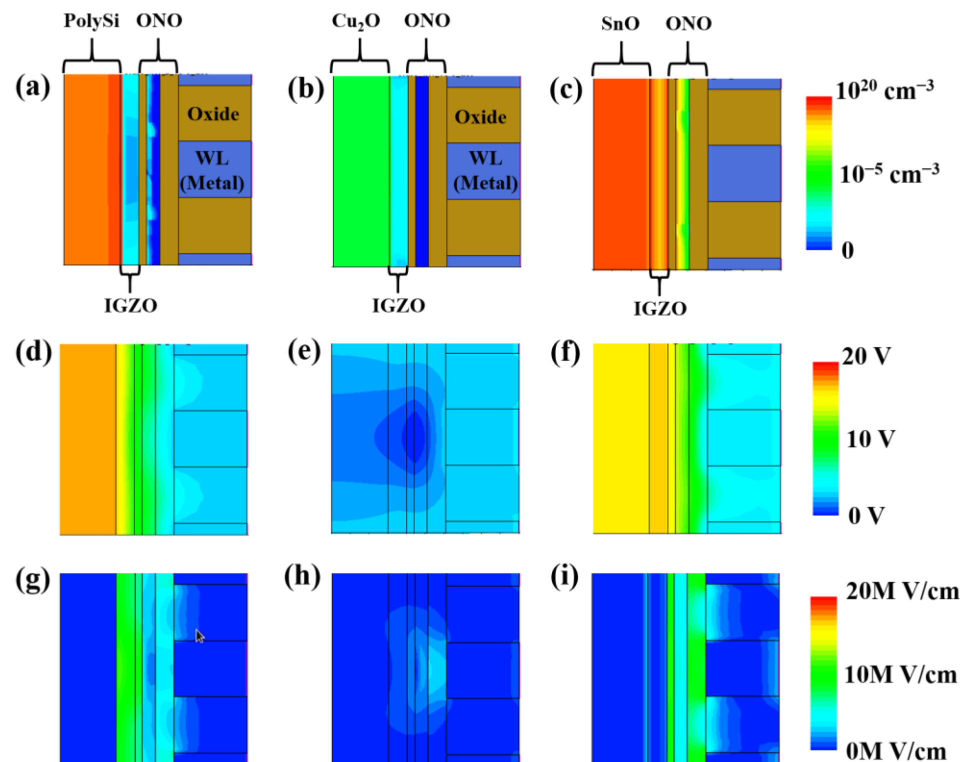

Figure 4. Result of state analysis for each material at the initial time (1 μs) of the erase operation: (**a**–**c**) show the hole density distribution, (**d**–**f**) show the electric potential distribution, and (**g**–**i**) show the electric field distribution.

In summary, it was confirmed that the most important factor in the selection of the P-type filler material to be used in the proposed structure is the P-type carrier density, while mobility is relatively insignificant. This result is encouraging because, in actual oxide semiconductors, mobility improvement generally involves a trade-off relationship with reliability improvement. Therefore, the fact that mobility is not deemed crucial can be considered a strength in terms of reliability.

3.3. Simulation Analysis to Establish Optimal Filler Material Parameters

As previously described, most attempts to improve the material properties of oxide semiconductors to date, especially P-type oxide semiconductors, have often sacrificed reliability. Therefore, in this section, our goal is to determine the optimal parameters for the erase operation by combining the material parameters of the two types of oxide semiconductors. This involves increasing the carrier density and band gap from the lowest state.

Figure 5 shows the results of the erase operation speed at different carrier densities and band gaps, while the mobility of the P-type oxide semiconductor used as a filler is fixed at 10 cm^2/V-s. Among the previous results, as confirmed in the case of SnO fillers, it was observed that the mobility of the material used as a filler did not significantly contribute to the improvement in the erase operation performance. Instead, it was evident that the bandgap and P-type carrier density played more crucial roles. Consequently, we adjusted the other conditions with the mobility fixed to an operable minimum.

First, when comparing the erase operation speed shown in Figure 5a,b, it can be observed that a satisfactory erase operation (with a V_{th} of -2 V or lower) occurs only when the carrier density of the oxide semiconductor used as a filler is 10^{19} cm^{-3}, regardless of the band gap. While it may be conceivable at a carrier density below that, for instance, approximately 5×10^{18} cm^{-3}, it is deemed essential for optimal performance to maintain a carrier density of 10^{19} cm^{-3}, as elucidated in subsequent discussions. Next, examining the

potential change in the IGZO channel during the erase operation according to the band gap, as shown in Figure 5d–f, when the band gap is 2.5 eV, the potential of the channel only rises to 14.5 V, even if the carrier density has reached 10^{19} cm^{-3}. This is attributed to a band gap of 2.5 eV, indicating that the hole density of the IGZO channel is not completely filled due to the formation of the IGZO channel and a barrier with a band gap of 3.1 eV. However, if the band gap is 3.0 eV, there is a minimal barrier, as there is only a 0.1 eV difference from the band gap of the IGZO channel. Consequently, it can be observed that the channel voltage has risen to 17.6 V due to the holes filled in the channel. Moreover, when the band gap reaches 3.5 eV, the potential of the IGZO channel rises to 18.2 V, as illustrated in Figure 5f. It is thought that this difference resulted in the varying erase operation performances shown in Figure 5a–c at the same carrier density.

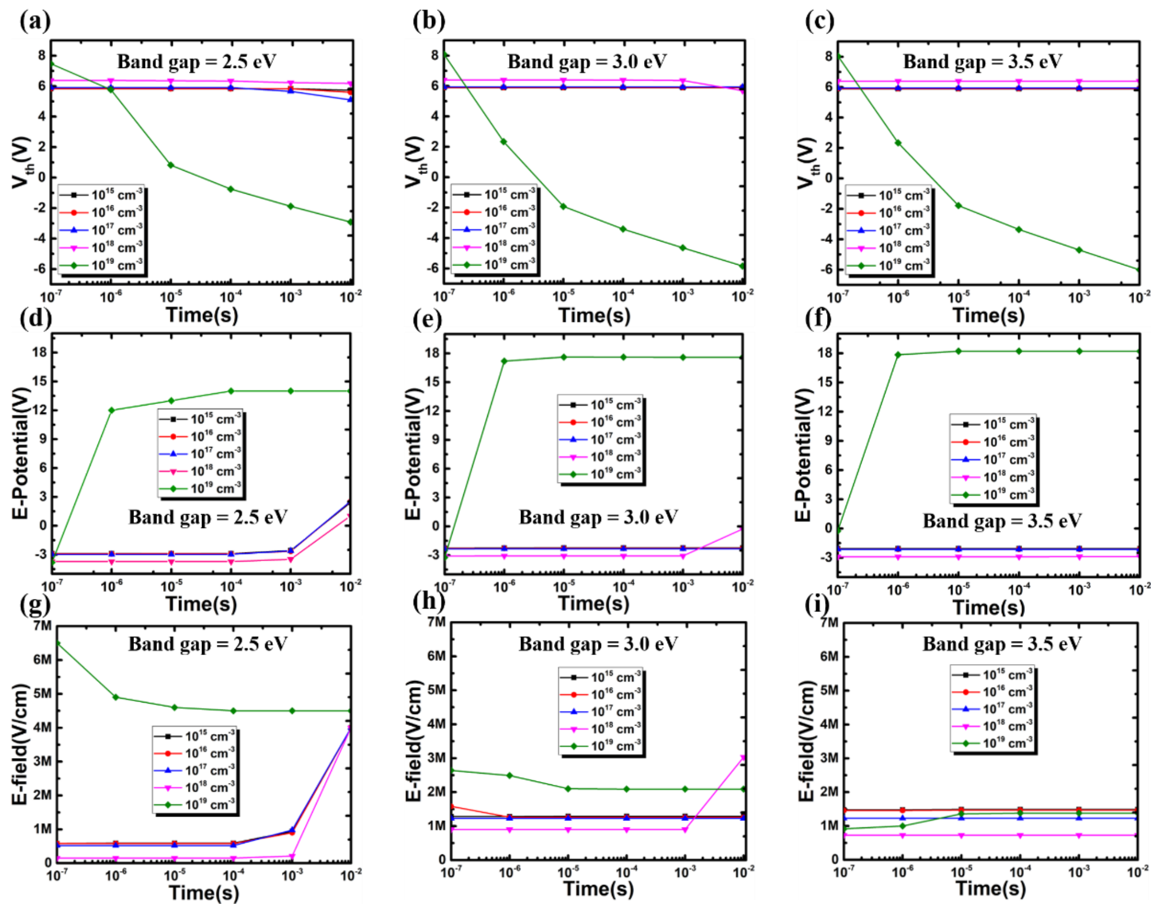

Figure 5. Analysis results of the erase operation at different carrier densities and band gaps of the P-type oxide semiconductor used in the filler. (**a**–**c**) Threshold voltage during the erase operation, (**d**–**f**) potential of the IGZO channel during the erase operation, (**g**–**i**) electric field applied to the IGZO channel at the same time zone.

Finally, Figure 5g–i explain the rationale behind the aforementioned minimum carrier density of 10^{19} cm^{-3}, and the requirement for a 3.0 eV bandgap. First, examining Figure 5g, where the bandgap is 2.5 eV, it is evident that the electric field applied to the IGZO channel reaches a maximum of 6.5 MV/cm. The issue lies in the fact that the carrier density associated with this highest electric field is 10^{19} cm^{-3}, in which the erase operation would be well facilitated by increasing the carrier density at a bandgap of 2.5 eV. However, this resultant high electric field induces continuous stress on the IGZO channel during the erase operation, presenting a significant reliability issue. Conversely, in Figure 5h, where the bandgap is 3.0 eV, the maximum electric field during the erase operation is 2.6 MV/cm. This represents an applied electric field of less than 1/3 compared to the result shown in Figure 5g. Consequently, the stress applied to the IGZO channel is also less than 1/3,

leading to an increase in reliability of more than three times, even using simple calculations. Furthermore, with a bandgap of 3.5 eV, the electric field applied to the IGZO channel decreases to 1.86 MV/cm, as illustrated in Figure 5i. It can be inferred from this result that if the bandgap of the P-type oxide semiconductor used as a filler is the same as or larger than that of the IGZO channel, it is suggested that the erase operation performance could be enhanced while mitigating the stress applied to the IGZO channel above a specific carrier density. However, increasing the bandgap is deemed necessary with a cautious approach, as it is recognized to adversely affect other material properties.

In conclusion, it is predicted that the minimum specifications of P-type oxide semiconductors to be used as fillers in the proposed structure should have a mobility of about 10 cm^2/V-s, a band gap of 3.0 eV or more, and a P-type carrier density of 10^{19} cm^{-3} or more.

4. Conclusions

In this paper, we proposed a new IGZO filler structure by applying a P-type oxide semiconductor as the filler material. In particular, the tin oxide used in this work demonstrated excellent erase operation performance due to its high band gap and abundant hole carrier density, which does not form a barrier hindering hole movement, despite having significantly poorer mobility compared to the polysilicon filler. The simulation results indicate that the hole erase operation performance of the proposed IGZO filler structure surpassed that of the polysilicon filler structure, showing a memory window more than twice as large. It was further confirmed that the electric field applied to the IGZO panel was significantly reduced owing to the abundant hole movement. Subsequently, we conducted a simulation to determine the minimum specifications required for the filler material to achieve optimal erase operation performance. The results indicated that the mobility was not significantly correlated, but the band gap should be at least 3.0 eV and the P-type carrier density should be at least 10^{19} cm^{-3}. When applying P-type oxide semiconductor fillers meeting these conditions, IGZO materials emerge as the best solution for use as channels in 3D NAND flash memory applications.

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