Article

25-cm^2 glass-like transparent crystalline silicon solar cells with an efficiency of 14.5%

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Highlights

25-cm^2 c-Si TPV shows efficiency of up to 14.5% at a transmittance of 20%

Chemical surface treatment improves surface quality of transparent c-Si wafers

Chemical surface treatment enables facile transmittance control of c-Si TPV

Chemical treatment allows high efficiency, scale up, and transmittance control

PCE: 14.5% @ T=20%

5 cm

A simple but effective chemical surface treatment method for removing surface damage from c-Si microholes is proposed by Park et al. A 25-cm^2 large neutral-colored transparent c-Si solar cell with chemical surface treatment exhibits the highest PCE of 14.5% at a transmittance of 20% by removing the damaged surface of c-Si microholes.

Article

25-cm² glass-like transparent crystalline silicon solar cells with an efficiency of 14.5%

Jeonghwan Park,[1,2] Kangmin Lee,[1,2] and Kwanyong Seo[1,3,*]

SUMMARY

Forming light-transmitting structures on c-Si photovoltaics to transmit visible light without wavelength dependency is a promising strategy to realize neutral-color transparent c-Si photovoltaics (c-Si TPVs). However, dry etching, which is used to form a light-transmitting structure on c-Si, inevitably causes nanoscale surface damages such as scallops and plasma-induced damage in c-Si. This aggravates carrier recombination, which decreases power conversion efficiency (PCE) of c-Si TPVs. Here, we propose an effective chemical treatment method for removing nanoscale surface damage from c-Si microholes. A large neutral-color c-Si TPV after the chemical treatment exhibits a high PCE of 14.5% at a transmittance of 20%. The chemical treatment also enables systematic control of the hole size (167 nm/s), and, thus, the transmittance is easily tuned from 10% to 70%. The proposed chemical treatment satisfies the three development factors of (1) high PCE, (2) opportunity for scale up, and (3) facile light transmittance tuning of c-Si TPVs.

INTRODUCTION

Transparent photovoltaics (TPVs) are in the spotlight as promising energy conversion devices that can expand the applicability of solar cells. This is because they can be applied to various fields in our daily life such as windows of buildings and vehicles where the application of conventional opaque PVs is difficult.[1,2] Enabling the partial transmission of incident light in the visible region from 400 to 750 nm, which can be recognized by the human eye, is an essential prerequisite to realize a practical TPV. In this regard, thin-film and selective light-transmission technologies have been mainly used to enable partial transmission of the visible light by PVs.[3–8] Among them, selective light-transmission technology is a method that transmits light in the visible region through selective light-transmission regions, while maintaining the conventional PV structure. In addition, selective light-transmission technology allows visible transparency regardless of the thickness of a crystalline silicon (c-Si) wafer, which is known as opaque.[8]

As a representative example, neutral-color c-Si TPVs reported by Lee et al. employ selective light-transmission technology. Lee et al. placed microhole arrays as light-transmission windows, which are not visible to the naked human eye, on a 200-μm-thick c-Si wafer. The device demonstrated a power conversion efficiency (PCE) of 12.2% at a light transmittance of 20% with a cell size of 1 cm², which is the record PCE among reported neutral-color TPVs.[8] However, the device had serious defective sites on the sidewall of c-Si microholes due to the side effect of the deep reactive ion etching (DRIE) method.[9–12] Although the DRIE method is powerful for fabricating structures with high precision and reproducibility, permanent surface damage inevitably occurs owing to high-energy-plasma-based etching processes on the target

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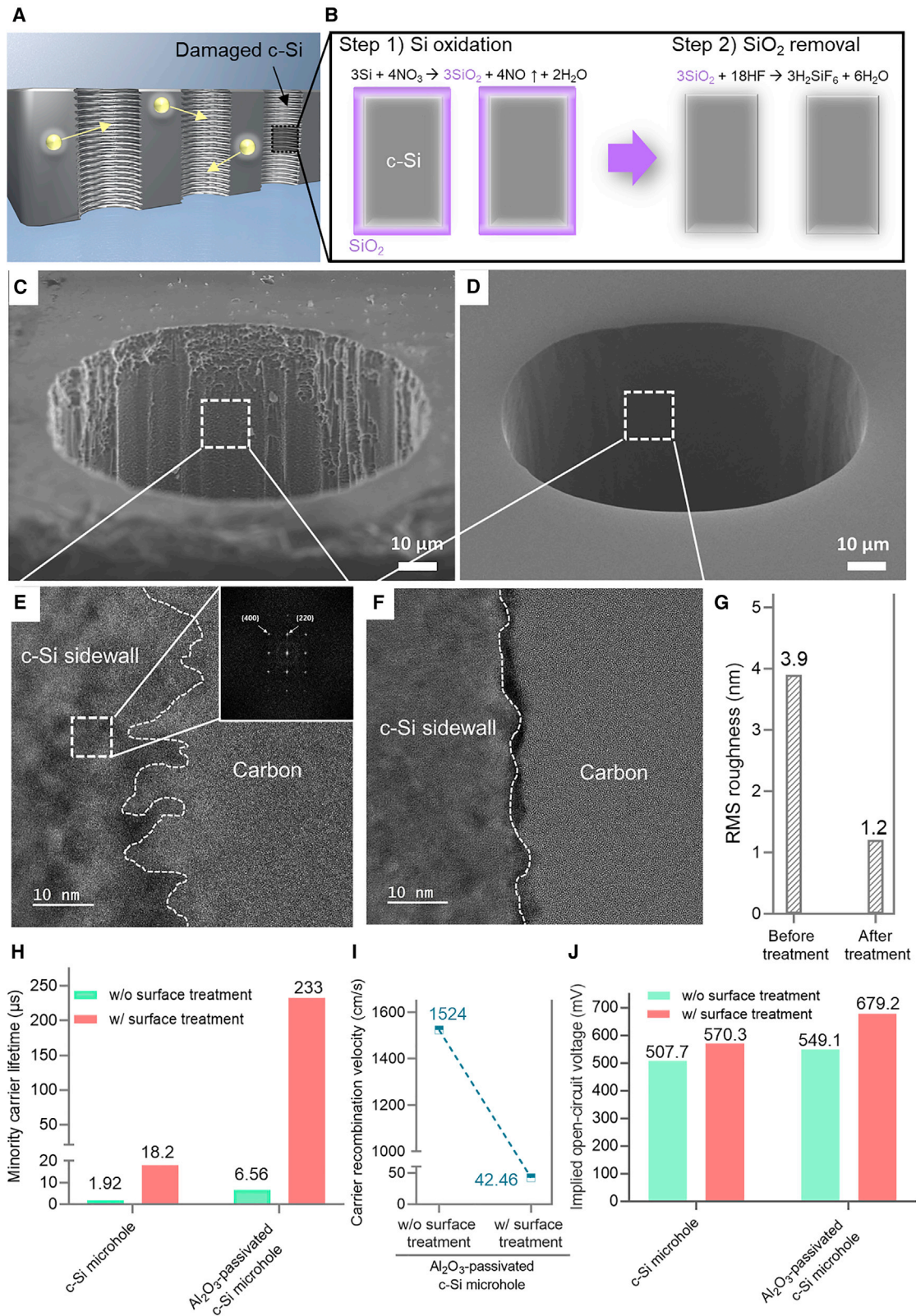https://doi.org/10.1016/j.xcrp.2021.100715

substrate.[13,14] The increased surface defect density increases the carrier recombination velocity in c-Si substrates.[15] Moreover, permanent surface damage such as dangling bonds and dislocations are generated in c-Si crystal structures because of the plasma state ion bombardment caused by DC bias.[16–18] Because of the two inherent limitations above, the increase in the PCE of c-Si TPVs is limited. Even though an Al_2O_3 passivation layer was applied to the surface of c-Si microholes, which is the light-transmission region, it only showed an open-circuit voltage (V_{oc}) of up to 588 mV.[8] In addition, the defective area will increase as the device size is increased for practical applications. Therefore, further research is required to overcome the fundamental limitations occurring in the etching process, and a strategy for improving the minority carrier lifetime should be proposed to improve V_{oc}.[8]

In this study, we propose a simple but powerful chemical wet-etching method using an $HF/HNO_3/CH_3COOH$ (HNA) solution for removing the DRIE process-induced surface damage from c-Si microholes. As the HNA solution has an isotropic etching property for c-Si, the solution can etch in all directions equally regardless of the c-Si crystal orientation. Because of this characteristic, conformal etching is possible on the damaged region of the entire c-Si surface. We confirm that the entire defective sidewall of the c-Si microholes is smoothened through the chemical surface treatment. Moreover, through the chemical surface treatment, it is confirmed that the minority carrier lifetime and implied V_{oc} of the device dramatically improve from 6.56 μs and 549.1 mV (without chemical surface treatment) to 233 μs and 679.2 mV (with chemical surface treatment), respectively. Moreover, the improvement in surface quality enables scaling up the device size. As a result, the fabricated large-scale neutral-color TPV exhibits a maximum PCE of 14.5% (transmittance = 20%, cell size = 25 cm²) corresponding to a V_{oc} of 638 mV, short-circuit current density (J_{sc}) of 28.9 mA/cm², and fill factor (FF) of 78.8%. Furthermore, the chemical surface treatment enables systematic control of the microhole diameter by a constant etching rate (10 μm/min), while removing the surface damage from the microholes. As the diameter of the c-Si microholes increases from 70 μm (before the treatment) to 190 μm (after the treatment for 12 min), the light transmittance in the visible light region (400–800 nm) is systematically adjusted from 10% to 70%. In other words, the proposed method potentially possesses dual advantages of controlling the transmittance by changing the c-Si microhole diameter and eliminating the sidewall damage from c-Si microhole arrays.
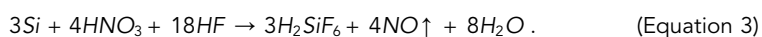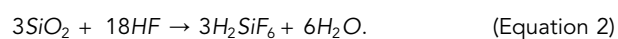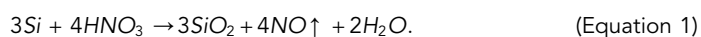
RESULTS AND DISCUSSION

Improvement in surface quality and passivation properties of transparent c-Si substrates

To impart transparency to a c-Si wafer, microhole arrays were employed as light-transmission windows throughout the wafer thickness. First, an Al etching mask was formed by the photolithography process, and, subsequently, c-Si microhole arrays were fabricated using the DRIE method (Figure S1). The transmission of all incident visible light was enabled owing to the c-Si microholes, and, thus, a transparent c-Si substrate and a c-Si TPV could be realized.[8] However, the DRIE method frequently generates scallops on the microhole sidewall. These scalloped surfaces increase the number of severe defect sites on the c-Si surface.[18] Furthermore, ion bombardment in the plasma state by applying a DC bias causes permanent surface damage to a c-Si substrate up to 30 nm.[16] Eventually, the surface recombination velocity of photo-generated carriers increases because of the above-mentioned surface damage to the c-Si substrate (Figure 1A).[18] As a result, the surface damage of c-Si significantly limits the PCE of c-Si TPVs owing to the loss of photo-generated carriers due to the carrier recombination. To overcome these limitations, we propose a

A

Damaged c-Si

B

Step 1) Si oxidation

$3Si + 4NO_3 \rightarrow 3SiO_2 + 4NO \uparrow + 2H_2O$

c-Si

SiO_2

Step 2) SiO$_2$ removal

$3SiO_2 + 18HF \rightarrow 3H_2SiF_6 + 6H_2O$

C

10 μm

D

10 μm

E

c-Si sidewall

(400) (220)

Carbon

10 nm

F

c-Si sidewall

Carbon

10 nm

G

RMS roughness (nm)

3.9

1.2

Before treatment   After treatment

H

Minority carrier lifetime (μs)

■ w/o surface treatment
■ w/ surface treatment

233

18.2

1.92

6.56

c-Si microhole   Al$_2$O$_3$-passivated c-Si microhole

I

Carrier recombination velocity (cm/s)

1524

42.46

w/o surface treatment   w/ surface treatment

Al$_2$O$_3$-passivated c-Si microhole

J

Implied open-circuit voltage (mV)

■ w/o surface treatment
■ w/ surface treatment

507.7   570.3

549.1   679.2

c-Si microhole   Al$_2$O$_3$-passivated c-Si microhole

simple but powerful method of removing surface damage from the sidewalls of c-Si microholes via chemical surface treatment using an HNA solution known as isotropic Si etchant. The HNA solution consists of a mixture of hydrofluoric acid (HF), nitric acid (HNO$_3$), and acetic acid (CH$_3$COOH). The wet etching of c-Si using an HNA solution is common process in the semiconductor industry because of its simple and low-cost nature.[19–21] Figure 1B shows the etching mechanism of c-Si microhole arrays using the HNA solution. The etching mechanism of c-Si microholes can be divided into two steps, namely, Si oxidation and SiO$_2$ removal as outlined in Equations 1 and 2.[22] The overall etching mechanism of c-Si using the HNA solution is presented in Equation 3.

$$3Si + 4HNO_3 \rightarrow 3SiO_2 + 4NO\uparrow + 2H_2O. \quad \text{(Equation 1)}$$

$$3SiO_2 + 18HF \rightarrow 3H_2SiF_6 + 6H_2O. \quad \text{(Equation 2)}$$

$$3Si + 4HNO_3 + 18HF \rightarrow 3H_2SiF_6 + 4NO\uparrow + 8H_2O. \quad \text{(Equation 3)}$$

The HNA solution is a representative isotropic Si etchant that enables Si etching in all directions regardless of the c-Si crystal orientation. Figures 1C, 1D, and S2 show scanning electron microscopy (SEM) images of a c-Si microhole before and after the chemical surface treatment using the HNA solution. As shown in the SEM images, the DRIE-etched c-Si microholes (diameter [D] = 100 μm) contain a severely rough surface (Figures 1C and S2A). In contrast, when the c-Si microhole surface was chemically treated using the HNA solution for 120 s, a clean and smooth surface on the entire sidewall was observed, as damaged c-Si was removed (Figures 1D and S2B). Furthermore, the sidewall morphology of the c-Si microholes was investigated in detail by high-resolution transmission electron microscopy (HR-TEM). As shown in the TEM image of Figure 1E, nanosized scallops were observed on the surface of a c-Si microhole fabricated via the DRIE process. Because a transparent c-Si wafer contains many microholes as an array, the number of localized nanoscale surface defects of the c-Si microholes significantly increase, which indicates that the carrier recombination problem may worsen.[23–25] Furthermore, as shown in the fast Fourier transform (FFT) pattern image in the inset of Figure 1E, the sidewall surface of the c-Si microhole shows multiple crystal planes ({400} and {220}). Nevertheless, the sidewall surface of the c-Si microhole was etched regardless of the crystal plane owing to the isotropic etching property of the HNA solution, so that the smooth surfaces of the sidewall were clearly observed (Figure 1F). In addition, the surface defects of the c-Si microhole can be quantitatively analyzed by estimating the root mean square (RMS) roughness value based on the TEM images. The RMS roughness value of the c-Si microhole sidewall before and after the chemical surface treatment was estimated to be 3.9 and 1.2 nm, respectively, indicating that the RMS roughness value decreased by more than three times through the chemical surface treatment (Figure 1G). Consequently, we confirmed that the damaged surface of the c-Si

Figure 1. Chemical surface treatment to remove the damaged surface of c-Si microholes

(A) Schematic illustration of the minority carrier recombination process in the damaged c-Si microholes.

(B) Chemical surface treatment mechanism of the c-Si microholes using an RSE-100 etchant.

(C) SEM images of a c-Si microhole before the chemical surface treatment.

(D) SEM images of the surface-treated c-Si microhole using an HNA solution for 120 s.

(E) TEM images of the untreated c-Si microhole sidewall. The inset shows the FFT dot pattern of the c-Si microhole sidewall region.

(F) TEM images of the surface-treated c-Si microhole sidewall.

(G) Comparison of the calculated RMS roughness of the c-Si microhole sidewalls without (w/o) and with (w/) chemical surface treatment.

(H) Minority carrier lifetimes of the bare and Al$_2$O$_3$-passivated c-Si microhole substrates for w/o (green) and w/ (red) the chemical surface treatment.

(I) Calculated surface recombination velocities of the Al$_2$O$_3$-passivated c-Si microhole substrates w/o and w/ the chemical surface treatment.

(J) Implied V_{oc} of the bare and Al$_2$O$_3$-passivated c-Si microhole substrates for w/o (green) and w/ (red) the chemical surface treatment.

microhole generated by the DRIE process can be effectively removed through the chemical surface treatment using the HNA solution.

For quantitatively determining the change in PV characteristics depending on the surface damage removal of the c-Si microhole arrays, the minority carrier lifetimes of the transparent c-Si substrates before and after the chemical surface treatment were measured using the quasi-steady-state photo-conductance (QSSPC) (Sinton, WCT-120) method (Figure 1H). First, we measured the minority carrier lifetime of the transparent c-Si substrate depending on the chemical surface treatment time. Although the minority carrier lifetime of the transparent c-Si substrate before the chemical surface treatment was 1.92 μs, it rapidly increased with the surface treatment time. After 30 s treatment, the minority carrier lifetime was saturated to be approximately 18.0 μs. We confirmed that it increased by 9.4 times, as compared with that of the untreated sample (Figure S3). Additionally, to fabricate high-PCE c-Si TPVs, not only surface treatment but also a surface passivation process should be considered. This is because in addition to removing the damaged c-Si surface, the surface recombination of photo-generated carriers should be minimized by saturating the dangling bonds at the c-Si interface. To compare the passivation characteristics of the transparent c-Si substrates before and after the chemical surface treatment, 10-nm-thick Al_2O_3 layers were deposited on the transparent c-Si substrates via atomic layer deposition (ALD). As a result, in the case of the transparent c-Si substrate the surface of which was not chemically treated, the change in the carrier lifetime of the substrate after the passivation with an Al_2O_3 layer exhibited only a slight increase from 1.92 to 6.56 μs. Although the passivation layer can effectively compensate for the dangling bonds on the c-Si surface, it cannot control the recombination process generated by the DRIE process-induced subsurface damage of up to 30 nm deep in c-Si.[16] In contrast, in the case of the transparent c-Si substrate after the chemical surface treatment, the minority carrier lifetime of the substrate after depositing an Al_2O_3 layer showed a significant improvement from 18.2 to 233 μs (Figure 1H). In addition, by calculating the carrier recombination velocity based on the measured carrier lifetime, the passivation quality of the transparent c-Si substrates before and after the chemical surface treatment was verified (Equation 4).

$$S_{eff} = \frac{W}{2} * \left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{in}} \right). \qquad \text{(Equation 4)}$$

Here, S_{eff}, W, τ_{eff}, and τ_{in} denote the carrier recombination velocity, wafer thickness, minority carrier lifetime, and intrinsic bulk carrier lifetime, respectively. W is 200 μm, and τ_{in} is 18,283 μs, referring to the product certificate of Topsil-produced float zone (FZ) n-type c-Si wafers. Consequently, S_{eff} can be obtained using τ_{eff} measured from the Al_2O_3-passivated transparent c-Si substrates. The S_{eff} values of the substrates before and after the chemical surface treatment were obtained to be 1,524 and 42.46 cm/s, respectively (Figure 1I). Because a S_{eff} of lower than 50 cm/s is required to achieve high PCE of c-Si solar cells with a surface structure, the decreased S_{eff} value would be a cornerstone for the realization of high-PCE c-Si TPVs.[23,25] Additionally, to confirm the potential PV characteristics of the transparent c-Si substrates as actual solar cells, the implied V_{oc} under the one sun condition was measured using QSSPC. As a result, when Al_2O_3 passivation was performed on the substrate the surface of which was not treated, the implied V_{oc} of the substrate increased by about 40 mV from 507.7 mV to 549.1 mV. In contrast, when an Al_2O_3 layer was coated on the surface-treated transparent c-Si substrate, the implied V_{oc} was increased to 678.2 mV, resulting in a drastic enhancement of about 110 mV, as compared with the substrate without a passivation layer (Figure 1J). The bottom line is that the proposed chemical surface treatment process is important for improving surface quality of transparent c-Si wafers to realized high-PCE c-Si TPVs.

Systematic transmittance tuning of transparent c-Si substrates

Another advantage of the chemical surface treatment using the HNA solution is the systematic tuning of the light transmittance by controlling the c-Si microhole diameter, while improving the surface quality of the c-Si microhole arrays (Figure 2A). The surface chemical etching was performed by immersing the substrate in the HNA solution after fabricating a transparent c-Si substrate with a diameter of 70 μm as an initial substrate. As the chemical etching time was increased, the c-Si microhole diameter increased from 70 to 190 μm after etching for 12 min. The etch rate was determined to be about 10 μm/min (Figure 2B). Figures 2C–2F show the top-view SEM images of the c-Si microhole arrays according to the etching time. As the etching time was increased, the microhole diameter increased, while maintaining a uniform circular shape in all directions. To measure the light transmittance of the transparent c-Si substrates fabricated according to the chemical etching time, the total transmittance (specular transmittance + diffuse transmittance) was measured using an ultraviolet-visible-near infrared (UV-Vis-NIR) spectrophotometer. The average light transmittance in the visible wavelength region (400–750 nm) was systematically controlled from 10% (without chemical etching) to 70% (with chemical etching for 12 min) depending on the etching time (Figure 2G). In a previous report, to realize the desired light transmittance of a transparent c-Si substrate, different sets of the diameter and spacing of c-Si microhole arrays were designed separately, and relevant photolithography, Al mask formation, and DRIE processes were used for each case.[8] In contrast, in the case of the wet-etching method using the HNA solution, a substrate with the desired transmittance from low to high can be obtained by adjusting only the wet-etching time (Figure S4). Figure 2H shows a photograph of transparent c-Si substrates with different transmittance values. We successfully fabricated transparent c-Si substrates exhibiting various light transmittance values from 10% (without chemical etching) to 70% (12 min etching).

Photovoltaic performance of large-size c-Si TPVs

Scaling up the device size and increasing the PCE are key problems in practical use of TPVs. In this work, we aimed to realize a high-PCE and large-size c-Si TPV with a size of at least 25 cm^2 because we successfully developed a simple and powerful surface treatment method to minimize the number of surface defects. Figure 3A shows a schematic of our c-Si TPV. The fabricated c-Si TPV with a size of 25 cm^2 was demonstrated as following the fabrication process (Figure 3B). The c-Si TPV fabrication process involved the following key steps: (1) transparent c-Si substrate fabrication and subsequent chemical surface treatment using the HNA solution, and (2) PV device fabrication (Figure 3C). First, microhole arrays were formed on an n-type c-Si substrate to prepare a transparent c-Si substrate (Figure S1), and, subsequently, surface damage of the c-Si microholes was removed through the chemical surface treatment using the HNA solution. To fabricate a c-Si TPV, a p-n junction was formed on the transparent c-Si substrates by the spin-on-dopant method. Before the formation of the p-n junction, a 2-μm-thick SiO$_2$ layer was selectively formed on the sidewall of the microholes via plasma-enhanced chemical deposition (PECVD) and the subsequent etching process. The SiO$_2$ layer would act as a diffusion barrier for the p-type dopants to prevent short circuit. After the doping process, a 10-nm-thick Al$_2$O$_3$ layer was deposited through the ALD process to minimize the surface recombination induced by the dangling bonds on the surface of the c-Si microholes. In addition, to minimize the surface light reflection, a 70-nm-thick SiN$_x$ layer was deposited on the front surface using PECVD. An microgrid electrode with a 200 μm spacing and a 2 μm width was then applied as the front electrode. The microgrid electrode had a uniform square pattern structure, which enabled efficient carrier collection
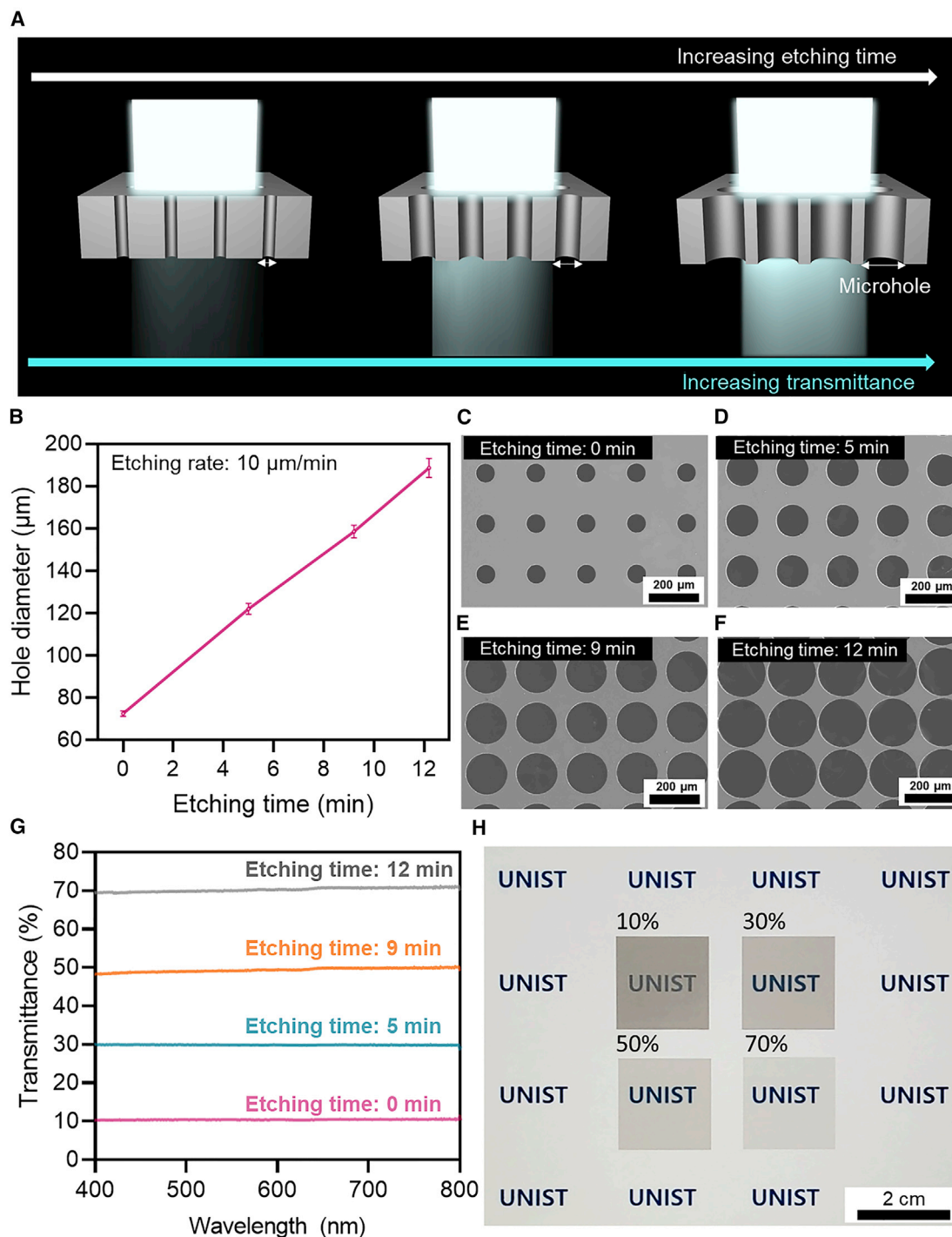
Figure 2. Systematic tuning of the transmittance by controlling the diameter of the c-Si microholes using an HNA solution

(A) Illustration of systematic transmittance tuning via microhole size control.

(B) Hole-diameter variations with respect to the etching time using the HNA solution.

(C–F) SEM images of the c-Si microholes with an etching time from 0 to 12 min.

(G) Total transmittance spectra of the transparent c-Si substrates with an etching time of 0 (pink line), 5 (cyan line), 9 (orange line), and 12 min (gray line) for wavelengths in the range of 400–800 nm.

(H) Photograph of the transparent c-Si substrates fabricated by etching with different transmittance values from 10% to 70%.

A

B

C
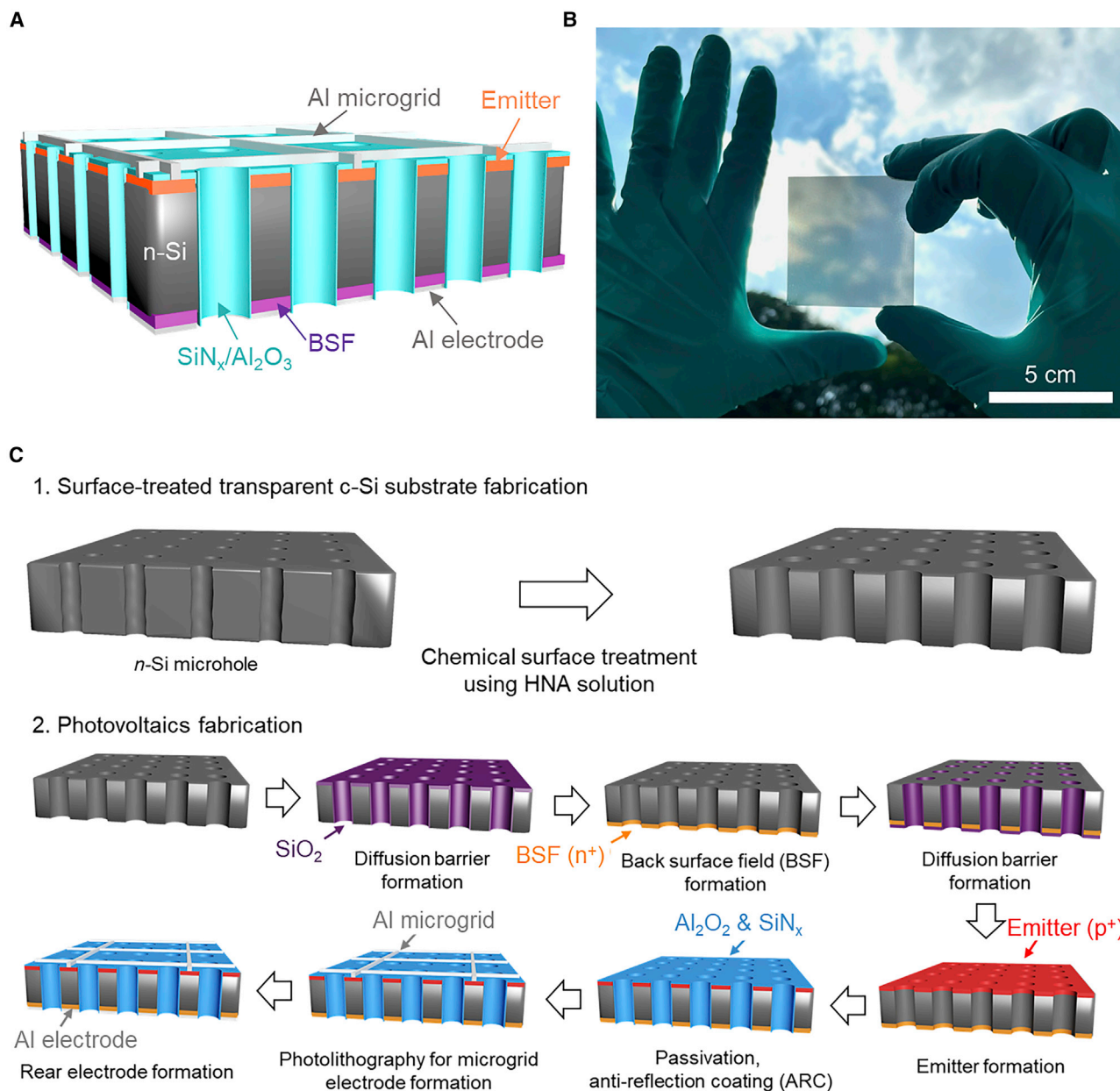
**Figure 3. Fabrication of large c-Si TPVs**
(A) Schematic representation of a c-Si TPV.
(B) Photographic image of a 25-cm^2 c-Si TPV with a transmittance of 20%.
(C) Schematics representations showing the fabrication process of a c-Si TPV.

for high *FF*.[26] Finally, as the rear electrode, 500-nm-thick aluminum (Al) was deposited by thermal evaporation.

To evaluate the PV characteristics of the fabricated c-Si TPVs with a size of 25 cm^2 (Figure 3B), the current density-voltage (*J-V*) curve was obtained under AM 1.5G illumination (Figure 4A). The PV parameters are summarized in Table 1. In the case of the c-Si TPV the surface of which was not chemically treated, a V_{oc} of 548 mV, a J_{sc} of 28.0 mA/cm^2, an *FF* of 71.0%, and a PCE of 10.9% were achieved. In contrast, the c-Si TPV with the chemically treated surface exhibited a V_{oc}, 638 mV, a J_{sc}, 28.9
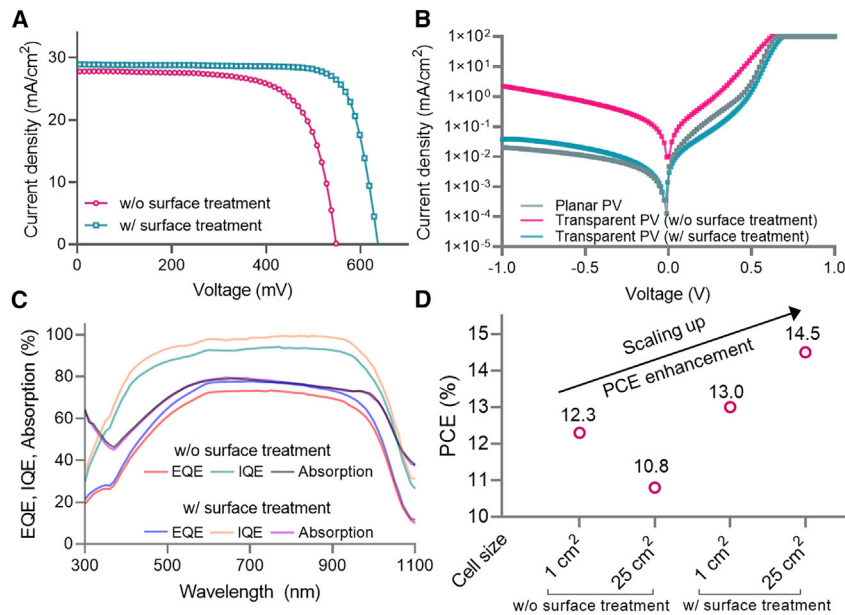
Figure 4. Performance of large c-Si TPVs

(A) *J–V* characteristics of the c-Si TPVs with and without chemical surface treatment under standard AM 1.5 G spectral conditions.

(B) Dark *J–V* curves of the c-Si TPVs with and without chemical surface treatment and planar PV.

(C) EQE, IQE, and absorption curves of the c-Si TPVs with and without chemical surface treatment.

(D) PCE comparison of the c-Si TPVs for different cell sizes and fabrication methods.

mA/cm^2, an *FF* of 78.8%, and a significantly improved PCE of 14.5%. Overall, the surface-treated device showed a drastic V_{oc} improvement of 90 mV, as compared with the untreated device. The V_{oc} improvement can be explained through Equation 5.[27]

$$V_{oc} = \frac{k_B T}{q} \ln \left(\frac{J_{sc}}{J_0} + 1 \right). \qquad \text{(Equation 5)}$$

Here, k_B, T, Q, J_{sc}, and J_0 denote Boltzmann's constant, temperature, electron charge, current density, and reverse saturation current density, respectively. As shown in the dark *J–V* curves in Figure 4B, there is a significant difference in the J_o value between the chemically treated and untreated devices at a reverse bias of −1 V. The c-Si TPV the surface of which is not chemically treated showed a high leakage current density of 2.26 mA/cm^2 at a reverse bias of −1 V under dark condition owing to the influence of the internal carrier recombination process in the c-Si microholes.[28,29] The J_o value was about 60 times higher at a reverse bias of −1 V, as compared with that of the surface-treated c-Si TPV. However, after the chemical surface treatment, the J_o value was close to that of the planar PV. The chemical surface treatment effectively reduced the number of carrier recombination sites on the sidewall of the c-Si microholes, thereby reducing the J_o value. Interestingly, as shown in Figure 4A and Table 1, the c-Si TPV the surface of which was chemically treated showed a higher J_{sc} of 1.1 mA/cm^2, as compared with the untreated c-Si TPV. The photocurrent improvement could be explained by the reduced carrier recombination. In other words, the surface-treated c-Si TPV showed lower J_o and higher J_{sc} than those of the untreated c-Si TPV, resulting in improved V_{oc}. As shown in the external quantum efficiency (EQE) spectra of the two devices in Figure 4C, the device the surface of which was chemically treated showed an enhanced EQE value, as compared with that of the untreated device. In addition, the device the surface of which was chemically treated showed an improved integrated J_{sc} (28.1 mA/cm^2), as

Table 1. Average photovoltaic properties of 25-cm² transparent c-Si solar cells

Device	J_{sc} (mA cm^{-2})	V_{oc} (mV)	FF (%)	E_{ff} (%)
Without chemical surface treatment	27.7 ± 0.30 (27.8)	538 ± 10.0 (548)	71.9 ± 1.25 (71.0)	10.7 ± 0.17 (10.8)
With chemical surface treatment	28.7 ± 0.15 (28.9)	631 ± 5.77 (638)	77.9 ± 2.29 (78.8)	14.1 ± 0.47 (14.5)

Average photovoltaic performances of three devices. The error range represents the standard deviation. The values in parenthesis are obtained from the champion device.

compared with that of the untreated device (26.5 mA/cm²) (Figure S5). We can infer that the chemical surface treatment enhances photocurrent by reducing carrier recombination.[28,29] To confirm the reduced carrier recombination, the internal quantum efficiency (IQE) was investigated in the entire wavelength region (300–1,100 nm). As shown in Figures 4C and S6, the total transmittance (T) and reflectance (R) of the two devices were measured using a UV-Vis-NIR spectrophotometer, and the absorption (A) value was calculated using the relationship of A (%) = 100-R-T. After that, the IQE value was derived using the relationship of IQE (%) = (EQE/A) * 100. When comparing the IQE responses of the devices before and after the chemical surface treatment, an improved IQE value of the surface-treated device was obtained in the entire wavelength region of 300–1,100 nm, although the A values of the two devices were almost same. Thus, we concluded again that the photocurrent was improved by mitigating the recombination of photo-generated carriers through the chemical surface treatment. Figure 4D shows the trend of PCE variations according to the surface treatment depending on the c-Si TPV size. The detailed PV parameters of the c-Si TPV with a size of 1 cm² are also summarized in Figure S7 and Table S1. In the case of 1-cm² c-Si TPVs, a PCE of the surface-treated device was obtained as 13.0% at a transmittance of 20%, indicating a PCE gain of 0.7%, as compared with that of the untreated device. In contrast, in 25-cm² c-Si TPVs, a PCE of the surface-treated device was obtained as the highest PCE of 14.5%, showing a significant PCE gain of 3.7%, as compared with that of the untreated 25 cm². In particular, the untreated 25-cm² c-Si TPV showed a low V_{oc}, resulting in significantly lower PCE than that of the untreated 1-cm² c-Si TPV. This result indicates that the carrier recombination would be further accelerated as the size of the c-Si TPV is increased. In contrast, the surface-treated device with a 25-cm² size showed an improved V_{oc} of 638 mV owing to the outstanding passivation quality. Furthermore, Suns-V_{oc} measurement was performed to confirm again the passivation effect attributed to surface treatment (Figure S8). The surface-treated 25-cm² solar cells have higher efficiency than the surface-treated 1-cm² solar cells because of the greater edge electrode area. In addition to the main grid electrodes, the edge electrode with a width of 500 μm was used on both the front and rear surfaces for photovoltaic performance measurements (Figures S9A and S9B). In general, the interface between the metal-Si contact leads to recombination.[30,31] When the cell size is 1 cm², the ratio of the Si/ Edge electrode contact area is 17.4%, while, on the other hand, the ratio of the Si/ Edge electrode contact area of the 25-cm² solar cell is 0.8% (Figure S9C). As a result, the 25-cm² device exhibits a reduced leakage current density by decreasing the number of recombination sites at the interface between the Si and the edge metal area (Figure S9D). Thus, the 25-cm² transparent solar cells obtained higher V_{oc} values than the 1-cm² transparent solar cells, ultimately resulting in a higher efficiency for the scaled-up device. Finally, even though the device size is 25 times larger than that of the previously developed c-Si TPV,[8] a higher efficiency by 14.5% was achieved, demonstrating both scaling up and high efficiency simultaneously. Furthermore, as shown in Figure S10 and Table S2, the 25-cm² transparent c-Si solar cells with various transmittances ranging from 20% to 50% were also

evaluated and were found to exhibit efficiencies of 14.5%–8.75%. The ability to produce transparent solar cells with such a range of transmittances is expected to maximize their applicability. This is the first step in practical research that can facilitate the commercialization of c-Si TPVs.

In summary, plasma-induced damage and scallops on c-Si microholes generated by DRIE were conformally removed via chemical surface treatment using an HNA solution. The surface-treated transparent c-Si substrates showed a significant improvement in the minority carrier lifetime and implied V_{oc} from 6.56 μs and 549.1 mV to 233 μs and 679.2 mV after the formation of an Al_2O_3 passivation layer, respectively. Accordingly, we demonstrated a large c-Si TPV owing to the enhanced surface passivation quality. In addition, the microhole diameter, which is the light-transmission region, increases with the chemical surface treatment time, so that the transmittance can be easily adjusted from 10% to 70%. Finally, the c-Si TPV the surface of which was chemically treated showed the highest PCE of 14.5% (V_{oc}: 638 mV, J_{sc}: 28.9 mA/cm^2, and FF: 78.8%) at a transmittance of 20% with a large cell size of 25 cm^2. Finally, to improve the efficiencies of such transparent c-Si solar cells, we have developed research roadmaps for enhancing their V_{oc} and J_{sc} values. In terms of V_{oc}, we are attempting to achieve a higher V_{oc} for the transparent device by employing the heterojunction with intrinsic thin-layer (HIT) or tunnel oxide passivated contact (TOPCon) structures. These structures will be expected to result in a high V_{oc} of about 700 mV through the introduction of ultimate passivation properties to c-Si. In terms of J_{sc}, it is expected that J_{sc} can be improved by employing surface structures capable of effective light trapping on the light absorption area (c-Si area). Based on these two perspectives, we plan further research related to improving the efficiencies of transparent c-Si solar cells. We expect that the development of transparent c-Si solar cells with an efficiency of >18% (transmittance = 20%) will be possible. To sum up, we successfully demonstrated high efficiency, scaling up, and even easy transmittance control of the c-Si TPV through the proposed chemical surface treatment. This would be a very remarkable study toward the commercialization of c-Si TPVs.

EXPERIMENTAL PROCEDURES

Resource availability

Lead contact
Further information and requests for resources should be directed to and will be fulfilled by the lead contact, Prof. Kwanyong Seo (kseo@unist.ac.kr).

Materials availability
This study did not generate new unique reagents.

Data and code availability
The authors declare that data supporting the findings of this study are available within the article and the Supplemental information. All other data are available from the lead contact upon reasonable request.

Fabrication of surface-treated transparent c-Si substrates
The transparent c-Si structures were fabricated using double-side polished FZ n-type (100) Si wafers with a thickness of 200 μm and a resistivity of 1–5 Ω·cm. Microhole arrays were periodically patterned using an AZ4330E photoresist (AZ Electronic Materials) via the photolithography process. A 400-nm-thick Al layer was deposited on the photoresist pattern as an etching mask. The microhole-array-patterned c-Si substrates were etched via the deep reactive ion etching (DRIE, Tegal 200) process with

a 1,500 W power source, 100 W stage power, and 45 mTorr gas pressure using source gases SF_6 (450 sccm) and C_4F_8 (200 sccm). The DRIE conditions were set to a uniform etching rate of about 3.33 μm/min. Therefore, it takes about 60 min to fabricate the microhole, and this process accounts for 68% of the total process cost. After the DRIE process, the Al metal mask was removed using an Al etchant (type A) for 5 min at 50°C, and a cleaning process was also performed using a piranha solution (a mixture of sulfuric acid [H_2SO_4] and hydrogen peroxide [H_2O_2]). Chemical surface treatment of the transparent c-Si substrate was performed by immersing the c-Si substrate in an $HF/HNO_3/CH_3COOH$ (HNA) solution (RSE-100, Transene).

Characterization of the transparent c-Si substrate

The surface morphology of the transparent c-Si substrate was characterized by field-emission scanning electron microscopy (FE-SEM, Hitachi S-4800). The sidewall of the microhole roughness was characterized by high-resolution transmission electron microscopy (HR-TEM, JEM-2100F). The minority carrier lifetime and the implied V_{oc} were determined using the quasi-steady-state photoconductance (QSSPC) method with WCT-120 manufactured by Sinton Instruments. The optical transmittance was determined using a UV-visible near-infrared spectrophotometer (Cary 5000, Agilent) equipped with a 110-mm integrating sphere.

Fabrication of transparent c-Si photovoltaics

After fabricating the surface-treated transparent c-Si substrate, a SiO_2 diffusion barrier of 2 μm was deposited on the front side of the substrate by using plasma-enhanced chemical vapor deposition (PE-CVD, PEH-600). After the formation of the SiO_2 diffusion barrier, a back surface field (BSF) layer was formed in a tube furnace under a mixed atmosphere of O_2 (125 sccm) and N_2 (500 sccm) at 880°C by using a phosphorous dopant source (P509, Filmtronics). The phosphorous silicate glass and SiO_2 diffusion barrier after the BSF formation were removed from the front of the substrate using a buffered oxide etchant (BOE). Subsequently, a SiO_2 diffusion barrier of 2 μm was redeposited on the rear side of the substrate by using PECVD. After that, an emitter layer was formed on the front surface of the substrate under N_2 (500 sccm) at 880°C by using a B dopant source (B155, Filmtronics). The SiO_2 diffusion barrier on the rear side was removed using a BOE solution. An Al_2O_3 passivation layer with a thickness of 10 nm was deposited on the front side of the wafer using atomic layer deposition (Lucida D100, NCD) and annealed under 500 sccm of mixed atmosphere of Ar/H_2 (96:4) at 500°C. In addition, a 70-nm-thick Si_3N_4 layer was deposited via PECVD as an antireflection coating. A photolithography process was carried out using an AZ9260 photoresist (AZ Electronic Materials) to develop a microgrid electrode as the top electrode. To conclude electrode fabrication, the substrate was dipped in a BOE solution for 3 min, and 600- and 400-nm-thick Al films were deposited on both sides of the substrate using thermal evaporation. The active area of the transparent c-Si photovoltaics was 25 cm^2.

Photovoltaic devices characterization

The photovoltaic properties of the transparent c-Si photovoltaics were investigated using a solar simulator (Class AAA, Oriel Sol3A, Newport) under AM 1.5G illumination. The incident flux was measured using a calibrated power meter and double-checked using a NREL-calibrated solar cell (PV Measurements). The transparent c-Si solar cells were measured from −1.0 to 1.0 V at a temperature of 25°C in air with a voltage scan rate of 380 mV/s. The EQE was measured using a Xe light source and a monochromator in the wavelength range of 300–1,100 nm. When measuring the J-V curves and the EQE of the c-Si TPV, the device area was calculated

as the total area, including both the light absorption region and the light-transmission area. Optical reflectance and transmittance measurements of the transparent c-Si photovoltaics were performed over wavelengths of 300–1,100 nm using a UV-Vis/NIR spectrophotometer (Cary 5000, Agilent) equipped with a 110-mm integrating sphere to account for the total light (diffuse and specular) reflected from the samples.

AUTHOR CONTRIBUTIONS

K.S. conceived the idea. J.P. and K.L. carried out the device fabrication, photovoltaic characterization, and analysis. J.P., K.L., and K.S. wrote the paper, and all authors commented on the manuscript.

DECLARATION OF INTERESTS

The authors declare no competing interests.

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